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A New Single-phase Symmetrical Cascade Multilevel Inverter with Low Number of Power Switches

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ABSTRACT

In this paper a new 5-level single phase symmetrical cascade multi-level inverter is proposed. The proposed topology contains combination of unidirectional and bidirectional power switches based on output voltage level number. The number of power switches and withstanding voltage of power swithces were reduced related to the other topologies. This configuration can be extended to the n-level inverter. In symmetrical case of proposed inverter the 5th harmonic output voltage will be eliminated. The performance analysis of the proposed inverter using suitable switching algorithm for producing the 5-level output voltage was confirmed by simulation and experimental results.

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NOMENCLATURE

N_u	*Number of unidirectional switches*	FC	Flying capacitor
N_B	Number of bidirectional switches	CHB	Cascade H-bridge
N_{level}	Number of volatge level	THD	Total Harmonic Distortion
N_{IGBT}	Number of IGBT	V_{DC}	DC source
S_n	Power switch	NPC	neutral point clamped

1. INTRODUCTION[1]

Application of DC power which is obtained by renewable energy sources such as photo voltaic (PV) systems and wind power plant require to AC power connection for safe operation. Because of significant interests in unlimited renewable energies applications in recent years, utilization of multilevel inverters as interface between DC and AC framework has become important topic in the field of power electronics especially in PV systems. The high number of PV cells with very low DC voltage generation is main reason for employing the multilevel inverters. Multilevel inverters contain a group of power electronic switches and DC voltage sources. In recent years, topologies and switching techniques of multilevel inverters were rapidly developed [1-4]. The most common and well known multilevel inverter configurations are Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB). The perverted voltage of neutral-point voltage in NPC inverter, unbalanced voltage in FC and large number of isolated DC volatge sources in CHB are the main disadvantages of these topologies [5, 6]. Therefore asymmetrical and hybrid multilevel topologies are becoming one of the most interesting alternatives. In asymmetrical CHB configurations, the magnitudes of DC voltage sources are unequal. These topologies reduce the cost and size of the inverter and improve the reliability since minimum number of IGBTs, capacitors, and DC voltage sources are utilized. The hybrid multilevel inverter are comprised different configurations with unequal DC

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voltage sources. With such converters, different modulation strategies and power electronic switches configuration are needed [7-16]. On the other hand, for efficiency improvement of conventional single-phase and three-phase inverters, different structures using bidirectional switches have been suggested in literature [17, 18]. bidirectional switch has been composed of two power switches or one power switch with four diodes. Comparing to the unidirectional switch, bidirectioanl switches can operate in both current directions. Bidirectional switches with a suitable switching algorithm can improve multilevel inverters performance; for example, IGBTs number reduction, blocking voltage minimization and attaining to the desired output voltage [19-24]. A new multilevel inverter presented in literature [22] has a limitation for generation of more output voltage levels. The magnitudes of the DC voltage sources should be unequal otherwise the number of output voltage levels decreases from seven to three. Therefore, DC voltage sources magnitudes should be unequal to produce more voltage levels without enhancement of the number of IGBTs. This structure is not general for any values of DC voltage sources and it is useful for asymmetrical cases. Based on this technical background, this paper suggests a simple topology for a single-phase CHB multilevel inverter. The numbers of switches, insulated-gate driver circuits are reduced significantly. In this paper a new topology is presented for any DC voltage sources magnitudes and it has no limitation for output voltage levels generation. In addition, the 5th harmonic of output voltage will be eliminated.

2. PROPOSED TOPOLOGY AND ITS OPERATION

Figure 1 depict the proposed single phase CHB topology for any value of DC voltage sources which contain two unidirectional power switches (S1, Sn) and n-2 bidirectional power switches where n is the number of DC voltage sources. The DC volatge sources in figure 1 can be a PV cell. According to Figure 1, six unidirectional power switches (S1 , Sn , T1 , T2 , T3 , T4) and n-2 bidirectional switches (S2 ,S3 ,..., Sn-1) were used in the proposed inverter. As shown in Figure 1 if power switches in the DC source side for example (S1, S2) or (S1, S3) are to be turn-on simultaneously, it causes the DC voltage sources to be short-circuited; therefore, the simultaneous turn-on of the these switches should be avoided. In this topology for 5-level output voltage generation does not require any bidirectional power switches which is illustrated in Figure 2. This is in contrast of the proposed inverter. Table 1 shows switching state of proposed 5-level inverter.

In Table 1, 1 and 0 represent the ON and OFF state of the switches respectively.

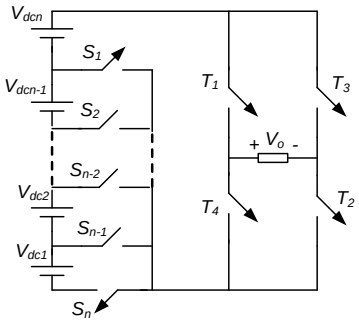

Figure 1. The proposed topology of single phase multi-level cascade inverter

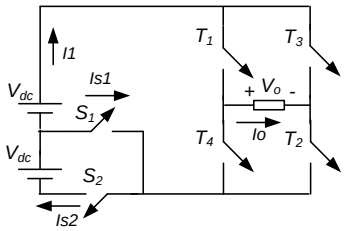

Figure 2. Proposed 5-level cascade inverter topology

TABLE 1. Switching states of proposed 5-level inverter

No.	S1	S2	T1	T2	T3	T4	Vo
1	1	0	1	0	1	0	0
2	1	0	1	1	0	0	V_{DC}
3	0	1	1	1	0	0	$2V_{DC}$
4	1	0	1	1	0	0	V_{DC}
5	1	0	0	1	0	1	0
6	1	0	0	1	0	1	0
7	1	0	0	0	1	1	$-V_{DC}$
8	0	1	0	0	1	1	$-2V_{DC}$
9	1	0	0	0	1	1	$-V_{DC}$
10	1	0	1	0	1	0	0

The output period is divided by ten equal sections. The output voltage waveform of proposed 5–level inverter based on this switching algorithm is illustrated in Figure 3. The two DC voltage sources magnitudes are equal (12V) and output frequency has been set to 50 Hz. The output voltage waveform and its harmonic spectrum are shown in Figure 3. It is clear that the 5^{th} harmonic of output voltage is eliminated. This topology can generate 5-level output voltage in both symmetrical and asymmetrical cases. There is not any bidirectional switches in this topology for the 5-level output voltage generation that is contrast of this paper. The Total Harmonic Distortion (THD) of output voltage is 42.8% which is good result for 5-level multilevel inverter

considering the simple implementation and low switching frequency.

By expanding the proposed 5-level inverter to the 7-level, proposed 7-level inverter is displayed in Figure 4. This inverter contains six unidirectional and one bidirectional power switches with three DC voltage sources. All three DC voltage sources magnitude are the same. According to the proposed 7-level inverter configuration if power switches of DC side i.e. ((S1,S2), (S1,S3), (S2,S3)) turn-on simultaneously; the DC voltage sources corresponding to these switches will be short-circuited. Therefore, the simultaneous turn-on of mentioned switches should be avoided.

Table 2 shows the switching patern of proposed 7-level inverter. The output voltage waveform and harmonic spectrum of proposed 7-level inverter are illustrated in Figure 5. According to the Figure 5 it demonstrates the 5th harmonic of output voltage is eliminated like proposed 5-level inverter. Consequently, it can be show that in proposed topology the 5th output voltage harmonic in n-level inverter has been eliminated. The THD of output voltage of 7-level inverter is 25.5% which is almost half of the 5-level inverter. The output volatge THD will be decreased due to increasing the number of levels.

The number of output voltage steps, IGBTs, unidirectional and bidirectional switches of proposed multilevel inverter can be expressed in Equation (1):

$$\begin{aligned} N_u &= 6 \\ N_B &= n-2 \\ N_{level} &= 2n+1 \\ N_{IGBT} &= 2n+2 \end{aligned} \quad (1)$$

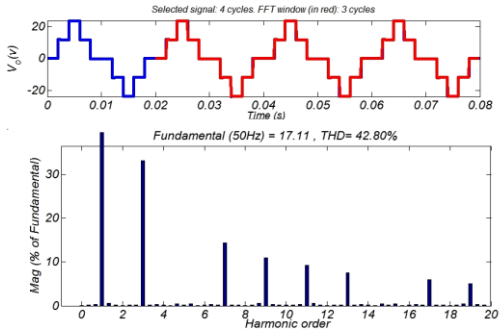

Figure 3. Output volatge waveform and harmonic spectrum of 5-level inverter

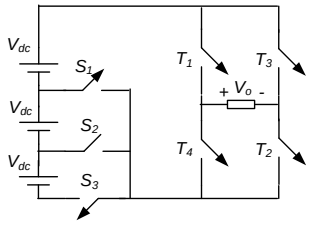

Figure 4. Proposed 7-level cascade inverter topology

TABLE 2. Switching states of proposed 7-level inverter

No.	S1	S2	S3	T1	T2	T3	T4	Vo
1	1	0	0	1	0	1	0	0
2	1	0	0	1	1	0	0	V_{DC}
3	0	1	0	1	1	0	0	$2V_{DC}$
4	0	0	1	1	1	0	0	$3V_{DC}$
5	0	0	1	1	1	0	0	$3V_{DC}$
6	0	1	0	1	1	0	0	$2V_{DC}$
7	1	0	0	1	1	0	0	V_{DC}
8	1	0	0	0	1	0	1	0
9	1	0	0	0	1	0	1	0
10	1	0	0	0	0	1	1	$-V_{DC}$
11	0	1	0	0	0	1	1	$-2V_{DC}$
12	0	0	1	0	0	1	1	$-3V_{DC}$
13	0	0	1	0	0	1	1	$-3V_{DC}$
14	0	1	0	0	0	1	1	$-2V_{DC}$
15	1	0	0	0	0	1	1	$-V_{DC}$
16	1	0	0	1	0	1	0	0

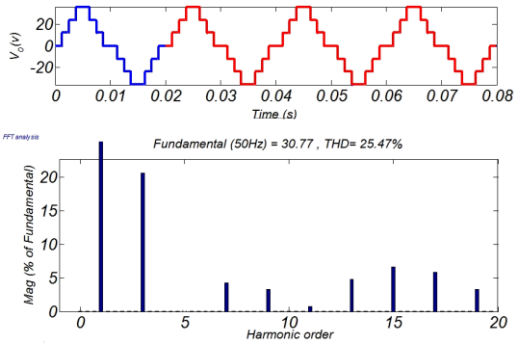

Figure 5. Output volatge waveform and harmonic spectrum of 7-level inverter

where, $N_u, N_B, N_{IGBT}, N_{level}, n$ are the number of unidirectional switches, bidirectional switches, IGBTs, output voltage levels and DC voltage sources number, respectively.

3. COMPARISON OF THE PROPOSED TOPOLOGY WITH RECENT TOPOLOGIES

In order to performance analysis of the proposed inverter, it should be compared advantages and disadvantages of proposed inverter with some recent types of multilevel inverters. It has been reported in literature [22], a new asymmetric cascade multilevel inverter using developed H-bridge type is presented.

This inverter needs a low number of DC voltage sources, IGBTs and withstanding voltage related to the other multilevel inverter. But the magnitudes of DC voltage sources should be unequal otherwise the number of output voltage levels will decrease. A new topology for cascade multilevel inverter is presented in literature [23]. This structure consist of series connection of basic unit blocks which are built with two both unidirectional and bidirectional power switches. This structure has some advantages for example: low number of IGBTs and driver circuits. The disadvantage of that is high withstanding voltage of power switches (twice of DC voltage sources). In addition, a new multi-level inverter topology was proposed [24]. This topology consist of single DC voltage source with two cascaded half-bridge (CHB) inverters which are connected to a 12-power switch three phase bridge. Related to comparable inverters, such as symmetrical CHB and hybrid multilevel inverters, the presented topology increase the number of output voltage levels and reduces number of the employed DC voltage source, power switches, gate driver circuits and installation area. The comparison of mentioned topologies and proposed inverter is listed in Table 3. In this table, VB is the blocking voltage. According to Table 3 information, the proposed inverter has lowest number of IGBTs except in literature [22]. In contrary, the cited literature [22] has a limitation in selection of DC sources values. The proposed inverter has the lowest blocking voltage except literature [24] but the number of proposed inverter IGBT is lower than the value reported in literature [24].

4. EXPERIMENTAL RESULTS

To verify the validity of proposed multilevel inverter the prototype of proposed 5-level inverter is implemented. This 5-level inverter which is shown in Figure 6 has been built in electrical machines research centre of Tafresh University. AVRATMEGA 32A microcontroller was used for switching gate signals generation and IRG4PH50UD is employed as MOSFET power electronic switches.

TABLE 3. Comparison of three recent topologies with proposed inverter

Converter type	[22]	[23]	[24]	Proposed inverter
N_u	7	7	7	7
N_{IGBT}	6	12	10	8
n	2 (the values of sources should be different)	6	3	3
V_B	$(V_{DC1}+V_{DC2})/2=(V_{DC}+2V_{DC})/2=1.5V_{DC}$	$2V_{DC}$	V_{DC}	V_{DC}

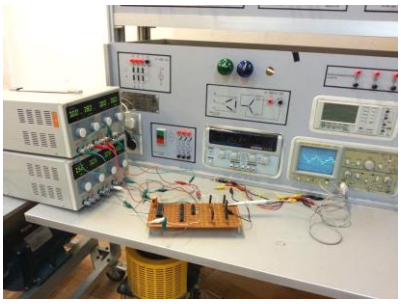

Figure 6. Experimental set up of proposed 5-level inverter

The proposed 5-level inverter is implemented by two equal isolated DC voltage sources VDC=12V and single phase resistive-inductive load (R=18.5 ohm, L=250 mH) which was connected to the output of inverter. The proposed switching pattern is employed to operate the proposed inverter at 50Hz as fundamental frequency. The experimental result of no load output voltage is illustrated in Figure 7.

The output volatge under RL load is shown in Figure 8. It demonstrates that the proposed inverter generate 5-level output voltage with no any spike under inductive load that is very good. This voltage was produced using only six unidirectional switches. The harmonic spectrum of measured output voltage under load is shown in Figure 9.

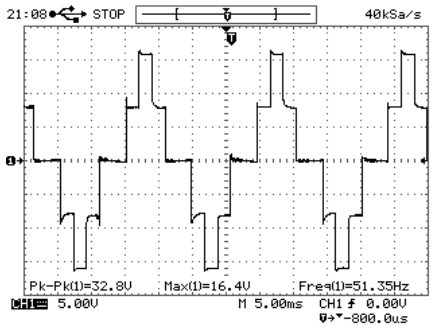

Figure 7. Measured volatge of proposed 5-level inverter at no load

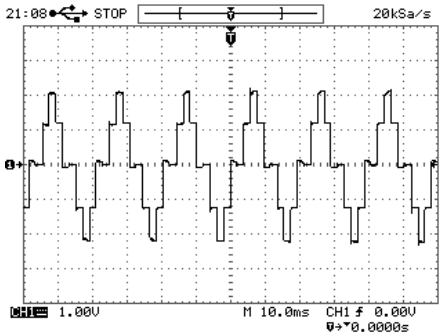

Figure 8. Measured volatge of proposed 5-level inverter under RL load

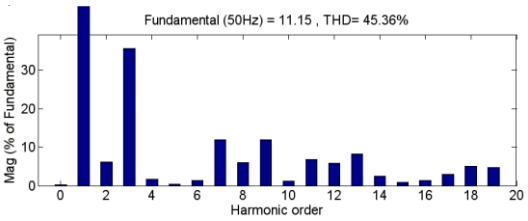

Figure 9. Harmonic spectrum of proposed 5-level output voltage under RL load

It is clear that the 5th harmonic was eliminated. In single phase 5 level cascade inverter this topology can be a best option for suitable number of power switches and simple implementation in hardware and software. The output current, the DC side switch current Is1 and DC source current I1 (which is shown in Figure 2) are illustrated in Figures 10, 11 and 12, respectively.

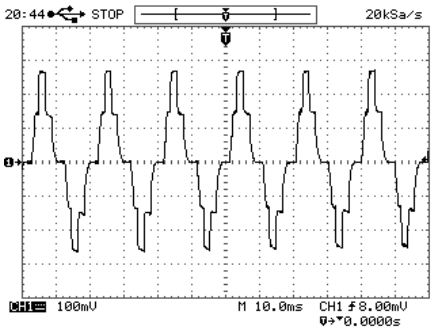

Figure 10. The proposed 5-level output current

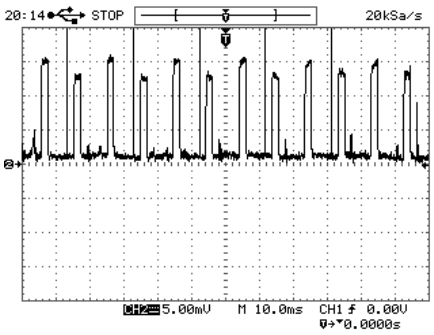

Figure 11. The DC side switch current I_{s1}

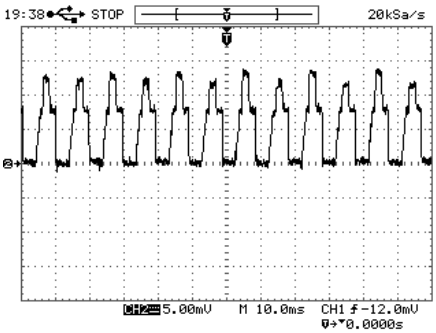

Figure 12. DC source current I_1

These results show that the short circuit of DC side switches was avoided and this topology could be well operate in RL load condition without any problem.

5. CONCLUSION

In this paper, a new single-phase symmetrical cascade multilevel inverter is proposed. Comparing with well-known and recent single phase multilevel inverter topologies, the proposed inverter has simple structure and reduced number of DC voltage source. The switching technique depends on the switching states of proposed inverter was successfully implemented. Furthermore, the possibility of the proposed inverter and the reliability of the implemented switching strategies were verified by the simulation and experimental results. In addition the 5th harmonic of output voltage was eliminated in proposed inverter.

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A New Single-phase Symmetrical Cascade Multilevel Inverter with Low Number of Power Switches

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چکیده

در این مقاله یک اینورتر تکفاز سری متقارن جدید ارائه شده است. در ساختار پیشنهادی از کلیدهای قدرت یک طرفه و دو طرفه با توجه به تعداد پله های ولتاژ خروجی استفاده شده است. تعداد کلیدهای قدرت و ولتاژ معکوس دو سر آنها در مقایسه با سایر ساختارها کاهش یافته است. ساختار ارائه شده قابلیت تبدیل به اینورتر n سطحی را دارد. در حالت متقارن هارمونیک پنجم ولتاژ خروجی حذف خواهد شد. بررسی کارایی طرح پیشنهادی در قالب یک اینورتر 5 سطحی شبیه سازی و پیاده سازی شده است.

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