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A Hysteretic Two-phase Supply Modulator for Envelope Tracking RF Power Amplifiers

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ABSTRACT

In this paper, a two-phase supply modulator suitable for envelope tracking power amplifier is presented. The designed supply modulator has the linear assisted switching architecture. Two-phase architecture is used in order to reduce the output switching ripples. The proposed architecture uses hysteretic control instead of pulse width modulation (PWM) which significantly reduces the circuit complexity. Moreover, fewer number of external R and C elements are used which leads to simpler architecture in comparison with reported two-phase PWM supply modulators. The proposed envelope modulator is evaluated with 0.18 µm CMOS technology. The results show that the designed two-phase modulator improves the output switching noise ripples and consequently enhances the overall linearity of the modulator compared to the single-phase case. The overall efficiency of the two-phase envelope modulator is 72.5% with 80 MHz switching frequency for a one-tone 5 MHz envelope signals at 27.4 dBm output power. The RMS output voltage ripples is less than 7.2 mV in a wide range of input signal amplitude while a SFDR of 50.4dB is achieved.

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1. INTRODUCTION

Envelope tracking RF power amplifier (PA) is a popular architecture for enhancing the linearity and efficiency of PAs in complex modulated signals, like OFDM. As shown in Figure 1, in this architecture the amplitude and phase of the signal are amplified in different paths. Envelope amplifier is the block that is used for modulating the amplitude of the signal at the drain of the main RF power amplifier. Different architectures have been proposed in the literature for implementation of the envelope modulator. Switch mode amplifiers [1-4], low dropout (LDO) regulators [5], series/parallel combination of linear and switch mode amplifiers [6-13] are among different architectures of the envelope modulator.

Linear amplifiers have wide bandwidth and low output ripple at the cost of lower efficiency. On the other hand, switching modulators have higher efficiency even at low output voltages but the output ripples are large in comparison to linear architectures which degrades the linearity.

One of the most popular architectures is the hybrid switching envelope modulator (HSEM). As shown in Figure 2, HSEM consists of the parallel combination of class-AB and class D power amplifiers. It provides a desirable combination of wide bandwidth, low output ripple, and high efficiency. In this architecture, the class D PA provides the average output current while the linear amplifier is mostly used for compensating the switching noise ripples. In order to maintain a high switching frequency for elimination of the switching noise, the bandwidth of the linear amplifier should be high enough that results in a higher power consumption of the linear stage.

On the other hand, the output impedance of the class-AB PA should be low at the switching frequency to reduce the switching noise ripples. There are some other challenges in the design of the HSEM to obtain a highly linear and efficient architecture which are addressed throughout the context. Higher switching frequency demands lower inductance at the cost of higher switching noise ripples in the output. On the other hand, the large

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signal behavior of the modulator is improved by reducing the output inductance. In this paper in order to improve both large signal behavior and output switching noise ripples, a new reconfigurable two-phase hysteretic parallel envelope modulator is proposed. The proposed architecture has several advantages compared to the one reported in [12].

One of its advantages is that hysteretic architecture does not need ramp signals, so there is no need for two-phase ramp generator circuit as in [12], that will result in significant circuit complexity reduction. Another advantage of the proposed architecture is that fewer number of external R and C elements are used in comparison with that of [12]. A wide bandwidth, low output impedance and low power consumption class AB PA is designed in this work, which reduces output switching noise ripples up to 100 MHz. With the help of this class AB PA the inductor needed for the proposed modulator becomes much lower than that of other two-phase modulators reported in [14, 15] while achieving better linearity performance.

The rest of this paper is organized as follows: In Section 2 a brief review and some of the challenges existing in the design of one-phase HSEM are discussed. The proposed two-phase architecture and its different building blocks are discussed in Section 3. In Section 4, simulation results of the architecture are given and conclusions are presented in the last part.

2. CIRCUIT DESIGN

2. 1. Conventional One-Phase HSEM A conventional one-phase envelope modulator consists of a linear and switching power amplifier as shown in Figure 2. In this architecture, a linear amplifier is used in a negative feedback loop to produce a replica of the input voltage while the switching class D power amplifier is used to generate the output current of the whole modulator. There are many challenges in the design of the envelope modulator which have been described in many previous reported works [8-12, 16]. A brief overview of some of these challenges will be explained in this section. The design of a wideband, low static power consumption linear amplifier is critical in this architecture.

The ripples of the class-D power amplifier at switching frequency passes through the parallel combination of the output impedance of the linear stage and the load impedance. So, in order to reduce the effect of these ripples on the output voltage, the output impedance of the linear stage should be low enough at this frequency. On the other hand, the bandwidth of the linear stage should be wide enough to cover the switching noise frequency. In the next section, the characteristic of the class AB PA, designed in this work, will be discussed.

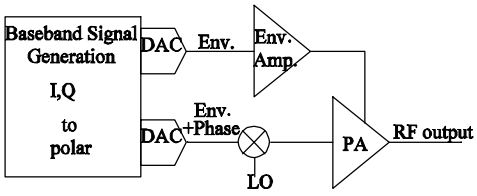


Figure 1. Block diagram of envelope tracking power amplifier

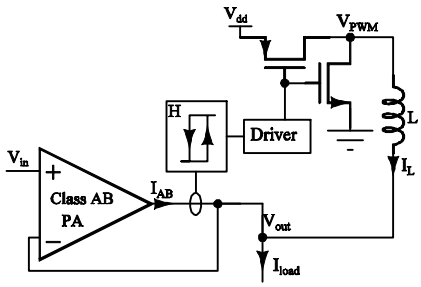


Figure 2. Block diagram of HSEM

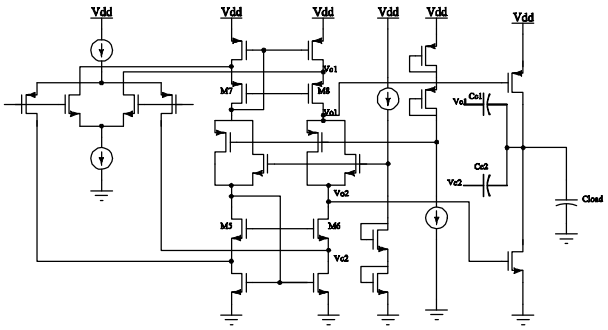


Figure 3. Class AB power amplifier architecture

2. 2. Class AB PA Different class AB PA topologies have been introduced in the literature to implement the linear amplifier stage of parallel hybrid supply modulators. Two-stage, three-stage and super source follower are different topologies that are considered in different works for class AB PA [8, 11, 12]. Although super source follower is popular for its low output impedance, its low bandwidth makes it less popular for high switching frequencies. It should be mentioned that in addition to higher power consumption, the design of three-stage class AB PAs are more complex than two-stage counterparts.

The class AB PA designed in this paper is based on the conventional two-stage class AB PA [17-19] as shown in Figure 3. This design is a modified version of the one reported in [16] to scale the input and output voltage swing of the amplifier. The specifications of the designed class AB PA are given in Table 1. As illustrated in the table, the output impedance of this amplifier is low enough to reduce the switching noise ripples with the frequency up to 100 MHz.

The amount of the output impedance is related to the DC output voltage. In order to show this relationship, the simulated output impedance is plotted in Figure 4 by sweeping the output DC voltage. The curves illustrated in this figure correspond to the closed loop output impedance of the class AB amplifier. This output impedance can be expressed as follows:

$$Z_{out\_CL} = \frac{Z_{out\_OL}(s)}{1 + A(s)\beta} \quad (1)$$

where, $Z_{out\_OL}(s)$ is the output impedance of the class-AB biased amplifier and $A(s)$ is the frequency response of the OTA. Since $Z_{out\_OL}(s)$ and β are nearly constant values, we can say that Z_{out_CL} is inversely proportional to $A(s)$. If the bandwidth and DC gain of $A(s)$ is increased, the output impedance will be low in a large range of frequencies below 100MHz. This low output impedance is beneficial for reducing the output switching noise ripples.

Figure 5 shows the output voltage of class AB PA tracking a 10 MHz square wave signal. The output voltage settles in around 12 ns for a 0.5-2.7 V pulse signal in both rising and falling edges.

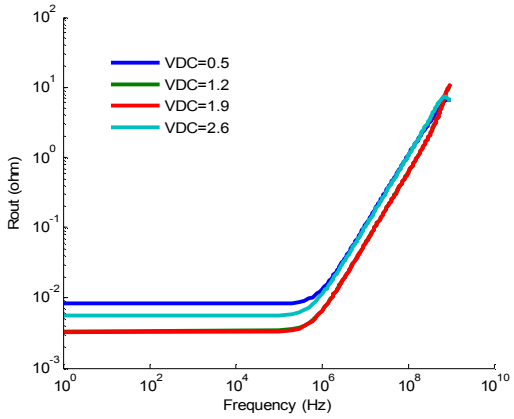


Figure 4. Simulated output impedance of class AB PA versus frequency for different DC output voltages

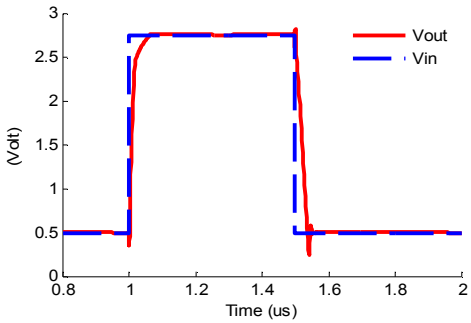


Figure 5. Class AB PA tracking a 10 MHz (0.5-2.7 V) square wave

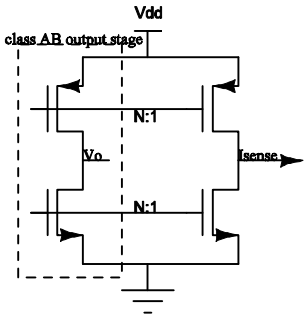


Figure 6. Current Sense Circuit

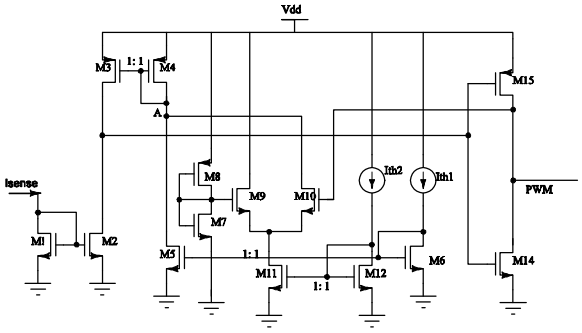


Figure 7. Current hysteretic comparator

TABLE 1. Characteristics of the Designed Class AB Power Amplifier in [16].

Parameter	Value
Technology	0.18umCMOS (thick oxide)
Supply	3.3 V
DC gain	82
Phase Margin	55.8
UGBW	985 MHz
Output impedance (For more than 50dB SFDR)	0.147 @ 25MHz 0.646 @ 100MHz
Quiescent Current	32 mA
SR+	2.59e9
SR-	2.34e9

2. 3. Current Sense and Hysteretic Current Comparator The sense and control circuit of the hysteretic comparator is designed based on the one reported in [11] and shown in Figure 6 and 7. I_{sense} is obtained from the circuit shown in Figure 6. As shown in this figure, the transistors used for current sensing are scaled by the ratio of N:1 with respect to the class-AB output stage transistors. This scaling is required in order to prevent the current sensing circuit from affecting the class-AB PA characteristics. The sensed current will be fed to the second hysteretic circuit H2 to produce the *PWM* signal in the block diagram. The resulting square wave signal will be fed to the driver circuit in one-phase

modulator while in two-phase architecture it is served as a control signal to produce two $PWM_{1,2}$ signals.

The switching frequency of this architecture depends on class D output filter inductance and the thresholds of hysteresis circuit. It should be mentioned that in the hybrid architecture, if the switching frequency becomes larger than the signal bandwidth, most of the load current will be provided by the class D PA and the class-AB PA will be used mainly for compensating the switching noise ripples. Otherwise the class D PA works as a constant current source in parallel with the class-AB PA. In this mode of HSEM operation, the switching frequency is independent of the circuit parameters and will be equal to the input signal frequency.

As illustrated in Figure 7, the I_{sense} current will be mirrored via M1-M4 transistors to node A. At this node I_{sense} will be compared with I_{th1} or $I_{th1}+I_{th2}$ depending on the M10 transistor state which will be turned on during the rising edge of the output voltage. So, in this architecture I_{th2} determines the hysteresis bandwidth. One of the advantages of this architecture is the elimination of R_{sense} that causes extra power dissipation.

3. THE PROPOSED ARCHITECTURE

3. 1. Two-phase Hysteretic Parallel Modulator

In order to reduce the output voltage ripples a new hysteretic envelope modulator is proposed. The block diagram of the proposed architecture which is based on the combination of the parallel hybrid modulator and hysteretic two-phase switching amplifier is shown in Figure 8. Two integrator circuits are used to convert the PWM voltages V_{oD1} and V_{oD2} to triangular like voltage waveforms that are similar to the current of inductors. The integrator circuits are shown in Figure 9. In order to increase the average output voltage of the integrator, R1 is connected to the supply voltage instead of ground.

A hysteretic architecture composed of a conventional hysteretic architecture with an extra preamplifier circuit is designed for H1 and shown in Figure 10. The designed hysteretic architecture is used for generating the control signal V_{sense} based on the difference between $v_{oD1,2int}$ voltages. The extra preamplifier circuit is used to decrease the zone of the hysteresis in order to support very small differences. The positive and negative trip point of the hysteretic voltage comparator is expressed by:

$$V_{TRP} = \frac{g_{m3,4}}{g_{m1,2}} \sqrt{\frac{2I_{BIAS}}{\mu C_{ox}\left(\frac{W}{L}\right)_{5,7}}} \frac{\sqrt{\alpha}-1}{\sqrt{\alpha}+1} \quad (2)$$

where, I_{BIAS} is the DC current of M17 transistor and α can be expressed with the following equation:

$$\alpha = \frac{(W/L)_{9,10}}{(W/L)_{8,11}} \quad (3)$$

Voltage transfer curve of the designed hysteresis comparator is shown in Figure 11.

3. 2. Reconfigurable IL Sharing Control Circuit

In a two-phase switching modulator, a current sharing circuit is required to prevent the current from changing to negative values in one of the phases. This is because negative current will degrade the efficiency and overall performance of the architecture.

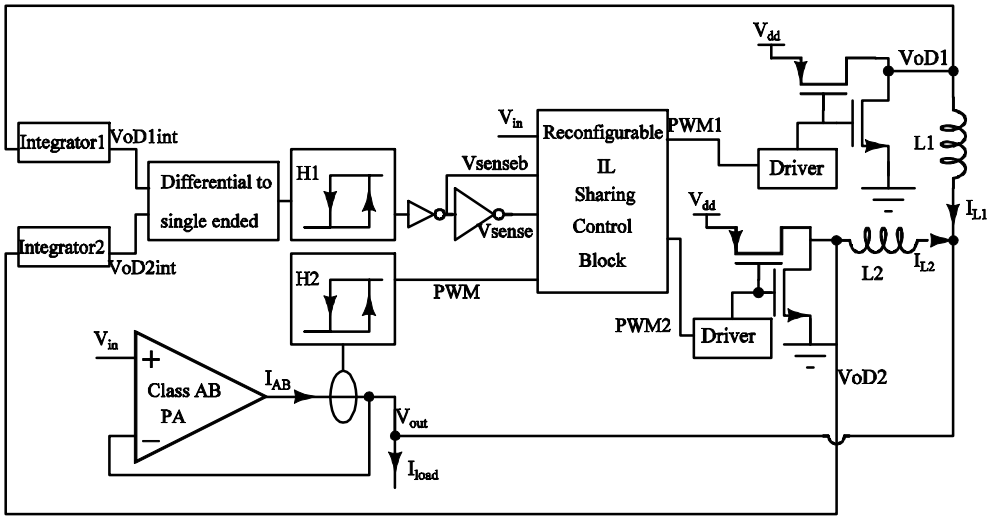


Figure 8. Block diagram of the proposed hysteretic two-phase envelope modulator.

In this paper, a new reconfigurable current sharing is proposed as depicted in Figure 12. In this figure, V_{in} , V_{sense}, V_{senseb} and PWM are input control signals of the current sharing control block. V_{in} is used to generate an extra control signal to improve the large signal behavior of the design. When V_{in} is less than the half of the supply voltage, the circuit will operate as a two-phase converter, otherwise the two-phase input voltages become equal and perform like two parallel switching amplifier. The operation can be summarized as the flowchart shown in Figure 13.

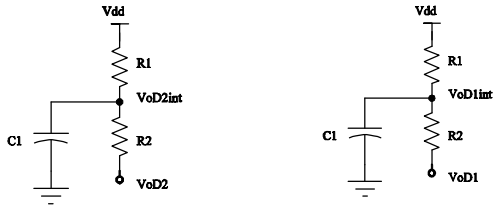


Figure 9. Integrator circuits used for integrating the switching voltages

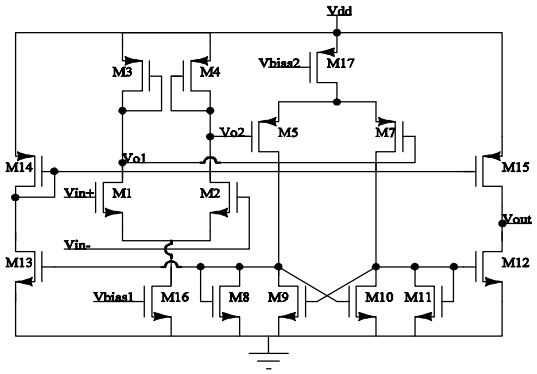


Figure 10. Voltage hysteretic circuit used for block H1

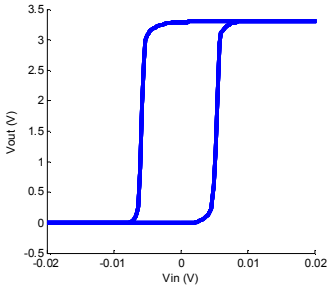


Figure 11. Voltage transfer curve of the designed hysteresis comparator

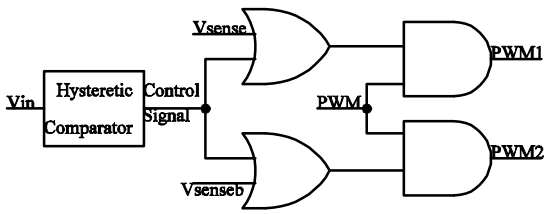


Figure 12. Reconfigurable IL sharing control block

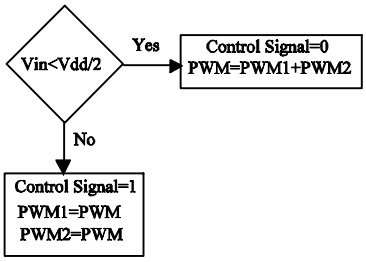


Figure 13. Flowchart of reconfigurable IL sharing control block operation principle

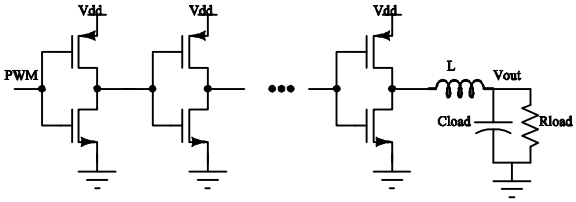


Figure 14. Class D power amplifier with driver stages

In the parallel mode of operation, the equivalent inductance is half of the inductance of each phase. In this mode of operation, the large signal behavior of the architecture will be improved with regards to both single phase architecture and two-phase mode of operation. The reason for this improvement is lower equivalent inductance compared to two-phase mode of operation and larger switching stage current with regard to single phase architecture. As illustrated in Figure 8, the square wave signal V_{sense} is generated based on the difference between the currents of two-phases. For simulation, the equivalent CMOS circuits of digital AND and OR blocks are replaced. As it will be discussed in the next section, the width of the transistors in these blocks and class D driver and power stage will be determined in accordance to logical effort method [20] in order to reduce the gate delays.

3. 3. Class D and Driver Stages As discussed in the previous sections, in order to reduce delay, the driver stage of class D power amplifier should be designed with the logical effort method. In this work (see Figure 14) a conventional class D architecture with one-phase driver is used in each phase. The size of class D transistors is optimized to reduce the power loss of this PA. Assuming that the total power loss of the class D PA is the sum of the conduction loss and switching loss, the total power dissipation can be written as follows:

$$P_d = P_{cond} + P_{SW} \quad (4)$$

where, P_{cond} and P_{SW} are conduction loss and switching power loss of the class D PA, respectively. They can be computed by the following equations:

$$P_{cond} = R_{eq} I^2 = I^2 \left[DR_{onP} + (1-D) R_{onN} \right] \quad (5)$$

$$P_{SW} = C_{eq} f V_{dd}^{\ 2} \quad (6)$$

where, C_{eq} is the equivalent capacitance seen at the output, I is the average output current and R_{onN} and R_{onP} are the resistance of the NMOS and PMOS transistors in the class D PA, respectively. If a minimum channel length is assumed, the product of P_{cond} and P_{SW} is independent of the transistor sizing. So, the problem is minimizing the sum of two terms which has the constant product when the only varying parameter is the width of the transistors. The answer is the geometric mean of the two terms as follows:

$$P_{cond} = P_{SW} = V_{dd} I \sqrt{f R_{eq} C_{eq}} \quad (7)$$

Therefore, the minimum loss is given by:

$$P_{d\min} = 2 V_{dd} I \sqrt{f R_{eq} C_{eq}} \quad (8)$$

After the class D transistors size is determined, the number of driver stages and stage ratio should be computed based on the ratio of C_{eq} and the output capacitance of the current sense circuit. The size of the PMOS transistors should be chosen two or three times larger than that of the NMOS transistors to have the same on state resistance. The output filter of the class D PA determines the bandwidth of the class D PA. The larger inductance corresponds to the lower switching frequency but at the cost of lower class D bandwidth, higher difficulty for on-chip implementation and better large signal tracking ability.

4. SIMULATION RESULTS

The proposed two-phase supply modulator is simulated with 0.18 µm CMOS process in which the thick oxide devices are chosen for high voltage operation. For simulation a 5Ω and 10Ω resistive load were used individually for modeling the main RF power amplifier. Time domain current waveforms of class D, class AB and load resistance are shown in Figure 15 for both single-phase and two-phase modulators. As it is shown, the peak to peak voltage ripple of the output voltage has been improved significantly in comparison to single phase modulator. Root mean square (RMS) and peak to peak output voltage ripples versus input voltage level for both two-phase and single-phase architectures are plotted in Figures 16 a and b, respectively. Based on these figures the output ripple of the two-phase modulator is lower than that of single-phase mode in the whole input voltage range. In order to represent the ability of the architectures to attenuate the switching noise ripples, the simulated power spectrum of the proposed modulator is plotted in Figure 17.

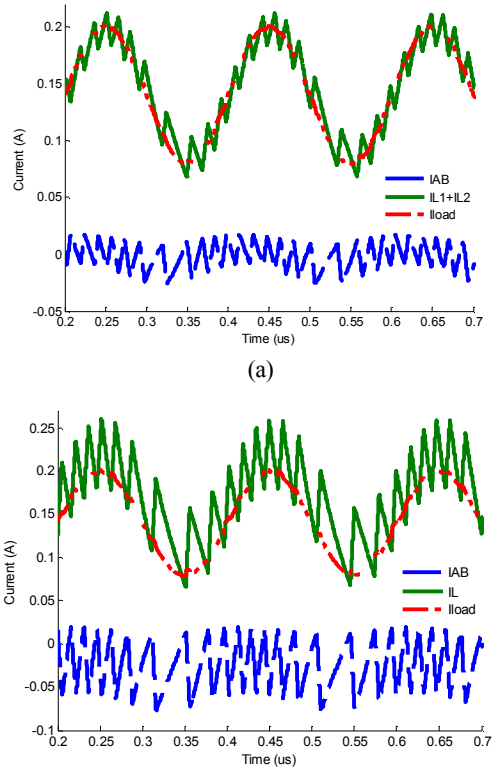


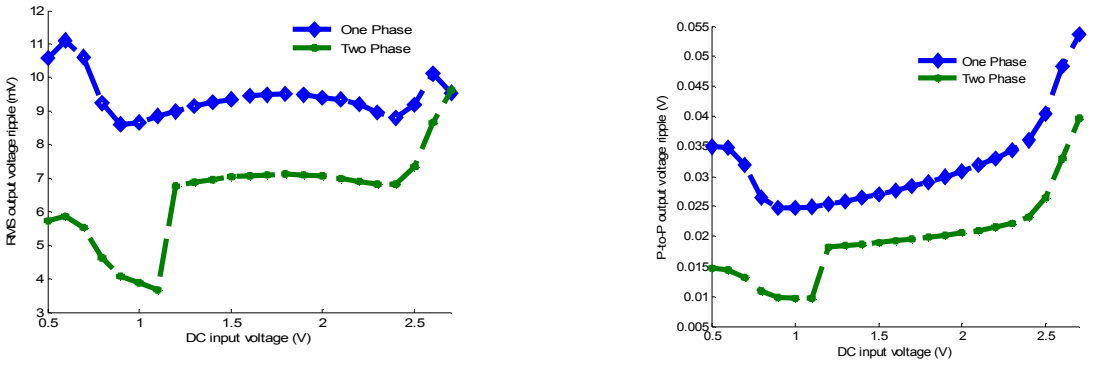
Figure 15. Time domain waveforms of class D, class AB and load resistance output current a) two-phase b) single phase

The simulated spurious tones of the two-phase modulator are less than -50.4 dBc which is lower than conventional one-phase modulators.

The simulated static power efficiency of both one-phase and two-phase architectures are shown in Figure 18. As illustrated in the figure, the maximum DC efficiency of the modulator is 89% at maximum output power of 33 dBm. To compare the dynamic efficiency of both two-phase and single-phase envelope modulator architectures, a one tone signal is applied. Figure 19 shows the simulated dynamic efficiency of both architectures versus input signal bandwidth.

To show the performance, the simulation results of the proposed two-phase architecture and equivalent one-phase modulator are compared with other previous works in Table 2. As illustrated in the table two 400 nH output inductors are used which are lower than other reported two-phase designs with approximately the same output power. Lower inductance will improve the large signal response of the modulator which results in lower output ripples in transitions and consequently better linearity performance. However, it leads to higher switching frequency and therefore higher switching loss, but because of lower ripples, the power consumption of the linear amplifier is improved. Thanks to the low output

impedance, high bandwidth and current driving capability of the designed class AB PA, the modulator is able to have less than 7.2 mVrms ripple and 50.4 dBc SFDR at 27.4 dBm output power. The modulator is tested with 5 MHz WiMAX signal with 6dB PAPR at an average output power of 27 dBm. The simulated input and output waveforms are plotted in Figure 20. The maximum average efficiency in this case is 70% with 5Ω load.



(a) (b)

Figure 16. a) RMS of output voltage ripple as a function of DC input voltage, b) Peak to peak of output voltage ripple as a function of DC input voltage

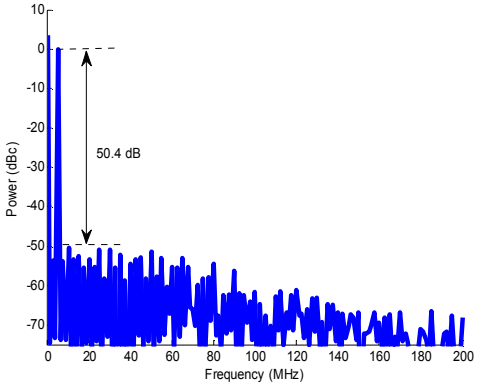


Figure 17. Power spectrum of the output voltage of two-phase modulator for 5 MHz signal at Pout=27.4 dBm

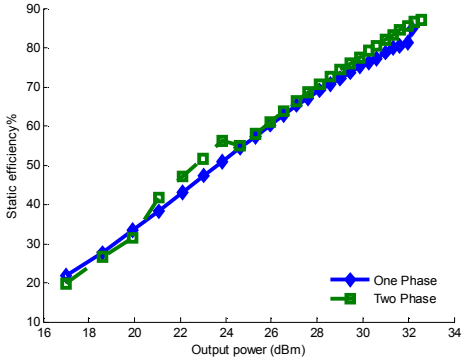


Figure 18. Simulated static efficiency of the envelope modulator versus DC output power

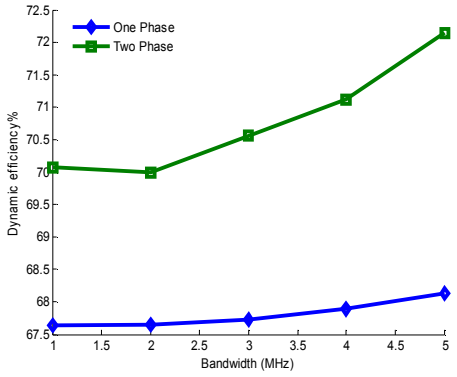


Figure 19. Simulated dynamic efficiency of the envelope modulator versus input signal bandwidth at Pout=27.4 dBm

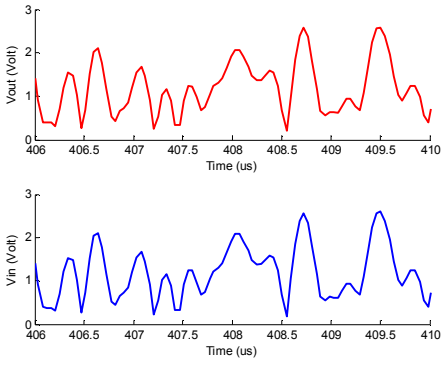


Figure 20. Simulated 5 MHz WiMAX time-domain waveforms of the proposed digital supply modulator.

TABLE 2. Comparison of envelope modulators

Ref.	Tech. (nm)	Supply voltage	Signal	Switching Freq .(MHz)	Maximum Average Efficiency (Load)	Vrms (ripple)	SFDR (dBc)	Inductor Size (µH)	Average output power (dBm)
[10]	65	1.2	20 MHz	118	40 % (5.3 Ω)	4.3 mV	54.24	0.08	12
[11]	350	3.5	2 MHz RSW	10	60% (3.8 Ω)	40 mVp_p	43	Two 0.5	23
[13]	180	5.5	20 MHz LTE	NM	83% (5.2 Ω)	NM	38.5	1/0.3	28.3
[14]	180	5.5	10 MHz LTE	5.64/15.1	80%	NM	34	1.1/2.2	27
This work (single phase)	180	3.3	Single tone 5 MHz	80	62% (10 Ω)	5.5 mV	52	0.4	23
					68.2% (5 Ω)	10 mV	49.3	0.15	27.4
This work (two-phase)	180	3.3	Single tone 5 MHz	80	72.5% (5 Ω)	7.2mV	50.4	Two 0.4	27.4
This work (two-phase)	180	3.3	5 MHz WiMAX	80	70% (5 Ω)	---	50.4	Two 0.4	27.0

5. CONCLUSIONS

In this paper, a two-phase supply modulator suitable for envelope tracking power amplifiers is proposed. The modulator has fewer numbers of external R and C elements and simpler architecture in comparison with PWM two-phase modulators. The output voltage ripples and consequently the linearity of the output voltage of the architecture has been improved compared to the single-phase architecture. Although the complexity of the two- phase modulator is more than that of the single-phase architecture, the efficiency is improved up to about 4 percent. These stems from the lower output voltage ripples, and consequently lower linear amplifier power consumption. The inductor size of the proposed modulator is lower than that of previously reported modulators. The lower inductance although increases the switching frequency, it improves the large signal transition response of the modulator, resulting in a better linearity performance. The class AB PA designed in this paper has a two-stage folded cascode architecture which has the ability to allow the switching ripples to be as low as 7.2mVrms at the switching frequency of 80 MHz.

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A Hysteretic Two-phase Supply Modulator for Envelope Tracking RF Power Amplifiers

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چکیده

در این مقاله یک مدولاتور منبع تغذیه دو فاز برای استفاده در ساختارهای تقویت کننده دنبال کننده پوش، ارائه شده است. ساختار دو فاز، به منظور کاهش ریپل خروجی مورد استفاده قرار گرفته است. ساختار پیشنهاد شده از کنترل کننده هیسترزیس به جای کنترل PWM استفاده کرده است که پیچیدگی مدار را تا حد زیادی کاهش می دهد. علاوه بر این تعداد کمتری از المانهای R و C نیز استفاده شده است که ساختار ساده تری نسبت به ساختارهای دو فاز PWM که تا کنون پیشنهاد شده اند، نتیجه می شود. مدولاتور پوش پیشنهاد شده با تکنولوژی ۰/۱۸ میکرومتر CMOS ارزیابی شد. نتایج نشان می دهد که مدولاتور دو فاز پیشنهاد شده ریپل های ناشی از فرکانس سوئیچینگ را کاهش و در نتیجه خطینگی کل مدولاتور را نسبت به ساختار تک فاز افزایش می دهد. راندمان کل مولاتور پوش حدود ۷۲/۵٪ برای سیگنال تک تون ۵ مگاهرتز در حضور ۸۰ مگاهرتز فرکانس سوئیچینگ و در متوسط توان خروجی ۲۷/٤ dBm می باشد. در محدوده وسیعی از دامنه سیگنال ورودی میزان RMS ریپل ولتاژ خروجی کمتر از ۷/۲ mV است و SFDR حدود ۵۰/٤ dB می باشد.

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