

# CHARACTERISTICS OF P-TYPE AlAs/GaAs BRAGG MIRRORS GROWN BY MBE ON (100) AND (311)A ORIENTED SUBSTRATES

M. K. Moravvej-Farshi

Department of Electrical Engineering  
Tarbiat Modarres University  
Tehran, Iran

**Abstract** P-type GaAs/AlAs distributed Bragg mirrors have been grown using molecular beam epitaxy on (100) and (311)A GaAs substrates in a similar conditions. A comparison of I-V measurements shows that the resistance of the ungraded mirrors grown on the (311)A substrate is 35 times lower than those grown on the (100) substrate with similar structure. The effective barrier heights for both (311)A and (100) barriers were extracted from their Arrhenius behaviour, obtained from their current temperature dependence. The calculated values for (311)A and (100) effective barrier heights are 141 meV and 341 meV, respectively. The room temperature values of the specific differential resistance for both devices around zero bias [i.e.  $R_C = (dV/dJ)|_{V=0}$ ] were calculated. The approximated values for (311)A and (100) devices are  $80 \text{ m}\Omega\text{-cm}^2$  and  $2.8\Omega\text{-cm}^2$  respectively.

**Key Words** AlAs, GaAs, DBR, Substrate Orientation, VCSEL

**چکیده** آینه های براگ (Bragg)، با رشد لایه های نازک و متوالی AlAs و GaAs نوع p روی پولکهای GaAs با جهت های (100)، (311)A، به روش اشعه ملکولی (MBE) در شرایط یکسان شناخته شده است. مقایسه مشخصه های I-V این دو نوع ساختار نشان می دهد که مقاومت آینه های رشد داده شده بر روی پولک های (311)A، 35 مرتبه از مقاومت آینه های مشابه رشد داده شده بر روی پولک های (100) کوچکتر است. ارتفاع موثر سد پتانسیل، برای هر دو ساختار، با استفاده از اندازه گیری بستگی جریان الکتریکی آنها به دما، به دست آمده است. مقادیر محاسبه شده ارتفاع موثر سد پتانسیل در جهت های A (311) و (100) به ترتیب عبارت است از 141 meV، 341 meV. اندازه های مقاومت ویژه تفاضلی هر دو نوع ساختار در حوالی بایاس صفر [یعنی،  $R_C = (dV/dJ)|_{V=0}$ ] محاسبه شده است. مقادیر تقریبی آنها به ترتیب برای آینه های (311)A و (100) عبارت است از  $80 \text{ m}\Omega\text{-cm}^2$  و  $2.8 \Omega\text{-cm}^2$ .

## INTRODUCTION

The numerous unique properties of vertical cavity surface emitting lasers (VCSELs) have made them the center of the attention. Figure 1 illustrates schematic diagrams of two different VCSEL structures. Depending on the designed structure, the output light may either be emitted from the bottom surface via the n-type mirrors [Figure 1(a)] or from the top surface through the p-type mirrors of the VCSEL [Figure 1(b)]. In a typical VCSEL, current is injected into the active region through the mirrors normally formed by epitaxially grown distributed

Bragg reflectors (DBR) stacks.

There are several developed commercial applications in which VCSELs could be used. As arrays they could serve as print heads in laser printers, or as multi-track readout heads from optical data storage media. However, the high resistance of VCSEL's p-type AlAs/GaAs DBR mirrors limits the device efficiency and has been the major obstacle in preventing VCSELs becoming an integrated part of many other practical optical systems [1]. The higher resistance of the p-type AlAs/GaAs mirrors is attributed to the heavier effective mass for the holes than to the electrons in both materials, and also to

the solubility limit of Be in AlAs. Be is a common p-type dopant in MBE grown  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layers [2]. Low resistance mirrors recently have been fabricated, either by electrically by-passing the VCSEL's top p-type Bragg mirrors deposited after formation of the top ohmic contact [3] or by using Be-doped piecewise linearly graded (Al, Ga)As Bragg mirrors [4].

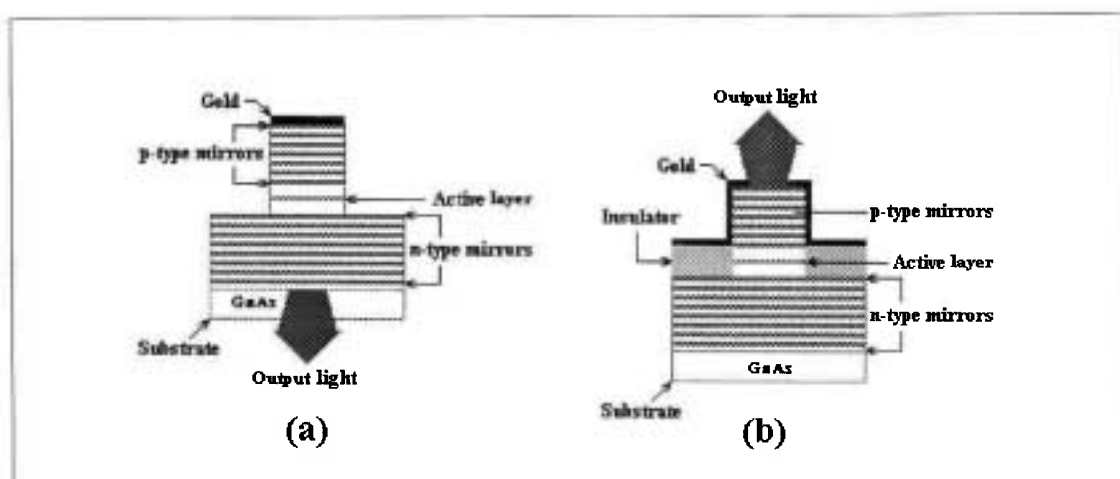
The importance of the DBR resistance and the possibility of producing lower threshold currents when lasers are grown on the high order index GaAs substrates rather than conventional (100) oriented substrates is well known [5]. Therefore, in this paper the influence of the substrate orientation on the resistance of the ungraded p-type AlAs/GaAs Bragg mirrors grown by molecular beam epitaxy (MBE) has been examined, and the effective heights of the respective barriers have been compared. The p-type mirrors grown on a (311)A oriented substrate demonstrated a significantly lower resistance and considerably smaller effective barrier height than those of p-type mirrors grown on a (100) oriented substrate.

### ISOTYPE HETEROSTRUCTURES UNDER BIAS

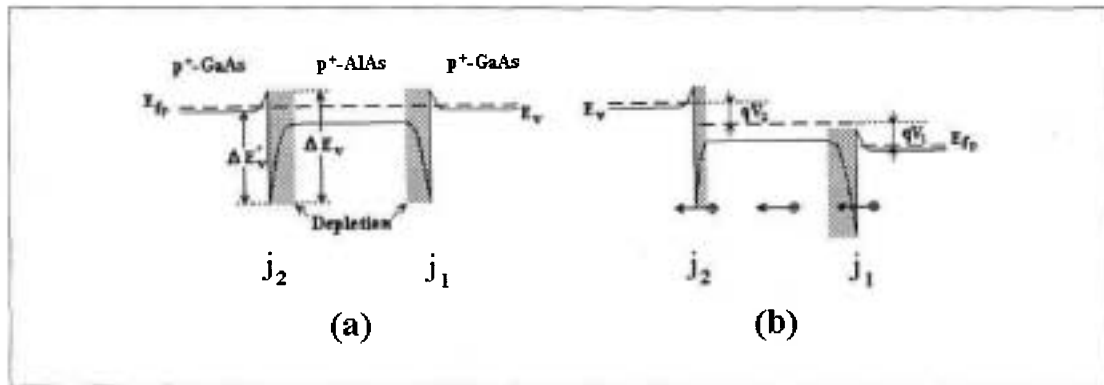
As shown in Figure 1, the structure of a typical

VCSEL is so doped to form a p-i-n diode. The p- and n-type DBR stacks are highly doped. Therefore, the fermi levels in these regions lie close to the respective band edges and band bendings occur in the vicinity of the heterointerfaces. Schematic diagrams of valence band edge for one pair of such heterointerfaces in a p<sup>+</sup>-doped GaAs/AlAs stack are illustrated in Figure 2. While the diagram shown in Figure 2(a) represents the valence band edge under thermal equilibrium condition, Figure 2(b) shows the same valence band edge under a biased condition. As it can be seen from Figure 2(a), after formation of the heterojunction, holes are depleted from the wide bandgap material (i.e. AlAs) into the narrow bandgap material (i.e. GaAs) and accumulate there.

When  $\Delta V$  is the potential dropped across the pair of heterointerface, shown in Figure 2, junctions  $j_1$  and  $j_2$  are subject to potential drops of  $V_1$  and  $V_2$ , respectively, where  $\Delta V = V_1 + V_2$ . Note that in such a structure if  $j_1$  is a reverse biased junction,  $j_2$  will be under a forward bias. As long as the depletion width near  $j_1$  is sufficiently narrow, the barrier at  $j_1$  will show a very small resistance toward the carrier flow, and holes tunnel through the potential spike, from GaAs into AlAs. Hence, the "thermionic field emission" is the dominant process



**Figure 1.** Schematic diagrams of two VCSEL structures: (a) emitting from the bottom surface; (b) emitting from the top surface.



**Figure 2.** A schematic diagram of valence band edge for one pair of highly doped p-type AlAs/GaAs hetero-interface under: (a) thermal equilibrium condition; (b) an arbitrary biased situation. The symbol  $\oplus$  indicates the direction of hole flow.

in the carrier flow across  $j_1$ . Otherwise, the structure will have a large electrical resistance. Junction  $j_2$ , however, presents no barrier to holes travelling, from AlAs toward GaAs, under the forward bias. That is, the "thermionic emission" is the dominant process in the carrier flow across  $j_2$  and thus,  $j_2$  offers a very low resistance to the holes current. Therefore, in order to achieve a low series resistance in a VCSEL, it is necessary to ensure a significant tunnelling probability through the reverse biased junctions in the DBR mirrors. This is done by doping the layers to a sufficient level to give narrow depletion regions.

### DEVICE FABRICATION

Samples were grown, simultaneously, by MBE on semi-insulating GaAs substrates with orientations (100) and (311)A. The growth temperature and As/Ga equivalent flux ratio were 630°C and 12:1 respectively. The epitaxial structure consisted of a 1 $\mu$ m GaAs buffer layer followed by 21 periods of quarter-wavelength AlAs (687Å)/GaAs (576Å) Bragg stack covered by a 1 $\mu$ m GaAs capping layer. All layers were doped with Be to the nominal level of  $2 \times 10^{18} \text{ cm}^{-3}$ .

First, in order to compare the reflectance of

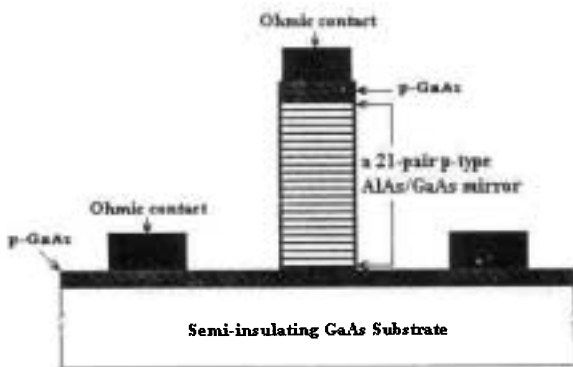
the Bragg reflectors, the top GaAs buffer layer and the first AlAs layer have been etched, from the test samples, selectively using 5NH<sub>4</sub>OH: 95H<sub>2</sub>O<sub>2</sub> and HF respectively.

Then, the epitaxial layers were processed into mesas of various radii by means of conventional photolithography and wet etching. The etchant used was a 1:10 mixture of H<sub>3</sub>PO<sub>4</sub>: H<sub>2</sub>O<sub>2</sub>. The etch rate depended on the substrate orientation and for the (311)A and (100) oriented substrates, it was 4.0  $\mu\text{m}/\text{min}$ , and 4.5  $\mu\text{m}/\text{min}$  respectively. The etching processes were carefully controlled so that the device lower contact could be made to the top of p-type GaAs buffer layer. The ohmic contacts consisted of 10nm Au, 5nm Zn, 200 nm Au and were annealed for 30 seconds at 310°C. A schematic representation of the device structure is illustrated in Figure 3.

### RESULTS AND DISCUSSIONS

First, the reflectances of both Bragg stacks were measured. The comparison showed a quite similar reflectance for mirrors grown on both (311)A and (100) oriented substrates.

Figure 4 illustrates the typical room temperature I-V characteristics of the Bragg mirrors grown on the

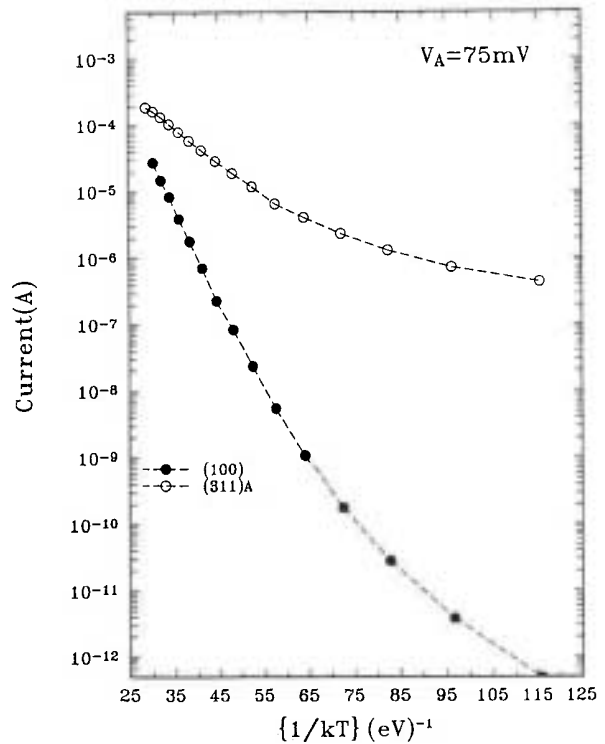


**Figure 3.** A schematic representation of the device structure, consisting of a 21-pair AlAs/GaAs DBR sandwiched between two 1- $\mu\text{m}$ -GaAs layers grown on a semi-insulating GaAs substrate.

(100) and (311)A substrates. The forward and reverse I-V characteristics for (100) sample are shown by solid line and open squares, respectively, whereas for (311)A sample these are illustrated by the dashed line and open circles. It is worth noting that the I-V characteristics for both the (100) and (311)A devices are symmetrical. This result was expected because of the symmetry of the devices.

It can be seen that the device manufactured from the (311)A wafer has a current which is nearly two orders of magnitude greater than the equivalent device grown on the (100) plane for any given voltage within the measured range, at the room temperature. This indicates that the resistance of the ungraded Bragg reflectors grown on the (311)A oriented substrate is lower than that of the similar Bragg reflectors grown on the (100) oriented substrate. The data shown in Figure 4, was obtained from devices whose mesas had nominal diameters of 100  $\mu\text{m}$  and with ohmic contacts of 90  $\mu\text{m}$  diameters. Results from other devices with a range of mesa sizes are in broad agreement with those presented in Figure 4.

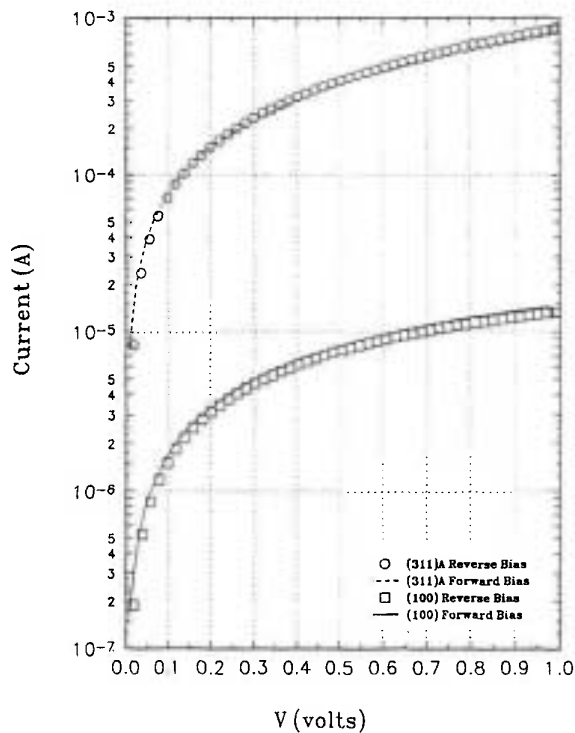
Measurements of the device characteristics, at various temperatures, were performed over the range of 100-400°K. The Arrhenius behaviour of both (100) and (311)A oriented devices at 75 mV is illustrated in Figure 5. The smaller slopes of the



**Figure 4.** Comparison of the I-V characteristics of the devices of Figure 3 grown on the (100) and (311)A oriented substrates. The forward and reverse I-V characteristics for (100) sample are shown by a solid line and open squares, respectively, whereas for (311) A sample these are illustrated by the dashed line and open circles. The device diameter was nominally 100  $\mu\text{m}$  with a 90  $\mu\text{m}$  diameter ohmic contact.

(311)A plots indicate that the effective height for the barrier at the interface of an AlAs/GaAs structure grown on the (311)A substrate is smaller than that of the similar structure grown on the (100) wafer. Fitting the data, using the "thermionic field emission" approximation [6], corresponding values of the effective barrier heights were approximated to be 341 meV for (100) and 141 meV for (311)A, respectively.

To extract values for the effective barrier heights around zero bias, the specific differential resistances of both devices at various temperatures around zero bias {i.e.,  $R_c = (dV/dJ)|_{V=0}$ } [7] were calculated. Figure 6 illustrates this behaviour for both devices. The dark circles connected with a solid line represent the calculated values of the specific differential resistance

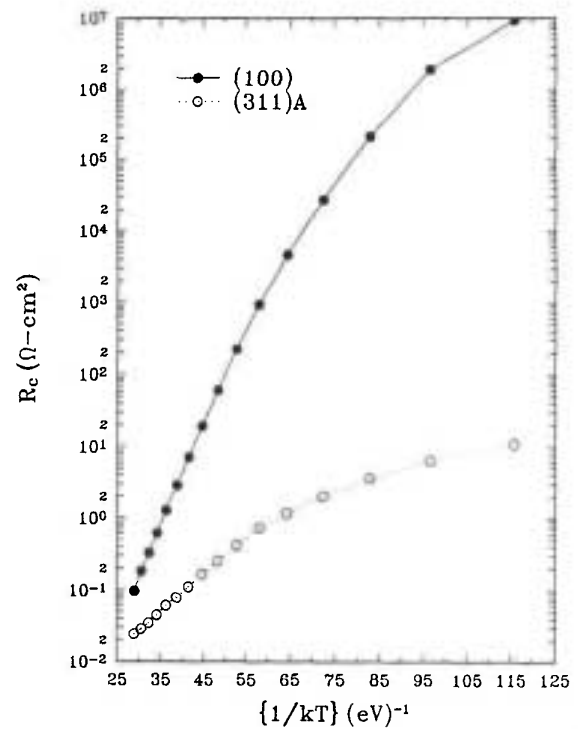


**Figure 5.** The Arrhenius behaviour of both (100) and (311) A oriented devices at 75 mV and 0 mV, extracted from the temperature dependence of device currents.

for the (100) device, whereas those of the (311)A device is shown by the open circles connected by the dotted line. The room temperature values are approximately  $0.080 \Omega\text{-cm}^2$  for (311)A device and  $2.8\Omega\text{-cm}^2$  for (100) device, respectively.

### CONCLUSION

It has been demonstrated that the resistance of ungraded p-type Bragg stack grown on (311)A oriented GaAs surface is 35 times smaller than the resistance of those grown on the conventional (100) oriented GaAs surface with similar structures. The temperature variations of I-V characteristics has shown that the effective height of the barrier at the interface of the AlAs/GaAs structure grown on the (311)A oriented wafer is smaller than that of the equivalent barrier on the (100) substrate. Although,



**Figure 6.** The specific differential resistance of both (100) and (311) oriented devices at various temperatures around Zero bias (i.e.,  $R_c = (dV/dJ)|_{V=0}$ ). The dark circles connected with a solid line represent the calculated values of the specific differential resistance for the (100) device, whereas those of the (311)A device is shown by the open circles connected by the dotted line.

the reason for the reduction in resistance of the p-type DBR is attributed to the lower effective barrier height for the (311)A structure, there are other possibilities which may account for this improvement. The band offset may be less for the (311)A than the (100), or the hole effective mass may be smaller (i.e. a smaller curvature in the valence band structure) in the (311)A direction. The lower effective barrier for the (311)A structure indicates that the tunnelling component of the hole current in this structure is greater than that of the (100) structure. Hence, one might conclude that the solubility limit of Be in (311)A AlAs layers grown by MBE should be much greater than  $5 \times 10^{17} \text{cm}^{-3}$ , obtained by Kopf et al. [2], for (100) oriented AlAs layers. In that case, the

depletion width in the (311)A oriented AlAs layers expected to be half of that in the (100) oriented AlAs layers, grown under the similar conditions, in this work. Regarding of the tunnelling probability, when the holes effective mass and the valence band offsets for both (100) and (311)A structures is considered to be similar, the tunnelling probability for the (311)A barriers under reverse bias is almost 5 times greater than that for the (100) barriers in the similar reverse bias.

By piece-wise linearly grading the heterointerfaces in a 21-pair  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  DBR mirrors with Al mole fraction of  $0.1 < x < 0.9$  and a uniform hole concentration of  $1.5 \times 10^{18} \text{cm}^{-3}$  grown on a (100) substrate, Chalmers et al. [4] have obtained resistivity of  $4.5 \times 10^{-5} \Omega\text{-cm}^2$ . Now, having the advantage of smaller effective barrier heights at (311)A oriented heterointerfaces, by using the piece-wise linearly graded interfaces in (311)A DBR, and hence reducing the effective barrier heights even further, there is the possibility of achieving resistance values of order of  $\mu\Omega\text{-cm}^2$ . In this case, manufacturing VCSELs on the (311)A oriented substrates with improved electrical performance over those grown on the (100) substrate could be beneficial.

#### REFERENCES

1. J. L. Jewell, J. Harrison, A. Scherer, Y. Lee and L. Florez, "Vertical Cavity surface Emitting Lasers: Design, Growth, Fabrication and Characteristics," *IEEE J. of Quantum Electron*, Vol. 27, 1332-1346.
2. R. F. Kopf, EF. Schubert, S.W. Downey and A. B. Emerson, "N and P-type Dopant profiles in Distributed Bragg Reflector Structures and their Effect on Resistance," *Appl. Phys. Lett.*, Vol. 62, (1992), 1820-1822.
3. A. Scherer, J. Jewell, M. Walther, J. Harbison and L. Florez, "Fabrication of Low Threshold Voltage Microlasers," *Electron. Lett.*, Vol. 28, (1992), 1224-1226.
4. S. Chalmers, K. Lear and K. Killeen, "Low Resistance Wavelength-Reproducible p-type (Al, Ga) As Distributed Bragg Reflectors Grown by Molecular Beam Epitaxy," *Appl. Phys. Lett.*, Vol. 62, (1993), 1585-1587.
5. T. Hayakawa, M. Kondo, T. Suyama, K. Takahashi, S. Yamamoto and T. Hijikata, "Reduction in Threshold Current Density of Quantum Well Lasers Grown by Molecular Beam Epitaxy on  $0.5^\circ$  Misoriented (111)B Substrates," *Jpn.J. Appl. Phys*, Vol. 26, (1987), L302-305.
6. F. A. Pavadoni and R. Straton, "Field and Thermionic-Field Emission in Schottky Barriers," *Solid State Electron*, Vol., (1966), 695-707.
7. A.Y.C. Yu, "Electron Tunnelling and Contact Resistance of Metal-Silicon Barriers," *Solid State Electron*, Vol. 13, (1970), 239-247.