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Testable MUXED-D Scan Cell in Quantum-dot Cellular Technology

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is one of the new nanoscale technologies which proposed for future circuits. This technology has been remarkable due to its faster speed, lower size and reduction in power consumption compared to CMOS technology. Many circuits have been implemented in this technology including shift registers, they are one of the most important digital circuits for many applications. With the development of QCA technology, it is important to provide testing methods for testing these circuits.4-Bit serial shift registers designed in previous research were not capable of testing their output. In this paper, MUXED-D scan cell concept helps to detect the errors before fabrication and reduce time and cost. The MUXED-D scan consists of a D flip-flop and a 2 to 1 multiplexer. Compared to the latest scan cell, we have seen a 25 % decrease in occupied area and 15.62 % decrease in the number of cells and latency from 1 to 0.75 clock cycle. In general, this scan cell circuit is made of 27 cells with an area of 0.03 μm^2 and a latency of 3 clock cycles. The proposed shift register includes four scan cells with two inputs which includes main and test signals. In fact, the number of cells used for the last 4-bit serial testable shift register in this design is 324, 0.39μm^2 occupied area and the corresponding delay is 6.75 clock cycles. In order to verify this performance, QCA simulator is used.

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1. INTRODUCTION

According to the Moore's law, the trend of doubling the number of transistors used in each chip with time has become a major challenge for CMOS technology. Physical limitations on the CMOS prevents the transistor from shrinking. It can be said that emerging Quantum-dot Cellular Automata (QCA) technology has partially compensated for the constraints of CMOS [1]. Due to the structure of the cells in the QCA, one of the suitable alternatives for CMOS is QCA technology [2]. What is clear is that registers are needful components for storing binary information [3]. So, designing circuits specially registers, without detects is something that needs to be addressed. One of the steps to complete the design is to test, obviously if the test is done in the last step of the design, it will take a lot of effort [4]. One such solution is using scan flip-flop. A scan flip-flop is one of the tools that is widely used to test the correct operation of the circuit, it consist of multiplexer and D flip-flop [5]. It has a control line for selecting data or scanning input. By checking the current status of the flip-flop, it ensures that the flip-flop output is correct, that we can troubleshoot the circuit in larger-scale , and locate the fault [6].

Apparently, not much research has been done on this issue, some of them have tried to improve the efficiency of scan cells. In these papers, they described how they could improve circuits such as scan cells by making multiplexers more efficient [5, 7, 8]. The scan circuit proposed by Goswami et al. [7] occupied a large area due to the large number of its cells. Harshitha et al. [5] and Shantala and Karthik [8] tried as much as possible to reduce the size of the circuit and use fewer cells, but they did not make any progress in terms of latency and it remained 4 clock cycles. In this paper, the scan cell is optimized and testing of QCA based shift register is studied. Eventually the proposed design is defined. In other words, by replacing the scanning cell, the function

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of the shift register can be checked. This means that by selecting the test input line of the shift register, we can change its status to test mode and check its output, and then the circuit can continue to operate normally. This article is divided into sections to make it easier to understand the essence of the case. It has been discussed in the second section about the structure and logic of QCA design. The main gates and the concept of clock are examined in QCA technology. Then, in the third part, the designed circuits that are used for the final simulation are introduced. In the next part, the recommended test shift register is introduced and its implementation and performance are examined. At the last part, the conclusion of the work has been done.

2. BACKGROUND

The technology is based on a quantum cell which has a square shape and has four quantum dots in its corners. Each cell has two electrons that can move between the quantum dots. These electrons tend to minimize their mutual Coulomb interaction, for this reason, they placed in opposite corners of the cell [9]. This act causes two polarizations in the form of +1 and −1.The polarization of the cell in the P=+1 represents logic "1" and P = -1 represents logic "0" (Figure 1) [10]. Basic implementations in QCA are wire, inverter, and majority gate. A line of cells can be used as a QCA wire to propagate information [11]. Due to the Coulomb interactions between cells, binary information transmit from input to output (Figure 2) [12]. Also, the majority gate consists of 5 cells. As shown in Figure3 cells are used as input and the middle cell is used as a voter and the other cell is the output of this gate. In fact, the voting cell performs the main operation. The logic of the majority voting can be demonstrated by Boolean operators in this way:

$$M(A,B,C)=AB+BC+AC \quad (1)$$

The said system can perform AND/OR operations. To convert the majority gate to the AND/OR gates, one of the input cells must consider as a program line. When program line is equal to 1, OR gate is performed and when the line is equal to 0, the AND gate is performed [13].

Moreover, the not gate is another one of the fundamental gates of QCA circuits. The position of the

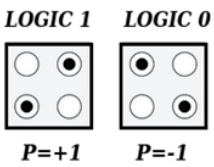


Figure 1. QCA cell [12]

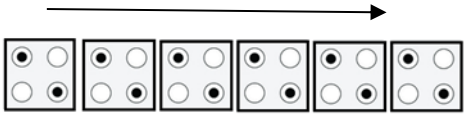


Figure 2. QCA wire [12]

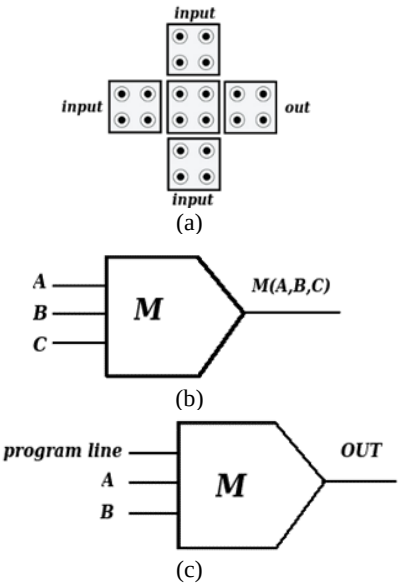


Figure 3. (a) The QCA majority gate; (b) The schematic of majority gate; (c) The schematic of programmable AND/OR gate [12]

cells makes them try to reach a stable state. Eventually, the input and output are reversed. Two types of implementation of this gate are shown in Figure 4.

In addition to controlling the flow of information throughout the circuit, clocking provides the true power of the QCA circuit [9]. QCA cells have 4 clock states, including switch, hold and release and relax (Figure 5) [14]. In fact, increasing or decreasing the potential barrier between neighboring cells changes the status of the cells. As the potential barrier rises, the tunneling rate decreases and the electrons are placed in the right place, and the

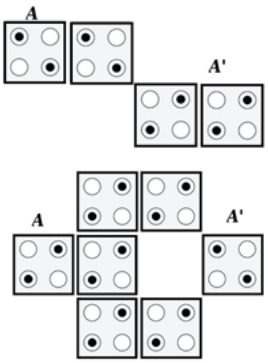


Figure 4. QCA inverter [12]

cell becomes definitively polarized [15]. In the first phase that it called switch, the polarization of the cell is done and reaches its final binary state. In the hold phase, the cell retains its polarity and is not affected by the surrounding cells. In the next phase potential barrier is decreases, as a result it gradually loses its polarity. In the following, there is no potential barrier and the cell does not affect other cells in relax phase.

3. RELATED WORKS

In this section related works which can prove the better performance of proposed designs will be introduced.

3. 1. QCA Multiplexer Multiplexer receives data from input lines, with one of the inputs sending data to the output at a time, based on selector signals [16]. The output of this combinational logic circuit for 2-input line is confirmed by following simplified Boolean expression

$$Q = \overline{S}\ \ I_1 + S\ \ I_0 \quad (2)$$

when S='0' the Q is equal to I_1 and when S='1' the Q is equal to I_0. This design has 12 cells and 1 clock zones latency. The schematic and QCA layout of the recent previous 2:1 multiplexer is shown in Figure 6 [17].

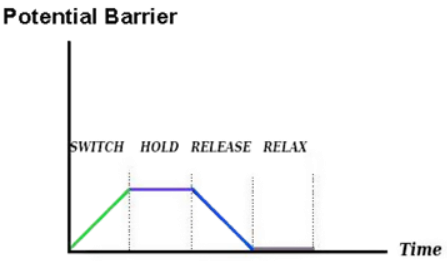


Figure 5. QCA clock phases [18]

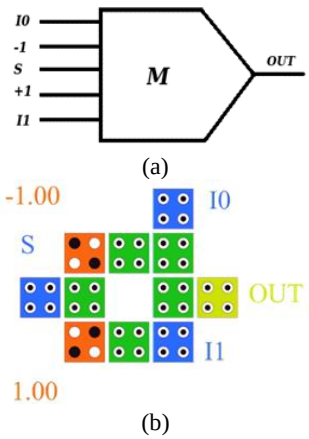


Figure 6. 2:1 multiplexer, (a) Schematic; (b) QCA layout [17]

3. 2. QCA D Flip-flop The D storage element is one of the most widely used in the structure of logic circuits design. A flip-flop called a 'Delay flip-flop' or 'data flip-flop' and latch is a circuit that stores one bit [19]. The main difference between the two circuits is that the latch is level-sensitive while the flip-flop is edge-triggered. Figure 7 shows the structure of D latch which consists of two input: a data line and a control line for the clock signal. The Q represents output state of the latch. The remarkable point about performance of latch is that the input can change the output state when the clock is not low. D latch layout which is implemented with multiplexer, involves 18 cells and input–output delay takes 0.5 clock cycle (Figure 8) [20].

It is possible to use the structure that mentioned by Hashemi and Navi [21] to convert the latch to a flip-flop. By performing the AND operation between the current and reverse clock pulses, the required output clock is generated. The corresponding layout and diagram of D flip-flop are shown in Figure 9.

4. PROPOSED SHIFT REGISTER WITH TEST ABILITY

Shift registers are sequential logic circuits, usable for storing and transferring data, this device shifts the input data to the output with each clock [18]. A shift register is created by connecting the output of one flip-flop to the input of the next flip-flop in the chain using a cascade of flip-flops with the same clock [19]. (Shown in Figure 10). Test capability is provided by having a scanning cells in desired circuit. As we can see in the Figure 11, this

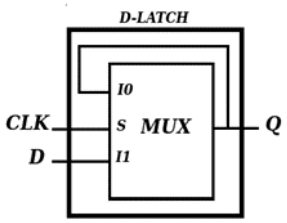


Figure7. D latch diagram

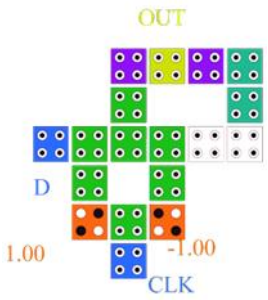
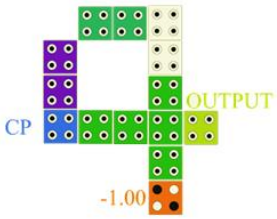
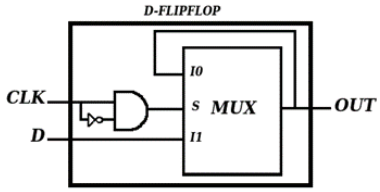


Figure 8. QCA layout of D latch [20]



(a)



(b)

Figure 9. (a) layout of the edge to level converter [22]; (b) diagram of the D flip-flop [23]

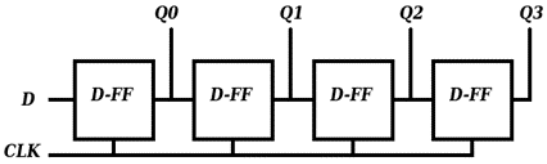


Figure 10. Diagram of 4-bit series shift register [20]

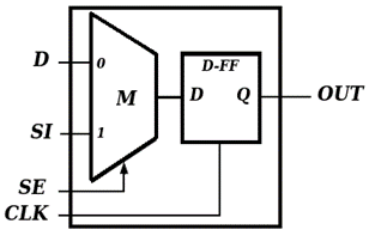


Figure 11. Scan cell diagram [8]

element consists of a multiplexer and a D flip-flop. The selector of multiplexer puts SI on the input line of the flip-flop when it has a '1' value and DI when it has a value of '0'. It contains 27 cells and takes 0.75 cycles that results get correct output [4]. Figure 12 shows the layout of scan cell that described. Suggested scan cell is more efficient than designed scan cells. Table 1 gives a brief overview of designed scan cells during past research.

Each of the flip-flops has been replaced with scan cells to add testability to the proposed SISO shift register circuit. The proposed shift register can be seen in the Figure 13. To form the shift register, the output of the first scan cell is connected to the inputs of the second scan cell, and each output is still connected to the SI and DI of the next scan cell. Also, the selector and clock inputs are connected to all scan cells simultaneously. As a result, a

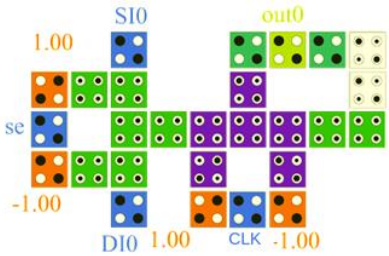


Figure 12. Scan cell layout

TABLE 1. Performance analysis of scan flip-flop

Sff	Number of Cells	Area (μm²)	Latency
[7]	72	0.12	4
[8]	40	0.06	4
[5]	32	0.04	4
Proposed	27	0.03	3

chain of scan has emerged. By placing the converter for the clock, we actually sensitized the D latches, which we have used in the scan cells structure, to the rising edge. Based on the simulation, the delay is equal to 6.75 cycles and its area is 0.39μm² with number of 324 cells. Figure 14 shows the proposed shift register which is made by joining 4 scan cells.

5. SIMULATION RESULTS

The designs of the proposed circuit have been performed on QCA Designer software. The result of the simulation is shown in Figure 15. In addition, the scan cell simulation result, which is an important component of the proposed shift register structure, is shown in Figure 16.

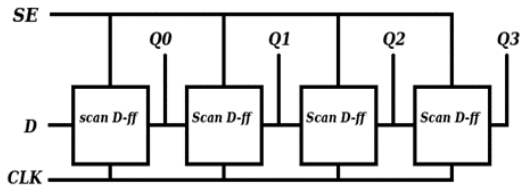


Figure 13. Proposed 4-bit SISO shift register

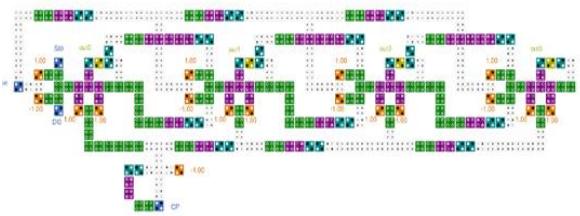


Figure 14. Layout of proposed testable shift register

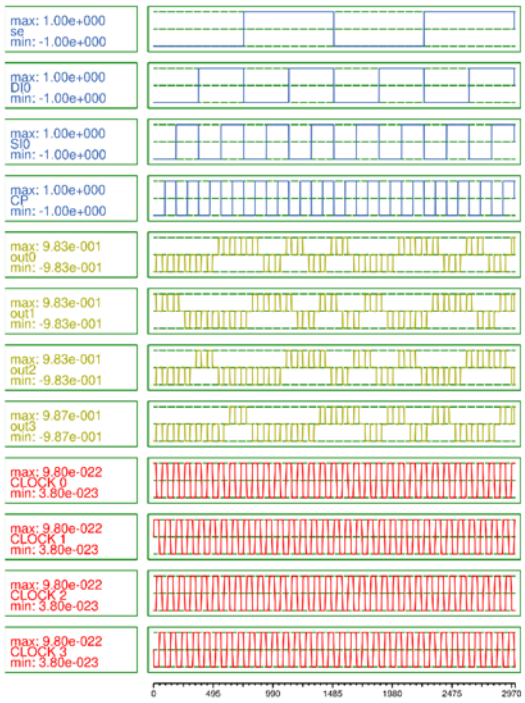


Figure 15. Simulation result of proposed 4-bit testable shift register

Figure 16. simulation result of scan cell

The output of the scan cell simulation shows the correct operation of this design. This circuit is made of a multiplexer and D latch. According to this, output is the result of changes in the clock and selector level. The multiplexer used in the scan cell allows us to choose between SI and D by SE. As it is known, if the clock is in the enable state and SE is zero, D will appear in the output and if its value is one, SI will be displayed. In the opposite case, if the clock is not enabled, the previous values of the circuit will be displayed again without considering the inputs and SE.

The proposed structure consists of positive edge-triggered flip-flops, so output changes only at the point in time when the clock changes from 0 to 1. When the clock pulse is applied, depending on the value of SE, one or two input values are enter the shift register. Applying the next clock will transfer the output of each scan cell to the input of the next scan cell. The result of this simulation is shown in Figure 15 represents that when SE is zero, D is selected as the input, and when the clock becomes one after a delay of 0.75 cycles, the first input is placed on output0. In the next cycle, the new input is placed at output0. Of course, this new input can be D or S depending on the SE value. So the previous value of output0 is stored in output1 and continues to reach output3.

The thermal hotspots in the average power dissipation map of proposed 4-bit testable shift register with 0.5 E_k is shown in Figure 17. We obtained this diagram with the QCAPro tool to estimate the average, maximum, and minimum power dissipation in a QCA circuit while the input is being switched [24]. In this diagram, the darker color indicates the high level of energy loss whereas the input cells are shown as white cells.

Figure 17. Energy diagram of proposed 4-bit testable shift register

6. CONCLUSION

With the complexity and increasing number of inputs in designed circuits, the ability to test different parts of the circuit has become very important. Therefore, by adding a test cells to the desired circuit, the output of different parts can be controlled. Necessity of presence of shift registers in the memory structure is not hidden from anyone, In addition, the test capability hasn't been implemented in previous shift registers. Though, in this

work, we have proposed a design and layout for QCA testable SISO shift register. In this proposed design, the efficiency of the shift register has been improved by reducing the size and latency of the test cells.

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Persian Abstract

چکیده

اتوماتای سلولی- نقطه‌ای کوانتومی (QCA) یکی از تکنولوژی‌های نوین در مقیاس نانو است که برای مدارهای آینده پیشنهاد شده است. این تکنولوژی به دلیل سرعت بالاتر، اندازه کوچک تر و کمتر بودن توان مصرفی در مقایسه با تکنولوژی CMOS قابل‌توجه بوده است. مدارات زیادی از جمله شیفت رجیسترها با این تکنولوژی پیاده‌سازی شده‌اند. شیفت رجیسترها از مهم ترین و پرکاربردترین مدارات دیجیتالی هستند. با توسعه تکنولوژی QCA، ارائه روش‌هایی برای تست این مدارات بسیار مهم و حیاتی است. شیفت رجیسترهای سری ٤بیتی که در تحقیقات قبلی طراحی شده‌اند، قادر به آزمایش خروجی خود نبوده اند. در این مقاله مفهوم سلول اسکن MUXED-D به شناسایی خطا قبل از ساخت، کاهش زمان و هزینه کمک می‌کند. اسکن MUXED-D از یک فلیپ فلاپ D و یک مالتی پلکسر ۲به۱ تشکیل شده است. در مقایسه با آخرین سلول اسکن طراحی شده، شاهد ۲۵ ٪ کاهش در مساحت اشغالی و ۱۵.٦۲ ٪ کاهش در تعداد سلول‌ها و کم شدن تاخیر از ۱ به ۰.۷۵ هستیم. به طور کلی، این مدار سلول اسکن از ۲۷ سلول با مساحت μm^2 ۰.۰۳ و تاخیر ۳ سیکل کلاک ساخته شده‌است. شیفت رجیستر پیشنهادی شامل چهار سلول اسکن با دو ورودی است که شامل سیگنال‌های اصلی و آزمایشی می‌باشد. در حقیقت، تعداد سلول‌های مورد استفاده برای شیفت رجیستر سری ٤ بیتی طراحی شده ۳۲٤ بوده و μm^2 ۰.۳۹ مساحت اشغال‌شده و تاخیر مربوطه ٦.۷۵ سیکل کلاک می‌باشد. به منظور تایید این عملکرد، شبیه‌ساز QCA مورد استفاده قرار گرفته است.