



Carbon Nanotube Field Effect Transistors Based Digitally Reconfigurable Single Differential Voltage Current Conveyor based Analog Biquadratic Multifunctional Filter at 32nm Technology Node

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ABSTRACT

As the scaling continues, Carbon Nanotube Field Effect Transistors (CNFET) are considered to be the potential candidates for overcoming the shortcomings associated with the scale of the art Complementary metal-oxide-semiconductor (CMOS) transistors. In this paper a digitally reconfigurable CNFET based biquadratic multifunctional filter employing a CNFET based single Differential Voltage Current Conveyor (DVCC) at 32nm technology node is presented. The circuit utilizes a single CNFET based DVCC block along with the arrangement of few resistors and capacitors. The proposed digitally reconfigurable multifunctional filter circuit is able to obtain programmable low pass, high pass and band pass filter configurations using the same topology. The designed CNFET based multifunctional filter obtains a resonant frequency of the order of GHz. Furthermore, a 3-bit digital control of the designed multifunctional filter parameters i.e. Quality Factor (Q_0) and resonant frequency has been made possible using the Current Summing Network (CSN). Sensitivity and comparative analysis has also been performed. The circuit has been simulated at a low voltage supply of 0.9V using Hewlett Simulation Program with Integrated Circuit (HSPICE) environment at 32nm technology node. The simulation results obtained are in sync with the theoretical analysis.

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NOMENCLATURE

D_{CNT}	Diameter of CNT	G	Conductance
V_{th}	Threshold Voltage	V_X	Potential at X terminal of DVCC
S	Inter-CNT pitch	$I_{Y1} \& I_{Y2}$	Currents entering the Y_1 and Y_2 terminals of DVCC respectively
N	Number of CNT's in the channel	Q	Quality Factor
q	Electronic Charge	ω_0	Resonant Angular frequency
N_1, N_2	Chiral Vector	R	Resistance
V_π	Carbon bond energy ($\pi-\pi$)	C	Capacitance
a	Lattice Constant	k	Current transfer gain parameter

1. INTRODUCTION

For the last 30-40 years, CMOS technology has played a quintessentially important role in the advancements observed within the fields of computation, telecommunications, electronics, mechatronics, and instrumentation. Miniaturizations, or scaling down the size of the basic device has been the blueprint, which

allowed for higher speed, lower power dissipation, lesser costs and higher integration density. However, as the CMOS transistors continues to scale down, various non-idealities like tunneling phenomenon, process variations, random dopant fluctuations, leakage currents etc. hinder its exemplary performance, thereby making it indispensable to look for alternatives that could continue to revolutionize the advancements. Off late a lot of

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research has been ongoing, in designing and developing new Nano-electronic devices, and various substitutes like Quantum FETs, FinFETs, Nano-sheet transistors have appeared. Carbon Nano Tube Field Effect Transistor (CNFET) is also considered among one of the potential candidates for extending the already saturated Moore's law and providing a platform for the next generation electronic circuits [1-5]. A CNFET is a molecular device, having three terminals namely drain, source and gate. It uses a semiconducting carbon nano tube (CNT) acting as a channel, bridging the contact between two electrodes i.e. source and drain. CNFET's are considered as potential candidates, in the post Silicon era owing to its exceptional electrical and structural characteristics. It offers high mobility, greater current carrying capacity, better transconductances, low intrinsic capacitances, improved subthreshold slope etc. among various improved parameters over the state of the art CMOS transistors [6, 7].

Second generation current conveyor, a well known current mode device (CC-II) was introduced by Sedra and Smith in 1970. It is a versatile analog building block, used to implement variety of voltage and current mode circuits like amplifiers, oscillators, multifunctional filters etc. [8, 9]. However, the design of various new circuits and topologies requires two high input impedance terminals or the usage for differential input signals; thereby restricting the utilization of the conventional Current Conveyor. Differential voltage Current conveyor (DVCC) is a relatively new analog building block, coming from the family of current conveyors. DVCC utilizes the concept of differential inputs and is widely used for the implementation of various voltage and current mode analog signal processing circuits. It also offers high signal bandwidth and greater linearity, thereby making it an attractive proposition for the researchers and designers [10, 11].

In this work, the single input multi output voltage mode multi-functional proposed by Chen et al. [12] has been redesigned using optimized CNFETs. Furthermore the circuit is digitally controlled using a 3-bit current summing network. Introduction of digital control to the DVCC based multifunctional filter provides flexibility in reconfiguring the circuit while helping to adapt specifically to the requirements of different modern analog system applications. The outline of the paper is as follows: After introduction in section 1, Carbon Nanotubes Field Effect Transistors (CNFET) have been discussed briefly in Section 2, followed by the discussions around Differential Voltage Current Conveyor (DVCC) and the design of CNFET based DVCC biquadratic multifunctional filter in section 3 and 4, respectively. Section 5 highlights digitally reconfigurable DVCC followed by the design of CNFET based Digitally reconfigurable multifunctional filter in

section 6. Section 7, 8 and 9 of the paper, discuss the obtained simulation results (in sync with the theory), sensitivity analysis and comparative analysis respectively; which is followed by conclusion.

2. CARBON NANOTUBE FIELD EFFECT TRANSISTORS

Carbon Nanotubes (CNT's), a promising nanostructured material was initially discovered by Iijima [13]. It is basically a group of carbon atoms; arranged hexagonally and rolled up into a seamless cylindrical shape with length of the order of few microns and diameter of few nanometers. CNT's can be of following types i.e. armchair, chiral or zig-zag in nature, depending upon the chiral vector (n_1, n_2). A CNT is called Zigzag if $n_1=0$ or $n_2=0$. If n_1 & n_2 are unequal and non-zero, CNT is said to be of chiral type and if $n_1 = n_2$, then it's called Armchair configuration [14]. Carbon Nanotube Field Effect Transistors (CNFET) utilize the semiconducting CNT's for the transport of electrons in the channel region. Depending upon the current requirement in the designed circuit, maybe one or usually multiple semiconducting CNTs are arranged in parallel configurations between the drain and source regions. The transport of charge carriers (electrons or holes) between the highly doped drain/source regions takes place through these semiconducting CNT's which expedite intrinsic ballistic transport properties associated with the CNTs. The Ballistic transport ensures that the mobility of the charge carriers is comparatively much higher as compared to the silicon CMOS devices. The top end view of CNFET device, incorporating the design parameters is shown in Figure 1. The number of CNT's in the channel (N), the Diameter of CNT (D_{CNT}) and the Inter CNT Pitch (S) are the important parameters associated with the design of CNFET based circuits [15]. The equations co-relating the important parameters of chiral vector (m, n), threshold voltage (V_{th}), diameter of CNT (D_{CNT}), Inter-CNT Pitch (S), Number of CNTs in the channel (N) and Energy Gap (Σg) are as follows :

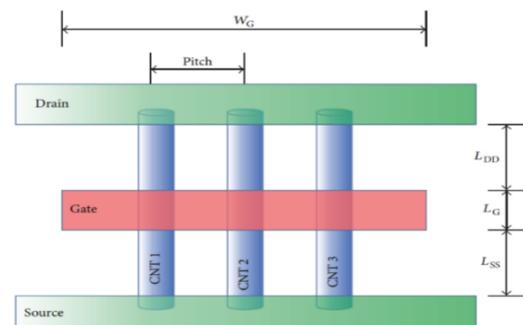


Figure 1. Top-End View of CNFET

$$D_{CNT} = \frac{\sqrt{N_1^2 + N_2^2 + N_1 N_2}}{\pi} \tag{1}$$

$$V_{th} = \frac{a V_{\pi}}{\sqrt{3} q D_{CNT}} \tag{2}$$

$$W = (N-1) * S + D_{CNT} \tag{3}$$

$$\Sigma_g = \frac{0.84 eV}{D_{CNT}} \tag{4}$$

where q is the electronic charge, a= 2.49 is the lattice constant and V_{π} is the carbon bond energy (π - π) and is equal to 3.033eV. Furthermore, the working principle of CNFET device is similar to the CMOS in which electrons flow from source to drain terminal and the gate terminal is used for controlling the current intensity in the semi-conducting CNT channel [16]. However, unlike CMOS, where there is a standard convention of keeping the transistor's width usually 2X-4X transistor's length; no such constraints exist for CNFETs, since in CNFETs both the n and p type of devices have equal current carrying capabilities, and the device is optimized in terms of number of CNT's (N), Inter-CNT Pitch (S) and diameter of CNT (D_{CNT}). The circuit compatible Stanford CNFET Model developed by Deng and Wong [17, 18] have used for carrying out the simulation using HSPICE environment at 32nm technology node. The model has been experimentally validated and accounts for the non-idealities like channel length dependence of current drive, source drain series resistance, inter-CNT charge screening effects etc. along with the device parasitics associated with more than 90% accuracy.

3. DIFFERENTIAL VOLTAGE CURRENT CONVEYOR

Differential Voltage Current Conveyor (DVCC) is one of the widely used blocks for analog signal processing. It is basically a current mode device and can be used for the design of various analog circuits like integrators, amplifiers oscillators, filters etc. The block diagram of DVCC is shown in Figure 2 and its terminal characteristics is described by the matrix given in equation 5, where V_X is the potential at X terminal ; I_{Y1} and I_{Y2} are the currents entering the Y_1 and Y_2 terminals, respectively. Furthermore I_{Z+} is the positive type current. It is to be noted that at terminal X, DVCC shows (ideally) zero input resistance, whereas at both terminals Y and Z, it exhibits (infinite) high resistance [19].

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \end{bmatrix} \tag{5}$$

Significant amount of research, off-late has been carried out using DVCC building block. Upadhyay and Pal [20] proposed an Op-Amp based on DVCC, capable of

operating at higher frequencies as compared to the conventional op-amp. Vavra [21] designed a capacitance multiplier employing a single DVCC, whereas Jain and Bharti [22] realized LNA for wireless receivers using CMOS based DVCC. The basic modules of integrators and differentiators have also been implemented using the same DVCC block incorporating a few passive elements by Minaei [23]. Furthermore numerous universal and multifunctional filters, based on voltage and current mode have also been designed, implemented and verified using the same DVCC thereby making it an extremely significant building block of interest for researchers [24-29].

4. DESIGN OF CNFET BASED DVCC MULTIFUNCTIONAL FILTER

The circuit diagram of Voltage Mode Multifunctional filter realized by Chen et al. [12] using TSMC 0.18 um CMOS technology is shown in Figure 3 and has been used in this work for redesigning as digitally reconfigurable CNFET based filter. It is to be noted that, the circuit has been completely re-designed using optimized CNFET transistors at 32 nm technology node. Number of CNT's (N), Inter-CNT Pitch (S) and diameter of CNT (D_{CNT}) have been carefully chosen to provide an optimum DVCC performance and then the circuit has

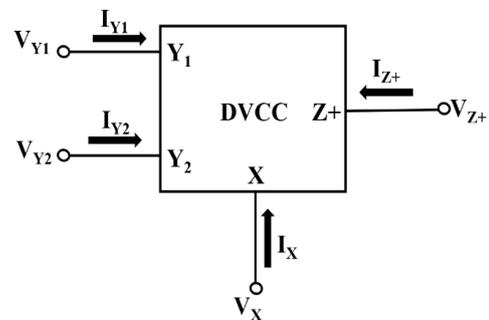


Figure 2. Block Diagram of DVCC based on Z+ node

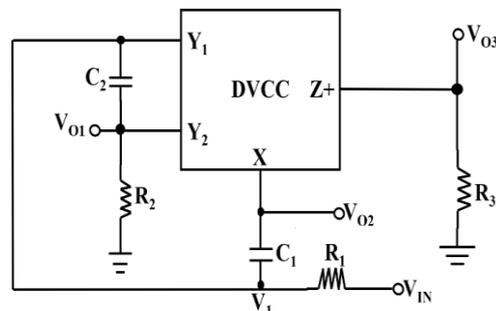


Figure 3. Circuit diagram of DVCC Multifunctional Filter [12]

been digitally programmable using Current Summing Network (CSN). The configuration of the used circuit [12] gives the band-pass, low-pass and high-pass filters as signified by Equations (6), (7) and (8), respectively.

$$\frac{V_{O1}}{V_{IN}} = \frac{sC_2G_1}{s^2C_1C_2 + sC_2(G_1+G_2) + G_1G_2} \quad (6)$$

$$\frac{V_{O2}}{V_{IN}} = \frac{G_1G_2}{s^2C_1C_2 + sC_2(G_1+G_2) + G_1G_2} \quad (7)$$

$$\frac{V_{O3}}{V_{IN}} = \frac{-G_1}{G_3} \frac{s^2C_1C_2}{s^2C_1C_2 + sC_2(G_1+G_2) + G_1G_2} \quad (8)$$

where $G_1 = \frac{1}{R_1}$, $G_2 = \frac{1}{R_2}$, $G_3 = \frac{1}{R_3}$

The quality factor(Q) and resonant angular frequency (ω_0) is given below:

$$Q = \frac{1}{G_1+G_2} \sqrt{\frac{C_1G_1G_2}{C_2}} \quad (9)$$

$$\omega_0 = \sqrt{\frac{G_1G_2}{C_1C_2}} \quad (10)$$

The circuit employed realizes the biquadratic band pass (V_{O1}), low pass (V_{O2}) and high pass filters (V_{O3}) simultaneously without changing the values of passive components. The DVCC multifunctional filter is simulated at supply voltages of $V_{DD}=-V_{SS}=0.9V$ using the 32nm Stanford CNFET model at HSPICE simulation environment. The circuit is re-designed for $f_0=1.06$ GHz and $Q=0.5$ by selecting the value of $R_1=R_2=R_3=10k\Omega$ $C_1=C_2=15ff$. The CNFET technology parameters used for the simulation have been listed in Table 1, whereas the optimized parameters of Number of CNT's (N), Inter-CNT Pitch (S) and Diameter of CNT (D_{CNT}) used for simulation have been discussed as a part of design in Section 5. Figure 4 shows the obtained amplitude frequency response of the multifunctional filter. It is to be noted that since CNFET technology has been used the obtained frequency response is having the 3-dB cut off frequency of the order of 1.08 GHz, which is significantly of the higher order. The 3-dB frequency of the designed filter in-fact could be further enhanced, by changing the optimized parameters of CNFET particularly the Diameter of CNT (D_{CNT}), however the same is achieved at the cost of increased power dissipation.

5. DIGITALLY PROGRAMMABLE CNFET DVCC

The terminal characteristics of digitally reconfigurable/programmable differential voltage current conveyor (DP-DVCC) is determined by the matrix given below in Equation (11) [30].

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ k & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \end{bmatrix} \quad (11)$$

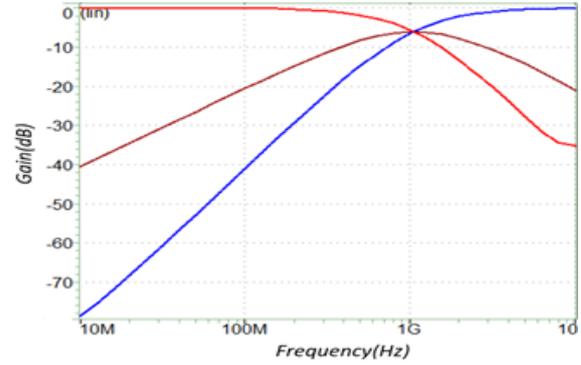


Figure 4. Simulated amplitude frequency response of MF

TABLE 1. technology parameters of CNFET

Parameters	Value ^a
Oxide Thickness	4 nm
Physical Channel Length	32 nm
Gate Dielectric & Dielectric Constant	HfO ₂ & 16
Mean Free path (Intrinsic CNT)	200 nm
Mean Free Path (Doped CNT)	12.5 nm

where, $k = \frac{I_Z}{I_X}$

Digitally programmable DVCC is used to inculcate the factor of re-configurability in DVCC multifunctional filter. A Digital control word is generated by the use of Current Summing Network (CSN) which is added at the Z+ terminal and it varies from 1 to 2^n-1 where n is number of transistor arrays connected in parallel. CSN is employed to control the current transfer gain parameter- k [31]. Therefore, Current at the Z+ terminal assumed to be flowing out of DP-DVCC is shown in Equation (12) and the current transfer gain parameter- k is given by Equation (13):

$$I_Z = \sum_{i=0}^{n-1} d_i 2^i (I_7 - I_{10}) \quad (12)$$

$$k = \frac{I_Z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i (I_7 - I_{10})}{(I_7 - I_{10})} = \sum_{i=0}^{n-1} d_i 2^i \quad (13)$$

where d_i is the digital code bit applied to the i^{th} branch of the CSN. Depending upon the value of d_i , whether it's a logic 1 or logic 0 the current flow in a particular branch is either enabled or disabled [32]. The implementation of DP-DVCC using CNFETs is shown in Figure 5 and the dimensions of the individual designed optimized CNFETs have been enlisted in Table 2. The CNFET transistors of DP-DVCC have been individually optimized in terms of design parameters i.e. Number of CNT's, Inter-CNT Pitch and Diameter of CNT to obtain an improved high frequency response. While designing, it has been ensured that the inherent port characteristics of the DVCC reflect near to ideal behavior. The

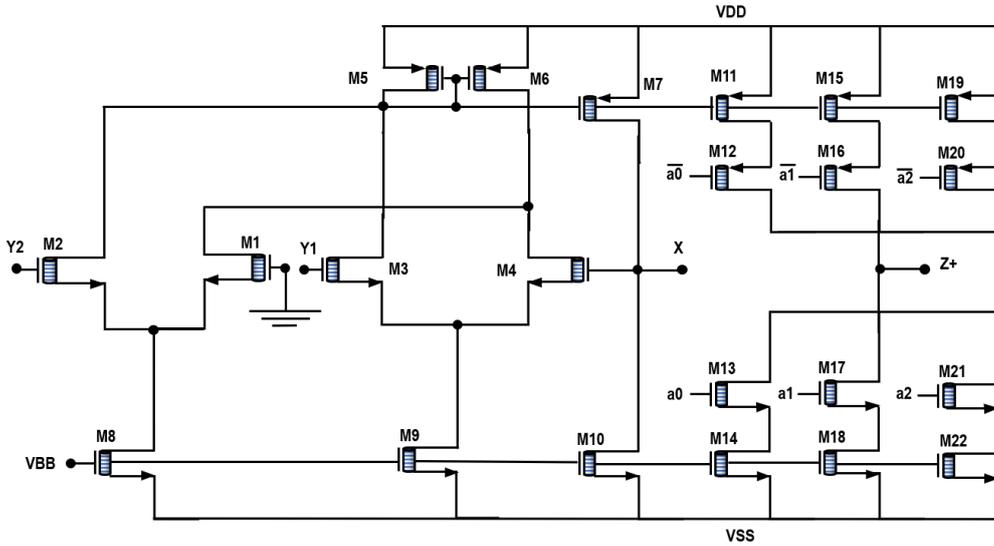


Figure 5. CNFET based implementation of DP-DVCC on Z+ node only

simulated obtained input resistances at Port Y₁ (R_{Y1}) and Port Y₂ is (R_{Y2}) 6.2 MΩ, whereas the value obtained at Port X (R_X) is 275Ω.

6. OPTIMIZED CNFET BASED DP-DVCC MULTIFUNCTIONAL FILTER

The designed DP-DVCC is now employed as the basic building block for the programmable multifunctional filter. The proposed circuit of DP-DVCC multifunctional filter with the help of CNFET technology; that incorporates the tunability factor using current summing network is shown in Figure 6. The circuit besides realizing the filter functions of low-pass, high pass and bandpass also includes the feature of varying the quality factor and resonant frequency with the help of the applied digital control word (k). There is a significant change in the transfer function of the tunable biquadratic multifunctional filter responses which is given below as follows:

$$\frac{V_{O1}}{V_{IN}} = \frac{k s C_2 G_1}{s^2 C_1 C_2 + s k C_2 (G_1 + G_2) + k G_1 G_2} \quad (14)$$

$$\frac{V_{O2}}{V_{IN}} = \frac{k G_1 G_2}{s^2 C_1 C_2 + s k C_2 (G_1 + G_2) + k G_1 G_2} \quad (15)$$

$$\frac{V_{O3}}{V_{IN}} = \frac{-G_1}{G_3} \frac{k s^2 C_1 C_2}{s^2 C_1 C_2 + s k C_2 (G_1 + G_2) + k G_1 G_2} \quad (16)$$

Equations (12), (13) and (14) depicts the transfer response of the digitally programmable band pass, low pass and high pass filters respectively. The modified expressions of quality factor (Q) and resonant angular frequency (ω_0) is shown as is:

$$Q = \frac{1}{G_1 + G_2} \sqrt{\frac{C_1 G_1 G_2}{k C_2}} \quad (17)$$

$$\omega_0 = \sqrt{\frac{k G_1 G_2}{C_1 C_2}} \quad (18)$$

The theoretical analysis hereby highlight the fact that the quality factor $Q \propto \frac{1}{\sqrt{k}}$ and the resonant frequency $\omega_0 \propto \sqrt{k}$ of the proposed multifunctional filter.

7. SIMULATION RESULTS AND DISCUSSION

The proposed digitally programmable optimized CNFET based multifunctional biquadratic filter comprises of a block of DP-DVCC, three resistors and two capacitors. The simulations results obtained have been verified on HSPICE. The obtained resultant waveform of the simulated multifunctional filter for different control words of [011] and [111] is shown in Figures 7 and 8, respectively. The obtained simulation results are in accordance to the theoretical results obtained in the previous section, where ω_0 is directly proportional to $k^{1/2}$ and for reference the variation of the resonant/cut-off

TABLE 2. design of cnfet based digitally programmable dvcc

Transistor	Number of CNT's	Inter CNT Pitch	Chiral Vector (m,n)	Diameter of CNT	Column 3 ^a
M1-M14	4	75nm	(19,0)	1.5 nm	zzz1
M15-M18	8	32nm	(19,0)	1.5nm	zzz2
M19-M22	16	15nm	(19,0)	1.5nm	zz3

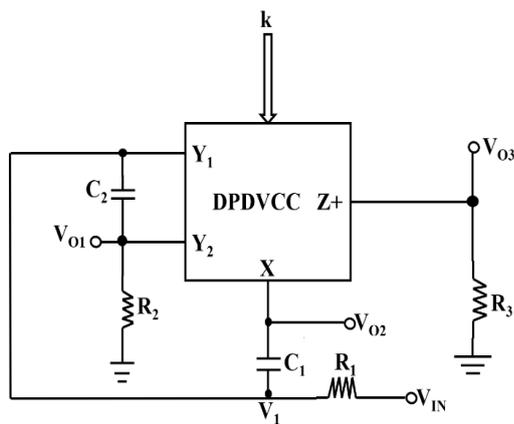


Figure 6. Circuit diagram of CNFET based DP-DVCC Multifunction filter

frequency with the digital control word for band-pass, low-pass and high-pass filters is depicted in Figures 9-11, respectively. The effect of the variation of quality factor with the digital control word has also been studied and is reflected in Figure 12, which shows that the quality factor is inversely proportional to the applied digital control word. It is to be further impressed that besides being programmable the circuit exhibits excellent high frequency response of the order of Gigahertz range that makes it useful for wideband, radio-frequency and Bluetooth applications.

8. SENSITIVITY ANALYSIS

This section deals with the sensitivity analysis of the programmable multifunctional filter circuit parameter’s such as quality factor, resonant frequency and bandwidth with reference to the passive components of resistance and capacitance. Table 3 depicts the results of sensitivity analysis of the circuit. The results obtained in Table 3 depicts the fact that the variations in the circuit parameters of the proposed programmable multifunctional filter with respect to the passive components is below 1; thereby affirming that tolerances in the values of passive elements won’t degrade the performance of the circuit.

9. COMPARATIVE ANALYSIS

Table 4 summarizes the comparison of the designed CNFET based biquadratic multifunctional filter, with other circuits of similar nature available in literature. The 3-dB cut off frequency, port resistances at input and output, number of active and passive components used, the realizations possible with the topology and sensitivity

analysis have been chosen as the parameters of comparison among various realized multifunctional filters. The comparative analysis clearly indicates the improved performance of the circuit, owing to the superior performance of the optimized CNFET transistors in terms of better cut-off and resonant frequencies, near to ideal port resistances and lower sensitivity issues.

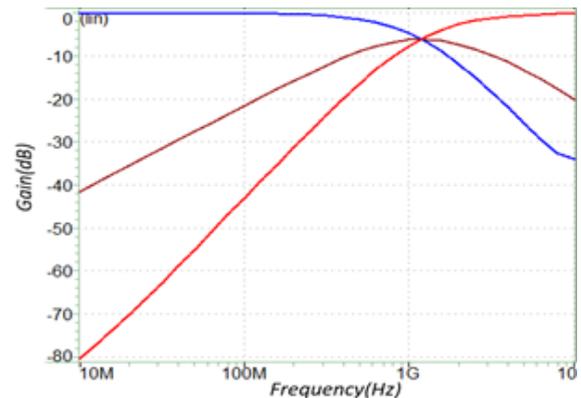


Figure 7. Simulated Gain Frequency response (in dB) for band pass , low pass and high pass filter with control word (k) [a2 a1 a0] = [0 1 1]

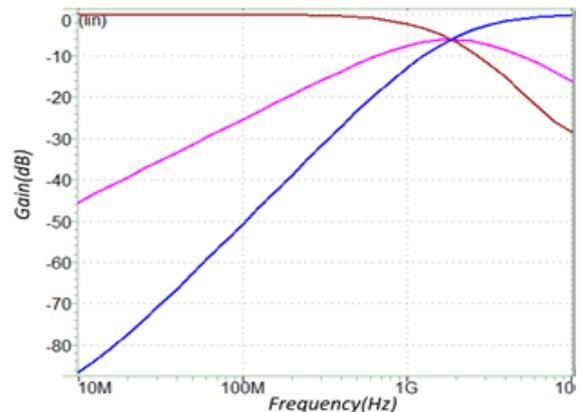


Figure 8. Simulated Gain Frequency response (in dB) for band pass , low pass and high pass filter with control word (k) [a2 a1 a0] = [1 1 1]

TABLE 3. Results of Sensitivity Analysis

Sensitivity	Value	Sensitivity	Value
$S_{C1}^{\omega_0}$	-0.5	S_{C1}^Q	+0.5
$S_{C2}^{\omega_0}$	-0.5	S_{C2}^Q	-0.5
$S_{G1}^{\omega_0}$	+0.5	S_{G1}^Q	+0.5
$S_{G2}^{\omega_0}$	+0.5	S_{G2}^Q	+0.5

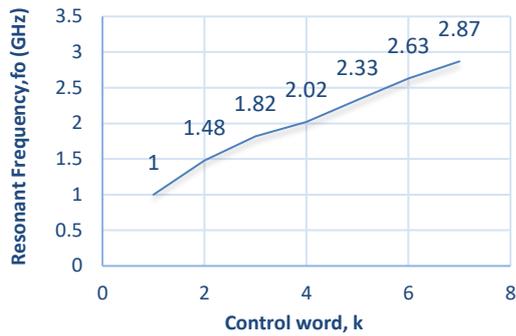


Figure 9. Variation in resonant frequency with digital control word of BPF

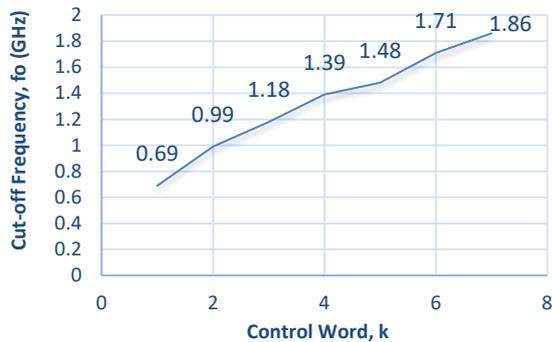


Figure 10. Variation of Cut-off frequency with digital control word of LPF

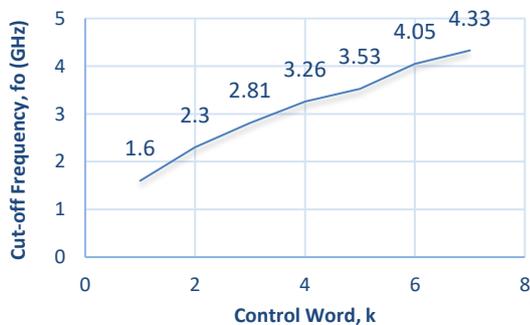


Figure 11. Variation of cut-off frequency with digital control word of HPF

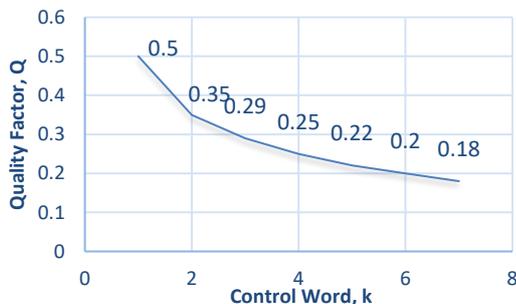


Figure 12. Variation in Quality factor with digital control word

TABLE 4. Comparative analysis with other circuits

Parameters	CNFET based multifunctional filter	Reference No. 24	Reference No. 25	Reference No. 26
Realizations	LPF, HPF, BPF	LPF, HPF, BPF, BRF, APF	LPF, HPF, BPF, BRF	LPF, HPF, BPF, BRF
Cut-off Frequency	1.08 Ghz	100 KHz	8.0025 MHz	100 KHz
Number of DVCC used	One	Two	One	One
Number of passive components	Five	Five	Four	Five
Resistance at port Y ₁ and Y ₂	6.2 Ohms	NA	NA	NA
Resistance at port X	275 Ohms	NA	NA	NA
Sensitivity	<1	<1	NA	<1

10. CONCLUSION

This paper proposes a digitally reconfigurable CNFET based multifunctional filter. The paper contributes by designing a filter using optimized carbon nanotube field effect transistors, which results in a resonant frequency of much higher order (GHz range). Furthermore the tunability factor has also been incorporated using Current Summing Network (CSN) and the simulation results are in accordance to the theory. The cut off frequencies of Band pass, Low pass and High pass is varied by varying the control word from [0 0 1] to [1 1 1]. It can be seen that cut off frequency of the filter is changed without changing any passive component present in the circuit. Due to control word the cut off frequency is varies from (1 GHz to 2.87 GHz) for band pass filter, (0.69 GHz to 1.86 GHz) for low pass filter and (1.6 GHz to 4.33 GHz). For practical considerations sensitivity analysis has also been performed on the circuit parameters with reference to passive components and the results lie well within the tolerant ranges. The comparative analysis with other similar circuits available in literature has also been performed. The circuit is expected to found use in the domain of high frequency low voltage analog signal processing.

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Persian Abstract

چکیده

با ادامه مقیاس بندی، ترانزیستورهای اثر نانولوله کربنی (CNFET) به عنوان کاندیداهای احتمالی برای رفع نقایص مربوط به مقیاس ترانزیستورهای تکمیلی فلز اکسید - نیمه هادی (CMOS) در نظر گرفته می شوند. در این مقاله یک فیلتر چند منظوره دو کاره مبتنی بر CNFET با قابلیت تنظیم مجدد دیجیتالی با استفاده از یک نوار نقاله جریان ولتاژ دیفرانسیل مبتنی بر CNFET (DVCC) در گره فناوری ۳۲ نانومتر ارائه شده است. این مدار از یک بلوک DVCC مبتنی بر CNFET به همراه آرایش مقاومت ها و خازن های کمی استفاده می کند. مدار فیلتر چند منظوره پیکربندی مجدد دیجیتالی با استفاده از یک توپولوژی می تواند پیکربندی فیلترهای کم گذر، بالا گذر و باند گذر قابل برنامه ریزی را بدست آورد. فیلتر چند منظوره مبتنی بر CNFET فرکانس طنینی از مرتبه گیگاهرتز را بدست می آورد. علاوه بر این، کنترل دیجیتالی ۳ بیتی پارامترهای فیلتر چند منظوره طراحی شده یعنی عامل کیفیت (Qo) و فرکانس تشدید با استفاده از شبکه جمع بندی فعلی (CSN) امکان پذیر شده است. حساسیت و تجزیه و تحلیل مقایسه ای نیز انجام شده است. مدار با منبع ولتاژ پایین ۰.۹ ولت با استفاده از برنامه شبیه سازی Hewlett با محیط مدار مجتمع (HSPIC) در گره فناوری ۳۲ نانومتر شبیه سازی شده است. نتایج شبیه سازی به دست آمده با تجزیه و تحلیل نظری همگام است.
