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Fast Grid Voltage Synchronization using Modified Frequency-locked Loop in Single Phase Grid-connected Power Systems

H. Hassanpour*, M. Ehsanian

Faculty of Electrical Engineering, K. N. Toosi University of Technology, Tehran, Iran

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ABSTRACT

One of the critical components for the efficient operation of single-phase grid-connected converters is the synchronization unit. This paper presents a fast and adaptive phase-locked loop (PLL) structure that ameliorates the dynamic response of the estimated frequency and amplitude for grid-connected single-phase power systems. The second-order generalized integrator (SOGI) with a novel frequency-locked loop (FLL) is utilized which contains a DC offset rejection loop. The proposed method not only eliminates the transient response of the estimated frequency which is produced by FLL in grid voltage phase angle jumps, but also improves the PLL dynamic characteristics. The whole system has been simulated in MATLAB Simulink environment where a very small settling time for the estimated frequency of the FLL has been achieved. Therefore, it will improve the whole dynamic parameters of the system. Based on the simulation results, the settling time for the estimated frequency and amplitude are 22 and 10 ms, respectively.

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1. INTRODUCTION

Single-phase grid-connected systems have gained substantial popularity in recent years. They are progressively utilized in numerous applications such as low power renewable energy resources [1-5]. One of the pivotal components for efficient operation of these systems is the synchronization unit. There is a multitude of synchronization methods in literature to monitor the grid voltage [6-8]. These units are responsible for the connection of the grid to the converter so that a unity power factor can be achieved. It is worth to note that phase, frequency, and amplitude are the other crucial information of the grid voltage for generating the reference current [9].

The most widespread technique of the synchronization is the Phase-Locked Loop (PLL) [10, 11]. The structures of PLLs that are presented in the literature, can generally be categorized into two classes: power-based PLLs (pPLLs) and quadrature signal generation PLLs (QSG-PLLs) [12]. In the pPLLs due to the presence of the multiplier, there are always second-order harmonic components [13, 14]. Therefore, the use of QSG-PLLs is more common than their pPLL counterparts [15-17]. The QSG-PLLs are a single-phase version of the synchronous reference frame (SRF), which are conventionally a three-phase PLL [18]. The predominant difference among the QSG-PLLs lies in their orthogonal signal generator (OSG) units which are responsible for generating a quadrature signal along with the PLL input signal [19]. There are various methods to generate the orthogonal signals, such as transport delay, Hilbert transformation, inverse park transformation, and filter base OSG [11]. All of these techniques have a suitable transient response, while they suffer from some weaknesses, such as frequency dependency, complexity, time-varying behavior, and inappropriate filtering.

The second-order generalized integrator (SOGI) method is another technique for generating quadrature signal which was introduced in literature [20] for the first time. The main issue of the SOGI is its frequency dependence, in which the estimated frequency is fed back to the SOGI blocks. Numerous techniques are presented in order to solve this problem. For instance, fixed

*Corresponding Author Institutional Email: h.hassanpour@email.kntu.ac.ir (H. Hassanpour)

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frequency is one of the methods that is used to overcome this issue [21]. Rodríguez et al. [22], presented a novel structure which has employed frequency locked loop (FLL) to estimate the frequency instead of the utilization of the feedback loop [23-25]. Although in this method, the dynamics of PLL are improved [25-28], the estimated frequency is dependent on the phase jumps of the PLL input signal.

One of the critical problems in the frequency estimation of the PLLs is the low transient response in the presence of the phase angle error. A verity of reasons like system malfunctioning could be the important origin of this error. Since the FLL is settled in the PLL input section, it will increase the dependency of the estimated frequency to the PLL input signal variations. Therefore, if a phase jump occurs in the input signal, then it will directly be imported to the FLL.

The existence of DC offset in the input signal is another challenge which needs to be considered in the design of the PLL [11, 29]. Several factors might be the cause of the DC offset, such as DC offset of voltage sensors, data converters, and grid faults [9, 30]. One of the major deficiencies of the SOGI and the SOGI-FLL is the absence of a DC offset rejection loop in their structures. A multitude of techniques has been suggested in the literature to eliminate the DC offset [31, 32]. A common method which is used to such issue in SOGI structure is utilization of the modified SOGI [33, 34]. It is worth to mention that a comprehensive analysis of the DC offset rejection techniques in SOGI-PLLs has been discussed in literature [35].

In this paper, a novel adaptive method is presented which removes the effect of the phase angle error for the input signal in the estimation process of the frequency. It also eliminates the DC offset rejection of the input signal in a very suitable manner. The proposed method makes some changes in the structure of the SOGI-FLL so that it can enhance the transient response for the estimated frequency signal. With the minimization of the estimated signal error, the dynamic responses of the PLL are improved. Additionally, a DC offset rejection is utilized to cancel the offset of the input signal. The corresponding relations for the proposed structure are discussed completely, where the correctness of the relations was demonstrated by the simulations.

This paper is organized as follows: section 2 introduces the SOGI-PLL and its performance; and after that, the FLL block is described along with its problems. The DC offset rejection loop is also presented in this section. Section 3 proposes a solution to improve the FLL units which are used to enhance the PLL dynamic performance. This section formulates the proposed method. Simulation results and comparisons are presented in section 5. Section 6 contains the conclusions.

2. STRUCTURE OF SOGI-FLL WITH DC-OFFSET REJECTION

The general structure of the QSG-PLL is shown in Figure 1, where v_i is the input signal of the PLL. v_α and v_β demonstrate the quadrature signal and V represents the amplitude of the input voltage. Moreover, ω_n, $\hat{\theta}$, and $\hat{\omega}$ mark the nominal frequency, estimated phase angle, and the estimated frequency, respectively. As it can be observed, the QSG structure consists of an OSG block. In addition, the park transformation is utilized in their structure for converting $\alpha\beta$ to dq frame. The SOGI block will be used as an OSG block.

Figure 2 illustrates the whole structure of a SOGI in which the two orthogonal signals (v_α, v_β) have been produced in its output. v_α contains the same phase with the input signal, where its amplitude is equal to the input voltage amplitude. On the other hand, v_β has a 90° phase shift and the same amplitude with the input signal. The two closed-loop transfer functions of the SOGI will abide by Rodríguez et al. [22]:

$$H_\alpha(s) = \frac{v_\alpha(s)}{v_i(s)} = \frac{k\hat{\omega}s}{s^2+k\hat{\omega}s+\hat{\omega}^2} \quad (1)$$

$$H_\beta(s) = \frac{v_\beta(s)}{v_i(s)} = \frac{k\hat{\omega}^2}{s^2+k\hat{\omega}s+\hat{\omega}^2} \quad (2)$$

Where $\hat{\omega}$ is resonance frequency which is fed back from PLL output (before integrator in Figure 1), and k is the gain which affects the bandwidth of the closed-loop SOGI. It is equal to the damping ratio multiplied by two ($k = 2\xi$). The bode plot of $H_\alpha(s)$ and $H_\beta(s)$ for different values of $k = 0.1,\ 0.6,\ 2.2$ are shown in Figure 3. As it can be observed from the Figures 3(a) and 3(b), $H_\alpha(s)$ and $H_\beta(s)$ behave like a band-pass and a low-pass filter, respectively. For $H_\alpha(s)$, $\hat{\omega}$ is the central frequency, and because of the small bandwidth of the filter, the larger value of k provides better filtering capability. If the central frequency ($\hat{\omega}$) of the band-pass filter is considered equal to the nominal frequency ω_n ($\hat{\omega}$=ω_n), v_α will be identical to the input signal in steady-state ($v_\alpha = v_i$). Likewise, by the aforementioned assumption, v_β will be equal to v_i with a 90° phase shift. As a result, the SOGI structure can produce two orthogonal signals which then will be filtered.

In SOGI-PLL the estimated frequency is fed back to SOGI block, which causes the frequency dependency. Therefore, the transient response of the estimated frequency increases. In contrast, for SOGI-FLL the estimated frequency is prepared by the FLL block, and there is no need for a feedback loop, so the settling time of the estimated frequency is lower than the SOGI-PLL [23]. In order to solve this issue, the FLL block is added to the structure which provides the capability of generating the estimated frequency without using feedback loop. Figure 1(a) illustrates the SOGI-FLL

topology where e_v and e_f are the voltage and frequency errors, respectively, and γ represents the gain. The transfer function of e_v/v_i is as follows[20]:

$$\frac{e_v(s)}{v_i(s)} = \frac{s^2+\hat{\omega}^2}{s^2+k\hat{\omega}s+\hat{\omega}^2} \quad (3)$$

As the loop of SOGI-FLL demonstrates very nonlinear characteristics, we cannot perform linear analyses to determine the value of γ. Complete dynamic analysis along with the techniques of linearity enhancement for the SOGI-FLL are available in literature [22]. The linear loop of FLL is shown in Figure 4(b) where Γ is a constant coefficient, and can be obtained using following expression [22]:

$$\Gamma = \gamma \frac{V^2}{k\hat{\omega}} \quad (4)$$

The closed-loop transfer function of Figure 4(b) can be written as follows:

$$\frac{\hat{\omega}}{\omega} = \frac{\Gamma}{s+\Gamma} \quad (5)$$

It can be concluded from Equation (5) that the dynamic response of the FLL is only dependent to the value of Γ. Settling time for the FLL is approximately equal to:

$$t_s = \frac{5}{\Gamma} \quad (6)$$

By substituting the value of Γ from Equation (4) into Equation (6), the settling time will be:

$$t_s = \frac{5k\hat{\omega}}{\gamma V^2} \quad (7)$$

Offset DC rejection is also a critical issue in the design of the PLLs. As it was shown in the bode plot of Figure 3(b) , the ratio of $\frac{v_\beta}{v_i}(s)$ cannot filter the DC component. The value of $\frac{v_\beta}{v_i}(s)$ at $\omega = 0$ is equal to:

$$\frac{v_\beta}{v_i}(j0) = 1 \quad (8)$$

Equation (8) illustrates that if the input voltage v_i has a DC component, then it will deteriorate v_β. The modified SOGI is utilized to solve this problem, which is illustrated in Figure 5(a) where v_{DC} is the estimated DC component of the input signal, and k_{DC} is the gain of the DC offset rejection loop. This technique uses an integrator and a gain coefficient of $k_{DC}\hat{\omega}$ to estimate the DC component of the input signal. Afterwards, this estimated DC component is subtracted from the input signal to enhance the system capability in the DC offset rejection.

The corresponding transfer functions of SOGI with DC offset rejection loop are:

$$\frac{v_\alpha(s)}{v_i(s)} = \frac{k_{DC}\hat{\omega}s^2}{s^3+(k+k_{DC})\hat{\omega}s^2+\hat{\omega}^2 s+k_{DC}\hat{\omega}^3} \quad (9)$$

$$\frac{v_\beta(s)}{v_i(s)} = \frac{k_{DC}\hat{\omega}^2 s}{s^3+(k+k_{DC})\hat{\omega}s^2+\hat{\omega}^2 s+k_{DC}\hat{\omega}^3} \quad (10)$$

$$\frac{v_{DC}(s)}{v_i(s)} = \frac{k_{DC}\hat{\omega}(s^2+\hat{\omega}^2)}{s^3+(k+k_{DC})\hat{\omega}s^2+\hat{\omega}^2 s+k_{DC}\hat{\omega}^3} \quad (11)$$

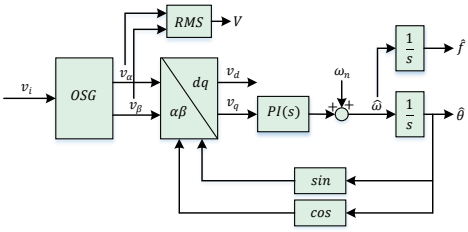


Figure 1. Diagram of a standard QSG-PLL

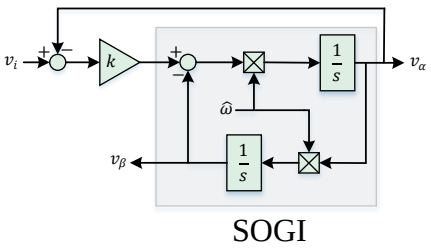
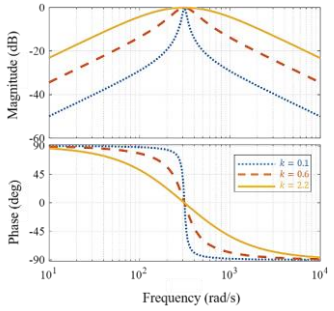
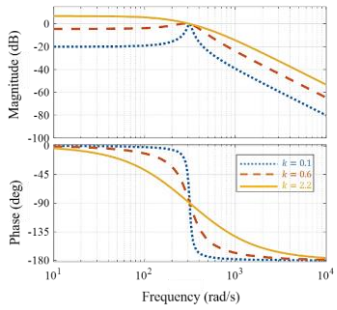


Figure 2. Structure of SOGI



(a)



(b)

Figure 3. Bode diagram of SOGI closed-loop transfer function. a)$\boldsymbol{H_\alpha(s) = \frac{v_\alpha(s)}{v_i(s)}}$, b)$\boldsymbol{H_\beta(s) = \frac{v_\beta(s)}{v_i(s)}}$

The bode diagrams of the above transfer functions with the gains of $k = \sqrt{2}$ and $k_{DC} = 0 \cdot 4$ are demonstrated in Figure 5(b). As it is visible, the behavior of v_{DC}/v_i is similar to a low pass filter which makes the v_β/v_i characteristic behave like a band-pass filter. On the other hand, the ratio of v_α/v_i is a band-pass filter just as before.

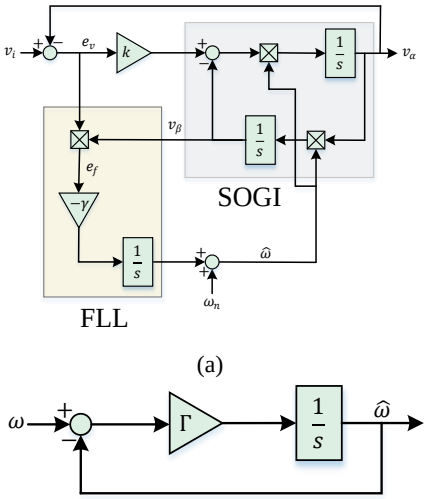
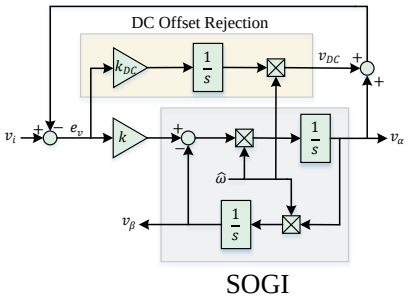


Figure 4. Structure of SOGI with FLL loop. a) Complete structure of SOGI-FLL, b) Simplified linear loop of FLL



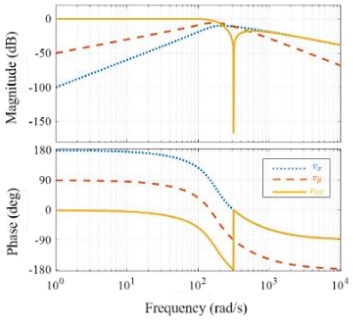


Figure 5. a) Structure of SOGI with DC offset rejection loop, b) Bode diagram of $\frac{v_\alpha}{v_i}, \frac{v_\beta}{v_i}, \frac{v_{DC}}{v_i}$

3. THE PROPOSED STRUCTURE

As it was mentioned before, utilization of an FLL results in a procedure for the estimation of the frequency. The virtue of this method is an independent estimation of the frequency which leads to a suitable transient response. Because the FLL is placed in the input of structure, changes of the input voltage can cause the unsatisfactory operation for the system. The phase jump of the input voltage is one of the changes that might happen. If a change occurs in the phase of the input signal, it will immediately be imported to the FLL unit. In other words, when the phase angle of the input voltage changes, the frequency error will no longer be equal to zero ($e_f \neq 0$). In order to illustrate this issue, a simulation for the SOGI-FLL structure is performed which is shown in Figure 6. In this test, a 45° phase jump in the time of $0 \cdot 1\ s$ is applied to the input voltage, and as a consequence, a considerable transient interval takes place in the estimated frequency response.

To solve the problem of frequency dependency, the structure of Figure 7 is proposed. In this structure, gain normalization is done in the first step. Then, the factor of Te^2 is added to the denominator of $\frac{1}{v_\alpha^2+v_\beta^2}$. When a phase

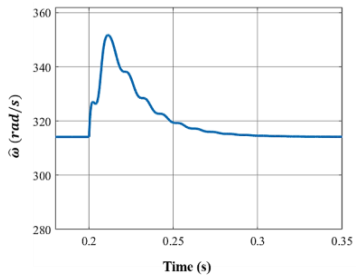


Figure 6. Transient response of FLL output signal

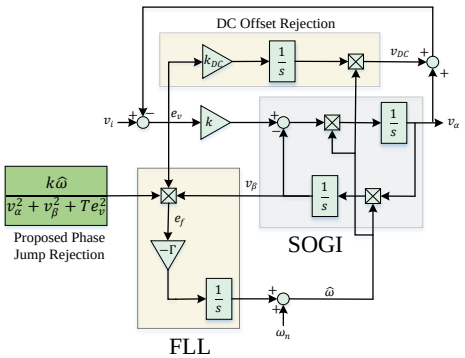
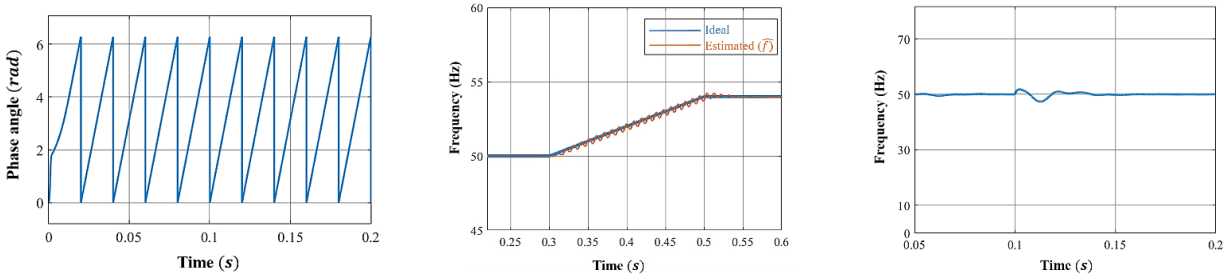


Figure 7. Proposed structure



(a) (b) **(c)**

Figure 8. Performance of proposed structure. a) Phase angle of proposed structure, b) Estimated and ideal grid frequency, c) Estimated frequency with the presence of DC offset

jump occurs in the input signal, it leads to the voltage error (e_v). In the conventional SOGI-FLL structure e_v was multiplied by v_β to result the frequency error (e_f). However, in the proposed structure e_v is multiplied by a third term $\frac{k\hat{\omega}}{v_\alpha^2+v_\beta^2+Te_v^2}$. By taking into account that the term Te_v^2 is in the denominator, the effect of e_v on e_f will be suppressed, especially when a large value of T is chosen. By assuming that the input signal is as follow:

$$v_i(t) = V\cos(\omega t) \tag{12}$$

The two quadrature signals will be:

$$v_\alpha(t) = V\cos(\omega t) \tag{13}$$

$$v_\beta(t) = V\sin(\omega t) \tag{14}$$

Now, if a phase jump with the value of φ occurs in the input voltage, Equation (12) will change as:

$$v_i(t) = V\cos(\omega t + \varphi) \tag{15}$$

At the first moment, the phase change is not reflected in the quadrature signals, and Equation (13) as well as Equation (14) will remain unchanged. Hence, the frequency error can be written as follows:

$$e_f = v_\beta \times e_v = (V\sin(\omega t)) \times (v_i - v_\alpha) \tag{16}$$

By substituting Equations (13) and (14) into Equation (16), the frequency error will be calculated as follows:

$$e_f = (V\sin(\omega t)) \times (V\cos(\omega t + \varphi) - V\cos(\omega t)) \tag{17}$$

With the simplification of Equation (17), the average frequency error can be written as follows:

$$\bar{e_f} = -\frac{1}{2}\sin\varphi \tag{18}$$

The estimated frequency will be:

$$\hat{\omega} = \frac{1}{s}\left[\frac{k\hat{\omega}}{v_\alpha^2+v_\beta^2+Te_v^2} \times -\frac{1}{2}\sin(\varphi) \times -\Gamma\right] \tag{19}$$

As it can be observed in Equation (19), larger value of T will result in a corresponding smaller value for $\hat{\omega}$. Therefore, by considering Equation (7), the lower value of $\hat{\omega}$ will decrease the settling time to the desired amount.

4. SIMULATION RESULTS

4. 1. Performance of The Proposed Structure

The whole system is simulated in the MATLAB Simulink environment where the parameters of the systems are summarized in Table 1.

Figure 8(a) shows the estimated phase angle of the proposed PLL. It is obvious that the phase angle has periodic feature. Moreover, as the results indicate, the PLL works correctly. In Figure 8(b) the proposed structure is tested by means of a ramp change for the grid frequency where the grid frequency changes from $50\ Hz$ to $54\ Hz$ with a slope of $20\ Hz/s$. As it can be observed, the estimated frequency ($\hat{f}$) accurately follows the grid frequency where the grid frequency is shown with the blue plot, and the red plot represents the estimated frequency. Figure 8(c) shows the estimated frequency when the input grid voltage has a DC offset, which is a step change having the value equal to the 10 percent of the grid voltage amplitude.

TABLE 1. System parameters

Item	Parameter	Value
Grid voltage Amplitude	V	$220\ V$ (RMS)
Grid Frequency	f	$50\ Hz$
PLL Gain	k	$\sqrt{2}$
PI Proportional Gain	k_p	7878
PI Integral Gain	k_i	$137 \cdot 5$
FLL Gain	Γ	50
Proposed Phase Jump Rejection Parameter	T	300
Offset DC Rejection Gain	k_{DC}	$0 \cdot 4$

4. 2. Comparison In this section, SOGI, SOGI-FLL, and the proposed structures are compared. In the first test, the transient response of the estimated frequency between the conventional and the proposed FLL is compared. For this test, a step change with a value of 45° in $0.1\ s$ is applied to the phase of the input grid voltage. The transient response for the two structures is demonstrated in Figure 9 where the result shows that the estimated frequency of the conventional FLL has a considerable transient value. Also, its overshoot and settling time are $38\ Rad/s$ and $49\ ms$, respectively. On the other side, the estimated frequency of the proposed FLL, has $1\ Rad/s$ overshoot while the corresponding settling time is almost zero. The obtained characteristics of the conventional and proposed FLL are summarized in TABLE .

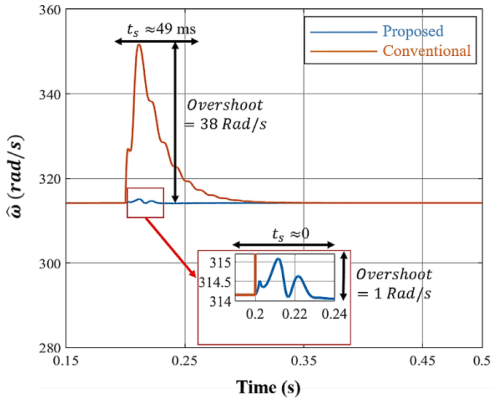


Figure 9. Output signal of FLL for conventional FLL and proposed FLL

TABLE 2. Comparison of conventional fll and proposed fll

Structure	Overshoot of $\hat{\omega}$	Settling Time of $\hat{\omega}$
Conventional FLL	$38\ Rad/s$	$49\ ms$
Proposed FLL	$1\ Rad/s$	zero

In another test, the estimated amplitude ($\hat{V}$) and frequency ($\hat{f}$) for the three structures are compared. All simulations have been performed in the same environment, where the corresponding parameters are shown in Table 1. Figure 10(a) shows the estimated frequency for SOGI which its settling time is equal to $157\ ms$. Also, Figure 10(b) shows the estimated amplitude for SOGI structure where its settling time is $140\ ms$. Figures 10 (c) and**Figure** 10(d) illustrate the estimated frequency and amplitude for the SOGI-FLL structure. They illustrate that the settling time is $50\ ms$ for the estimated frequency and $55\ ms$ for the estimated amplitude. The achieved results of the proposed system are demonstrated at Figures 10(e) and 10(f). Figure10(e) shows the estimated frequency in which the settling time is equal to $22\ ms$. Figure10(f) shows the estimated amplitude, where the settling time is $10\ ms$. Table 3 exhibits a comparison among the three structures from the viewpoint of settling time. It is apparently clear that the dynamic characteristics of the proposed method are better than the counterpart structures.

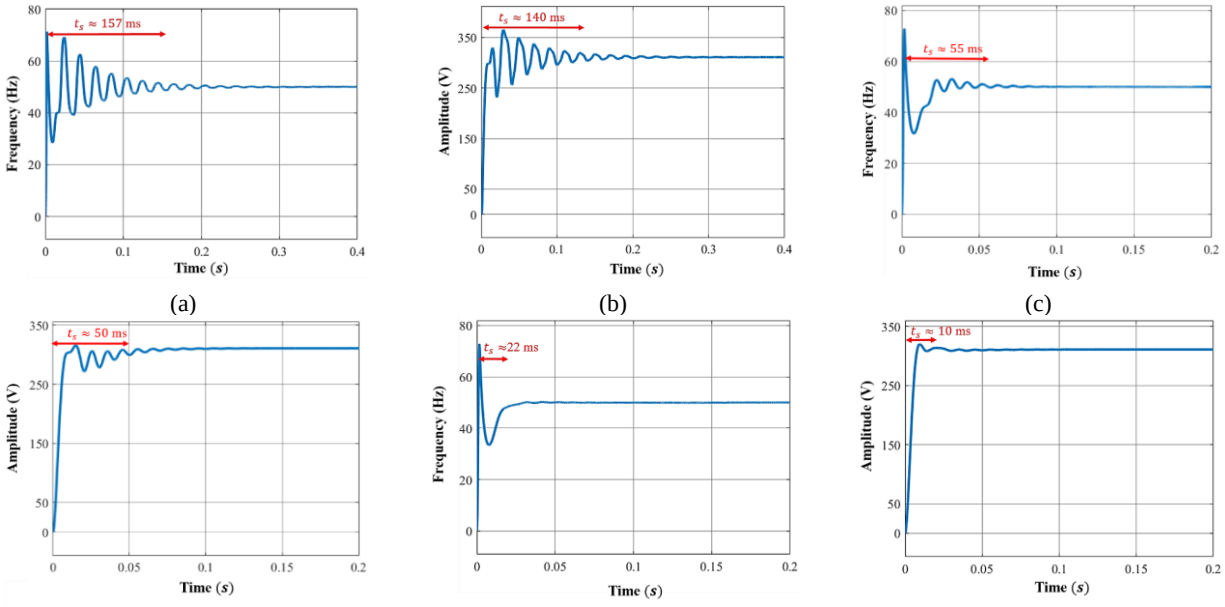


Figure 10. Dynamic performance of SOGI, SOGI-FLL, and proposed method. a) estimated frequency of SOGI, b) estimated amplitude of SOGI, c) estimated frequency of SOGI-FLL, d) estimated amplitude of SOGI-FLL, e) estimated frequency of proposed method, f) estimated amplitude of proposed method

TABLE 3. Comparison of sogi, sogi-fll, and proposed method

Structure	Settling Time of $\hat{V}$	Settling Time of $\hat{f}$
SOGI	140 ms	157 ms
SOGI-FLL	50 ms	55 ms
Proposed	10 ms	22 ms

5. CONCLUSION

The dynamic response of PLLs is a challenging issue in the design of the grid-connected single-phase power systems. A novel SOGI-FLL structure with DC offset rejection loop is introduced in this paper. The proposed mechanism solves the problem of the transient response produced by FLL in phase jumps of the grid voltage. From the viewpoint of the dynamic response, it completely removes the transient response. The simulations demonstrate the proper functionality of the system. Based on the results, the settling time for the estimated frequency along with the amplitude are $22ms$ and $10ms$, respectively.

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Persian Abstract

چکیده

یکی از اجزاء اصلی جهت عملکرد صحیح مبدل‌های تکفاز متصل به شبکه واحد همگام‌ساز است. این مقاله یک حلقه قفل فاز سریع و خود تطبیق ارائه می‌کند که پاسخ دینامیکی فرکانس و دامنه تخمین زده شده برای سیستم‌های قدرت تکفاز متصل به شبکه را بهبود می‌بخشد. انتگرال‌گیر تعمیم یافته مرتبه دوم (SOGI) به همراه حلقه قفل فرکانس مورد استفاده قرار گرفته است که شامل حلقه حذف‌کننده آفست DC نیز می‌باشد. روش ارائه شده نه تنها پاسخ گذرای فرکانس تخمین زده شده تولیدی توسط حلقه قفل فرکانس به ازای پرش‌های زاویه فاز ولتاژ شبکه را حذف می‌کند، بلکه ویژگی‌های دینامیکی حلقه قفل فاز را نیز بهبود می‌بخشد. تمامی سیستم در محیط متلب شبیه‌سازی شده، به طوری که زمان نشست بسیار کوچک برای حلقه قفل فرکانس بدست آمده است. لذا تمامی پارامترهای دینامیکی سیستم بهبود یافته است. بر اساس نتایج شبیه‌سازی، زمان نشست فرکانس و دامنه تخمین زده شده به ترتیب ۲۲ و ۱۰ میلی ثانیه بدست آمده‌اند.