A Temperature Compensation Voltage Controlled Oscillator Using a Complementary to Absolute Temperature Voltage Reference

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1. INTRODUCTION

Frequency drift over temperature variations is a crucial design consideration for voltage controlled oscillator (VCO) circuits in RF systems because transistors' parameters, on-chip inductor resistances, and capacitors are highly sensitive to temperature fluctuations [1]. Temperature compensation for the VCO oscillation frequency is a critical issue for RF designers. Also, it is important to improve other parameters of VCO like power consumption and phase noise after frequency compensating over the temperature range. The phase noise and power consumption are two critical issues in designing VCO [2]-[5].

Several methods are proposed to compensate frequency drift over temperature [6]-[11]. Placing VCO in a synthesizer loop is a solution for this problem [12]. The correcting nature of the synthesizer can decrease the frequency drift of VCO in closed loop condition, but it is limited by the selection of VCO gain (KVCO). Higher KVCO can provide temperature stability requirement, but it degrades the phase noise performance due to AM to PM noise conversion. Reference [6] presents an LC VCO with a MOS inversion varactor array with two voltage bias generators to compensate frequency drift. In the bias circuit a BJT and a resistor are used to produce the Vref and a BJT is used to track the frequency changes of the other BJT. This circuit fixes frequency by using varactor array. This method suffers from high power consumption and occupies a large area because of compensation circuit. A proportional to absolute temperature (PTAT) voltage reference to compensate oscillation frequency drift has been presented in [7]. In this method, a Widlar bandgap reference has been used. BJT transistors have been applied to the first stage of the reference and MOS transistors have been used in the second stage to mirror the PTAT current. This PTAT current has been applied to a resistor and PTAT voltage has been produced and then it has biased the 2 varactors.
to fix the frequency drift. This Reference has used BiCMOS Technology. Therefore, the cost has increased. By employing a complementary to absolute temperature (CTAT) voltage reference in [8], the frequency drift has been compensated. To design the CTAT voltage, an opamp has been used to fix the voltage deviation and then the output of the opamp has been connected to a MOS transistor for producing the CTAT current. This current has been passed through a resistor to produce a CTAT voltage. This circuit could have compensated the frequency drift but it suffers from poor phase noise performance.

A temperature compensation technique using constant-biased varactors has been presented in reference [9]. In this circuit to compensate the frequency drift, PMOS varactors have been used. According to this reference, PMOS varactors have better characteristics than NMOS varactors. This circuit has a good performance but the frequency of the circuit is low. Reference [10] has presented an LC cross-coupled VCO. To design this VCO, T-lines have been used instead of inductors and the size of circuit has decreased. But the circuit suffers from high power consumption and poor phase noise.

Most designs in the field of VCO temperature compensation have been performed at frequencies less than 10 GHz. Therefore, it is extremely important to design a VCO at high frequencies with temperature compensation. The other important issue in designing a VCO is the structure of its circuit. Cross-Coupled pair and Colpitts structures are the two mostly used structures due to their good performance like phase noise and dc power consumption at high frequencies. Therefore, it is important to design a high frequency VCO with good phase noise and low power consumption. Also, it is critical to have a stable frequency and performance over a wide temperature range.

In this paper, a temperature compensation VCO with good noise performance at 24.35 GHz is presented. To achieve good temperature performance, a CTAT voltage reference is applied to varactors. This helps the circuit to be stable over a wide temperature range and it fixes the frequency changes with a good approximation. By using this compensation circuit, the resulting drift from center frequency is 11.5 PPM/C. Besides, to achieve good performance, combination of Cross-Coupled pair and Colpitts structures are used. This circuit is suitable for military fields. Because it is stable over a wide temperature range.

The rest of the paper is organized as follows: the proposed VCO and temperature drift reasons are introduced in Section 2. The temperature compensation circuit is presented in Section 3. Design consideration is proposed in Section 4. Section 5 discusses simulation results and compares it with the results of prior works. Finally, conclusion is provided in Section 6.

2. THE MAIN PART OF VCO AND FREQUENCY DRIFT CONSIDERATION

2.1 VCO Core

The schematic circuit of proposed VCO has been shown in Figure 1. The proposed VCO includes Cross-Coupled pair and Colpitts structures. The Cross-Coupled pair is used due to its better start-up condition and low phase noise performance [13]. Also, by using Colpitts structure, DC power consumption has been reduced [13]. To have a better start-up condition, two inductors have been used between Cross-Coupled pair and Colpitts structures [14]. These inductors enhance the interesting gain of transistors and thus, the negative conductance increases leading to robust start-up condition. Moreover, these inductors reduce the noise effect of Cross-Coupled pair by resonating with parasitic capacitors of the transistor at oscillation frequency. Therefore, phase noise performance is improved. In addition, a simple capacitor bank and two varactors have been applied to have an acceptable tuning range.

Figure 1. The proposed VCO
To improve the start-up condition, a voltage is applied to bulk of transistors M1-4. To prove this claim, the transconductance gain is obtained as

$$g_m = \mu_n C_{ox} \frac{\omega}{L} \left[ V_{GS} - V_{tho} - \gamma \sqrt{|V_{th}-\frac{2}{3}}| \right]$$  \(1\)

where, \(\mu_n\), \(C_{ox}\), \(\frac{\omega}{L}\), \(V_{GS}\), \(V_{tho}\), \(\gamma\), and \(\phi\) are mobility of electrons, silicon dioxide capacitor, size of transistor, gate-source voltage, bulk-source voltage, threshold voltage \((V_{tho}=0)\), bulk threshold parameter, and surface potential at strong inversion, respectively.

According to \(1\), by applying a voltage to the bulk of transistors, the transconductance gain increases, and subsequently start-up condition improves.

The most important part of the proposed VCO is temperature compensation circuit. To compensate frequency drift over temperature, two varactors and a CTAT voltage reference have been used. This CTAT voltage reference produces a negative slope voltage over the temperature range and biases the varactors \(C_{var}\) and \(C_{act}\). The circuit design and its operation are thoroughly explained in section 3.

Thus, the total capacitance is formed by the series combination of \(C_A\) and parasitic diode capacitor \(C_{db}\) (or \(C_B\) and parasitic diode capacitor \(C_{sb}\)). In this case, the total capacitance is determined by the parasitic diode capacitors. The parasitic diode capacitance is defined as [15]:

$$C_{db} = C_{sb} = \frac{C_{jo}}{1 + \frac{V_{R}}{V_{o}}}$$  \(2\)

where, \(C_{jo}\), \(V_{R}\), and \(V_{o}\) are PN junction capacitance, reverse bias voltage of PN junction and built-in potential, respectively. Since \(V_{o}\) varies with temperature by -0.2 V/°C, the parasitic capacitance changes over temperature. Thus, according to “\(f = \frac{1}{2\pi \sqrt{LC}}\)”, the VCO does not oscillate at the desired frequency range due to variation of capacitance.

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2.2. Transistors

Transistor has the most effect on frequency drift due to the variation of its transconductance gain \((g_m)\), threshold voltage \((V_{th})\), mobility of electrons and holes \((\mu_n, \mu_p)\), and parasitic capacitors \(g_m, V_{th}, \mu_n, \mu_p\) and \(g_{m}V_{th} = \alpha(T-27)\) are obtained as follows [15]:

$$g_m = \mu_n C_{ox} \frac{\omega}{L} (V_{GS} - V_{th})$$  \(3\)

$$V_{th} = V_{tho} - \alpha(T-27)$$  \(4\)
\[ \mu(T) = \mu(T=27) \left( \frac{T}{27} \right)^\frac{3}{2} \]  

(5)

where, \( \mu_n \), \( C_{ox} \), \( \omega \), \( V_{GS} \), \( V_{th} \), \( \alpha \), and \( T \) are mobility of electrons, silicon dioxide capacitor, size of transistor, Gate-Source voltage, threshold voltage, temperature coefficient of threshold voltage, and ambient temperature, respectively.

According to (3)-(5), by increasing temperature, the threshold voltage and mobility are reduced and subsequently \( g_m \) decreases. The reduction in \( g_m \) changes the level of harmonic distortion and oscillation frequency [7]. The simulated \( g_m \) of NMOS transistor is demonstrated in Figure 4. As can be seen, the \( g_m \) decrement is very significant. The parameter \( g_m \) has a temperature coefficient of 1250 PPM/°C over a temperature range of -40-120 °C.

3. PROPOSED TEMPERATURE COMPENSATED CIRCUIT

Equations (2)-(5) show that the frequency increases by enhancing the temperature. Figure 5 shows the simulated frequency of the VCO without temperature compensation. As shown in Figure 5, the temperature drift is about 130 MHz. Also, the temperature coefficient of frequency is about 33.45 PPM/°C.

According to \( f = \frac{1}{2\pi\sqrt{LC}} \), the oscillation frequency, which is a drift from the desired frequency, can be compensated by changing the total inductance or capacitance seen from the output node. Changing the inductance is very difficult in integrated circuits. Also, inductor occupies a very large area in an IC. Thus, the best choice is changing the capacitance. Figure 6 describes the effect of temperature on frequency and its compensation. If the temperature rises and consequently it causes drop in the center frequency; it needs to decrease \( C_{\text{total}} \) for compensation. Also, if the temperature rises and consequently it causes rise in the center frequency; it needs to increase \( C_{\text{total}} \) for compensation. According to Figure 5 and 6, to compensate drift frequency, a temperature dependent voltage reference is needed to bias the varactors and change their capacitance and subsequently fix the oscillation frequency.

The proposed temperature compensation circuit has been depicted in Figure 7. The voltage differences of the diode connections (transistor \( M_{1,2} \)) which are located at the top of the circuit produce a PTAT voltage. This PTAT voltage is applied to another diode connection (\( M_{3} \)) and this transistor is biased. The drain voltage of transistor \( M_{3} \) becomes CTAT voltage. In addition, by mirroring the current of \( M_{3} \), the drain voltage of the transistor \( M_{4} \) becomes CTAT. This voltage is applied to varactors and the values of varactors is enhanced. As mentioned, the frequency grew when the temperature was increased.
By employing a CTAT voltage circuit and biasing varactors with this CTAT voltage, the value of varactors augments and frequency increases. Therefore, the frequency drift over temperature is compensated.

4. DESIGN CONSIDERATIONS

4. 1. Sizes of Transistors The first important step in designing an oscillator is to obtain the sizes of the transistors. In VCO design, to determine the sizes of transistors, it is necessary to consider the currents of the transistors. Since the transistors are in the saturation region, the sizes of NMOS transistors is defined as (7) [13].

\[
\left( \frac{W}{L} \right)_n = \frac{2I_D}{\mu_n C_{ox} (V_{GS} - V_{th_n})}
\]

(7)

where, \( \left( \frac{W}{L} \right)_n \) is sizes of NMOS transistors, \( I_D \) is the drain current, \( \mu_n \) is the electron mobility, \( V_{th_n} \) is threshold voltages of NMOS, \( C_{ox} \) and \( V_{GS} \) are silicon dioxide capacitor and gate-source voltage.

4. 2. Inductors To calculate the main frequency, it is necessary to compute the inductance from the following equation [13]:

\[
L = \frac{1}{2\pi Q f_o}
\]

(8)

where, \( Q \) is the quality factor of the inductor, \( R_p \) is the equivalent parallel resistor of the inductor, and \( f_o \) is the center frequency. The quality factor and \( R_p \) depend on the technology that is used and the inductance can be calculated by considering their values.

4. 3. Oscillation Frequency and Start-Up Condition After calculating the size of transistors from (7), the produced parasitic capacitors of transistors should be considered, since these capacitors affect oscillating frequency and the start-up condition. Furthermore, the inductor parasitic capacitors should also be considered. Thus, it is necessary to estimate all parasitic capacitances.

4. 3. 1. Inductor Capacitors The inductors that are used in integrated circuits often have spiral form as shown in Figure 8 [14]. The equivalent circuit of these inductors is demonstrated in Figure 9 [15].

According to Figure 9, the values of capacitors, inductors, and resistors of this equivalent circuit are determined as follows. The values of inductors can be calculated as (9) [15].

\[
L = \frac{37.5 \mu H N^2 a^2}{11D-14a}
\]

(9)

where, \( \mu_0 \) is the vacuum permeability, \( N \) is the number of inductor turns, \( a \) is the distance from the center of the inductor to the middle of the windings and \( D \) is the diameter of windings. The values of capacitors can be obtained from (10), (11) and (12) [15].

\[
C_{ox} = \frac{W L \varepsilon_{ox}}{t_{ox}}
\]

(10)

\[
C_p = \frac{NW^2 \varepsilon_{ox}}{t_{ox}}
\]

(11)

\[
C_l = \frac{2}{WLC_{sub}}
\]

(12)

where, \( W, L, N, C_{sub}, \varepsilon_{ox}, \) and \( t_{ox} \) are metal width, total length of the spiral, number of turns, body capacitance, silicon dioxide electrical permittivity and thickness of the oxide, respectively.

The values of resistors can be calculated using (13) and (14) [15].

\[
R_x = \frac{L}{W_0 \varepsilon (1 - e^{-\delta})}
\]

(13)

\[
R_I = \frac{WLC_{sub}}{2}
\]

(14)

where, \( W, L, \sigma, C_{sub}, t, \) and \( \delta \) are metal width, total length of the spiral, conductivity of the metal, body capacitance, thickness of the metal and skin depth, respectively.

4. 3. 2. Transistor Capacitors Figure 10 shows the parasitic capacitors of the transistor. In RF design, it
is necessary to consider these capacitors. In application, gate-source capacitor and gate-drain capacitor are often considered, and other capacitors are neglected [15].

Since the transistors are in the saturation region, the values of these capacitors can be obtained as follows [15]:

\[ C_{GS} = C_{GSO} + \left( \frac{2}{3} \right) C_{ox} L W \]  
(15)

\[ C_{GD} = C_{GDO} - W \]  
(16)

where, \( C_{GD} \), \( C_{GS} \), \( C_{GSO} \), \( C_{GDO} \), and \( C_{ox} \) are gate-drain, gate-source, gate-source overlap, gate-drain overlap and oxide capacitances, respectively.

### 4.3.3. Oscillation Frequency Analysis

The simplified equivalent half-circuit of the proposed VCO is illustrated in Figure 11. \( C_{L1} \), \( C_{gd1} \), and \( C_{gd3} \) are the parasitic capacitor of the inductor, gate-drain capacitors of NMOS and PMOS transistor, respectively. To derive the operation frequency, the transfer function between \( V_o \) and \( V_i \) is defined as (17).

\[ V_o = \frac{g_m L_2 C_0 \omega + (C_i + C_0) \omega}{\left[ L_2 C_0 \omega^2 + (C_i + C_0) \omega \right]} \]  
(17)

where, \( C_i \) and \( C_0 \) are calculated as (18) and (19).

\[ C_i = C_{L1} + C_1 + C_{gd1} \]  
(18)

\[ C_0 = C_{L1} + C_{T1} + C_{gd3} + C_{T2} \]  
(19)

Oscillation frequency will occur if loop gain of the circuit is unity, with a proper investigation, the oscillation frequency can be approximated as:

\[ f_o = \frac{1}{2\pi \sqrt{\frac{C_i + C_0}{L}} C_{L1} C_0} \]  
(20)

From (18), (19) and (20) the oscillation frequency is adjusted by the voltage control, \( V_{tune} \). The start-up condition can be obtained from the following equation:

\[ g_m R_P \geq 1 \]  
(21)

where, \( g_m \) is transconductance of transistors and \( R_P \) is the parallel resistor of the inductor. It is critical to consider this equation for maintaining oscillation.

The circuit parameters of the proposed VCO are listed in Table 1.

### 5. SIMULATION RESULTS

In this paper, a temperature compensation VCO is introduced at 24.3 GHz and is designed and simulated (pre-layout) in Hspice software in 0.18 µm CMOS process technology. The Results show that power consumption of the VCO is 10.4 mW at the center frequency.

Figure 12 illustrates the layout of the circuit. As shown in Figure 12, the occupied area is 378 µm × 440 µm. This Figure illustrates that most of the IC space is occupied by inductors.

By employing temperature compensation circuit, the frequency drift becomes less. To prove this claim, the simulated center frequency over a temperature range of -40~120 °C, before and after temperature compensation have been shown in Figure 13. As demonstrated in Figure 13, before and after temperature compensation, the frequency drifts are 33.45 PPM/°C and 11.5 PPM/°C respectively. The proposed VCO has improved in terms of frequency drift about 65.6% (The frequency drifts before and after compensation are about 130 MHz and 45 MHz respectively).

**TABLE 1. Circuit parameters of the proposed VCO**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Design Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>((W/L)<em>{M</em>{1,2}})</td>
<td>20/0.18</td>
</tr>
<tr>
<td>((W/L)<em>{M</em>{3,4}})</td>
<td>26/0.18</td>
</tr>
<tr>
<td>((W/L)<em>{M</em>{5,6}})</td>
<td>2/0.18</td>
</tr>
<tr>
<td>(L_{1,2})</td>
<td>382.75 μH</td>
</tr>
<tr>
<td>(L_{3,4})</td>
<td>214.68 μH</td>
</tr>
<tr>
<td>(C_{1,2})</td>
<td>206.3 fF</td>
</tr>
<tr>
<td>(C_{out\rightarrow in})</td>
<td>46-61 fF</td>
</tr>
<tr>
<td>(C_{out\rightarrow in})</td>
<td>93-122 fF</td>
</tr>
<tr>
<td>(V_{bulk})</td>
<td>0.4 V</td>
</tr>
<tr>
<td>(V_s)</td>
<td>1.8 V</td>
</tr>
<tr>
<td>(V_{DD})</td>
<td>1.8 V</td>
</tr>
<tr>
<td>(V_{DD1})</td>
<td>0.9 V</td>
</tr>
</tbody>
</table>
As demonstrated in Figure 14, the output frequency of the designed VCO can be tuned from 23.75 GHz to 24.8 GHz. Thus, the tuning range of the proposed VCO is 4.12%. This figure shows that the VCO covers a wide frequency range by applying 2 varactors and a simple capacitor bank.

Based on simulation and Figure 15, the phase noise is -118.3 dBc/Hz and -102.6 dBc/Hz at 1 MHz frequency offsets before and after temperature compensation. By adding the temperature compensation circuit, the noise of this circuit affects output of the VCO and the phase noise performance deteriorates. This problem happens because of the transistors which are used at the temperature circuit have noise parameters. Even by considering this problem, the phase noise still acceptable at this frequency.
According to the results, the maximum likelihood of occurring oscillation frequency and phase noise are around 24.36 GHz and -101.4 dBc/Hz. Furthermore, Figures 18 and 19 demonstrate the frequency range and phase noise of the VCO in different modes of the corners. In normal mode, the frequency range is 24.05–24.35 GHz and center frequency has a phase noise of -101 dBc/Hz at 1 MHz offset frequency. In SS and FF corners, The frequency range of 24.05–24.35 GHz with -100.4 dBc /Hz phase noise and the frequency range of 23.98–24.32 GHz with a phase noise of 101.9 dBc / Hz at 1MHz offset frequency have been obtained, respectively. As shown in these figures, in addition to temperature, the proposed VCO has a good stability against process variation.

To compare the performance of the designed VCO with other works, a figure of merit (FOM) has been used. The FOM is defined as follows [12]:

\[
\text{FOM} = L[f_{\text{offset}}] - 20\log \left( \frac{f_c}{f_{\text{offset}}} \right) + 10\log \left( \frac{P_{\text{DC}}}{1\text{mW}} \right)
\]

where, \(L[f_{\text{offset}}]\) is the VCO phase noise, \(P_{\text{DC}}\) is the dc power consumption and \(f_c\) is the carrier frequency. The FOM of the VCO is -179.8 dBc/Hz.

Table 2 summarized some of the published works in the field of temperature compensation VCO design. It is observed that by using the compensation circuit and biasing it to varactors, this VCO can achieve minimized drift frequency while operates at the highest frequency. The temperature coefficient of the proposed VCO is better than other works, however the frequency of this VCO is higher than published works. Moreover, by employing Colpitts and Cross-Coupled pair structures, the power consumption of the proposed VCO is lower than other works. In addition, the proposed VCO has good phase noise performance at higher frequencies.
Also, Table 2 shows that the proposed VCO outperforms other works in terms of FOM.

6. CONCLUSION

In this paper, a temperature compensation VCO based on Cross-Coupled pair and Colpitts structures has been designed and simulated in TSMC 0.18µm CMOS process. By employing this method, the phase noise and other performances are improved. To compensate the frequency drift over a temperature range, MOS varactors are used and biased with a CTAT voltage reference. The CTAT voltage reference and biasing it to varactors helps to have more stable frequency and phase noise versus temperature. By using this technique, the achieved temperature coefficient of the proposed VCO is 11.5 PPM/°C for temperature range of -40-120. In addition, based on simulation results, the phase noise of the proposed VCO is about -102.6 dBc/Hz at 1MHz offset frequency. Moreover, the VCO has 10.4 mW DC power consumption at 24.35 GHz frequency. The VCO covers frequencies of 23.75-24.8 GHz and the tuning range is 4.12%. Furthermore, the proposed VCO has FOM of -179.8 dBc/Hz.

7. REFERENCES

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PAPER INFO

Paper history:
Received 12 September 2018
Received in revised form 05 March 2019
Accepted 03 May 2019

Keywords:
Colpitts Complementary to Absolute Temperature Cross-coupled Pair Temperature Compensation Voltage Controlled Oscillator

چکیده

در این مقاله یک نوسان ساز کنترل شونده با ولتاژ همراه با جبرانسازی حرارتی بر اساس تابع واریتی گیلیت و زوج ضربدری ارائه می‌شود. با استفاده از این ساختار، می‌توان به نیروی فاز بهتر و توان مصرفی کمتر درست یک کر. این مدار در فناوری 0.18 میکرون طراحی و شبیه‌سازی شده است. برای جبرانسازی حرارتی از یک جفت خازن متغیر که به وسیله یک پنجم ولتاژ CTAT تغذیه می‌شوند، استفاده شده است. این معنی‌داره دارد که با استفاده از این روش در گستره دماهای پایدار شدن فرکانس در گستره‌های بالایی می‌شود. شبیه‌سازی نشان می‌دهد که با استفاده از این روش در گستره دماهای 40-120 درجه سانتی‌گراد، ضریب تغییرات 11/10 قسمت در میلیون بر درجه سانتی‌گراد (PPM/°C) در فرکانس مرکزی 24.375 گیگاهرتز به دست می‌آید. با توجه به نتایج کتر، یک میلی‌وات و dBc/Hz 6/102 می‌باشد. مقدار مصرفی نیز 1 مگاهرتز 10/4 می‌باشد.