High Gain DC-DC Converter using Active Clamp Circuit

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Abstract

In this paper, a boost converter with a clamp circuit is proposed for high intensity discharge (HID) lamp application. The clamp circuit provides zero voltage turn on for both main and clamp switches. Compared to conventional boost converters, the proposed converter has the following advantages: (i) high voltage gain without suffering from extreme duty ratio, (ii) low stress on the switches and (iii) low switching losses. Simulation and experimental results show that the voltage stress on the switches are well within acceptable limits and prove the converter’s performance over a wide load range.

1. INTRODUCTION

Many applications like DC back up energy storage system for UPS, HID headlamps, medical equipments etc., driven by battery power source require high efficiency, high conversion ratio DC-DC converters. Conventional boost converters are used to achieve high voltage gain employ various topologies and methods. One method of obtaining high voltage gain is increasing the duty cycle of the converter [1-4]. This gives rise to severe reverse recovery problems and leads to higher switch stress causing reduction in efficiency and EMI problems. Flyback topologies can be used; but, they impose severe voltage and current stress on the components due to the leakage inductance in the transformer windings [1, 5-9]. High voltage gain can also be obtained by paralleling the devices and circuits because of their advantages like expandability and reliability [3]. However, they suffer from interconnection complexity, unequal load sharing and current sharing problems. Hence, they cause system instability. Cascaded boost converters and quadratic converters are also employed to achieve high voltage gain without extreme duty cycle [10, 11]. Nevertheless, they suffer from stability and synchronization problems and also high voltage stress.

Some circuit topologies utilizing coupled inductors may also be used for achieving high voltage gain [4, 8, 10]. The coupled inductor reduces the switch voltage stress. Thus, it eliminates the reverse recovery problems of the diode. However, the leakage energy in the coupled inductor results in high voltage ripple across the switch because the resonant effect leads to degraded power conversion efficiency. Therefore, it becomes necessary to protect the switch from the voltage ripples. This can be achieved by using an active snubber circuit or high voltage rated device with sufficiently high $R_{DS}$ to deplete the leakage energy of the inductor. In addition, this topology may result in input current pulsations and require filtering. Switched capacitors can be utilized to obtain high voltage gain based upon the number of capacitors used in the circuit [11, 12]. For low power applications, they provide high power density, high efficiency, good stability and reduced EMI problems due to the absence of magnetic devices. Nevertheless, their efficiency decreases when a constant output voltage is required. They cannot provide voltage regulation for variations in the line voltage due to relatively high output voltage ripples.

Active clamp circuits can also be employed to achieve high voltage gain with reduced switch stress.
since they effectively recycle the transformer’s leakage energy [1, 13]. However, the voltage gain is about 5 in [14]. This is not suitable for the HID lamp application which requires a voltage gain of 10 when fed from a 12V battery source. In this paper, an active clamp circuit based boost converter is presented for a HID headlamp application. Unlike the existing converter, the proposed converter is designed to work over a wide load range from 35W to 350W. The circuit configuration, modes of operations, steady state analysis, design specifications, simulation and hardware results are presented in this paper.

2. CIRCUIT DESCRIPTION

The voltage conversion ratio of a conventional boost converter is given by

\[
\frac{V_o}{V_{in}} = \frac{1}{1 - D}
\]

where, D is the duty cycle. When a gain of more than 5 is required, conventional boost converters are not suitable due to restriction on duty cycle and reverse recovery problems. In case of cascaded boost converter, the gain is given by

\[
\frac{V_o}{V_{in}} = \frac{1}{(1 - D)^2}
\]

Thus, high voltage gain can be achieved without suffering from extreme duty ratio. However, circuit becomes complex as more components need to be used. Figure 1 shows a boost converter which is used to overcome the drawbacks of a cascaded boost converter. Here, the power switch is operated in hard switching which results in increased switching losses.

To reduce the switching losses of the power switch, soft switching is achieved using an active clamp circuit as shown in Figure 2. The active clamp circuit consists of a switch \( Q_a \), clamp capacitor \( C_c \) and a resonant inductor \( L_r \) which resonate with the body capacitance \( C_r \) of the main switch \( Q \) to achieve ZVS of both the switches.

The main switch and the clamp switch operate in complementary fashion with a short resonant time delay. When the main switch is turned off, the inductor current \( i_{L1} \) flows through the body diode of the clamp switch, the clamp capacitor and to the ground. This forces the drain to source voltage of the clamp switch to fall zero. Hence, it can be turned on to achieve soft switching. Similarly, when the clamp switch is off, the negative inductor current \( i_{L2} \) flows through the resonant capacitor which discharges and reaches zero so as to achieve ZVS of the main switch.

3. MODES OF OPERATION

The following assumptions are made to explain the modes of operation of the proposed circuit:

i. The values of capacitors \( C_1, C_c, C_o \) are kept large enough such that the voltage across them is maintained constant.

ii. The energy stored in the resonant inductor \( L_r \) is greater than the energy stored in the resonant capacitor \( C_r \), this ensures soft switching of both main and clamp switch.

iii. The inductances \( L_1 \) and \( L_2 \) are greater than the inductance of \( L_r \).

Figure 3 shows the characteristic waveforms of the circuit operating under continuous conduction mode (CCM) for one switching cycle.

3.1. Mode 1 [ \( t_0 < t < t_1 \) ] In this mode, the main switch \( Q \) is turned on, the clamp switch \( Q_a \) is off. The diodes \( D_1 \) and \( D_3 \) are off and \( D_2 \) is in conduction. The capacitor \( C_o \) discharges to feed the load. Since \( L_1 \) and \( L_2 \) is greater than \( L_r \), the inductor currents \( i_{L1} \) and \( i_{L2} \) increases which is given by the governing equations as given below.
\[ i_{L1} = i_{L1}(t_0) + \frac{V_{L1}DT}{L_1} \]  
\[ i_{L2} = i_{L2}(t_0) + \frac{V_{C1}DT}{L_2} \]

where, \( D \) is the duty cycle of the main switch. The switch currents are given by \( i_{Q1} = I_{L1r} \) and \( i_{Q2} = 0 \). The inductor voltages are given by

\[ V_{L1} + V_{L2} = V_{in} \]  
\[ V_{L2} = V_{C1} \]

3. 2. Mode 2 \([ t_1 < t < t_2 ]\) The main switch \( Q \) is turned off at \( t_1 \). \( D_2 \) is still conducting. The positive inductor current \( I_{Lr} \) charges the resonant capacitor \( C_r \). Since \( C_r \) is very small, it is charged linearly and is given by the following equation:

\[ V_{C_r} = \frac{i_{Lr}(t_0)(t-t_1)}{C_r} \]

As long as \( V_{C_r} < V_{C1} \), the diodes \( D_1 \) and \( D_3 \) remain in reverse bias. When \( V_{C_r} = V_{C1} \), voltage across \( D_1 \) and \( C_1 \) is approximately equal to \( V_{C1} \). Therefore, \( D_1 \) is turned on. Now, the diode current \( i_{D1} \) increases and \( i_{D2} \) decreases. \( C_r \) charges further till it is equal to \( V_{C1} \). When \( V_{C1} = V_{C2} \), the antiparallel diode of clamp switch is turned on. This forces the drain to source voltage of the clamp switch to zero. The switch can now be turned on to realize ZVS. This mode ends when \( i_{D2} = 0 \) and \( D_3 \) is turned on.

3. 3. Mode 3 \([ t_2 < t < t_3 ]\) This mode begins when \( D_3 \) is turned on at \( t_2 \). The inductor currents \( i_{L1} \) and \( i_{L2} \) decrease which in turn decreases \( i_{Lr} \). \( i_{Lr} \) decreases from positive value to zero and then goes to negative value. Before \( i_{Lr} \) becomes negative, \( Q_t \) is turned off. This mode ends when \( Q_t \) is turned off at \( t_3 \). The inductor current is given by

\[ i_{Lr}(t) = i_{Lr}(t_2) - \frac{(V_{C2} - V_{Q_t})(t-t_3)}{L_r} \]

3. 4. Mode 4 \([ t_3 < t < t_4 ]\) In this mode, \( D_3 \) remains in conduction. The negative inductor current \( i_{Lr} \) discharges the capacitor \( C_r \). The capacitor voltage \( V_{C1} \) decreases from \( V_{C2} \) to zero. When \( V_{C1} = 0 \), the antiparallel diode of the main switch is turned on. This makes the drain to source voltage of the main switch equal to zero. The main switch \( Q \) can now be turned on at this instant to achieve ZVS. This mode ends when \( Q \) is turned on. The output diode currents \( i_{D3} \) decreases. When \( i_{D3} = 0 \), \( D_2 \) is turned on.

3. 5. Mode 5 \([ t_4 < t < t_5 ]\) This mode commences when \( D_4 \) is turned off and \( D_1 \) and \( D_2 \) are in commutation interval. The voltage across inductor \( L_2 \) is zero. Hence, \( V_{C1} = V_{Lr} \) thereby increasing \( i_{Lr} \). The diode currents \( i_{D1} \) decreases and \( i_{D2} \) increases. This mode ends when \( i_{D1} = 0 \), so it turns off \( D_1 \).

4. STEADY STATE ANALYSIS

Applying voltage-second balance across inductances \( L_1 \) and \( L_2 \) and neglecting the duty cycle losses for each mode, we can obtain the steady state voltage gain of the circuit. When the switch \( Q \) is closed, \( V_{L1} = V_{in} \) and \( V_{L2} = V_{C1} \). When the switch is open, \( V_{L1} = V_{in} - V_{C1} \) and \( V_{L2} = V_{C1} - V_o \). Thus, we have

\[ V_{in}D + (V_{in} - V_{C1})(1-D) = 0 \]

Rearranging Equation (9), we get a gain which is given by Equation (10).

\[ \frac{V_{C1}}{V_{in}} = \frac{1}{1-D} \]

Similarly, applying volt-second balance for the inductor \( L_2 \), we get,

\[ V_{C1}D + (V_{C2} - V_{C1})(1-D) = 0 \]

Rearranging Equation (11) yields,

\[ \frac{V_{C1}}{V_{C2}} = \frac{1}{1-D} \]

Figure 3. Characteristic waveforms of the proposed circuit
Combining Equations (10) and (12), we get the overall conversion ratio as
\[
M = \frac{V_o}{V_{in}} = \frac{1}{(1-D)^2}
\]
(13)

5. DESIGN SPECIFICATIONS

The efficiency of the given circuit is given by
\[
\eta = \frac{P_o}{i_{L1av}V_{in}}
\]
(14)
The maximum duty cycle of the main switch is obtained at minimum input voltage and is expressed as
\[
D_{max} = 1 - \sqrt{\frac{V_{o,min}}{V_o}}
\]
(15)

If the ripple currents \(\Delta i_{L1}\) and \(\Delta i_{L2}\) are given, the value of inductances \(L_1\) and \(L_2\) can be obtained as follows
\[
L_1 > \frac{DTV_{in}}{\Delta i_{L1}}
\]
(16)
\[
L_2 > \frac{DTV_{in}}{\Delta i_{L2}(1-D)}
\]
(17)
The energy stored in the resonant inductor \(L_r\) should be greater than the energy stored in the resonant capacitor \(C_r\) to achieve soft switching of both the main and the clamp switches. This assumption can be used to calculate the value of \(L_r\) or \(C_r\) if one of the values is known.
\[
L_r > \frac{C_rV_o^2}{(i_r(t_r))^2}
\]
(18)
The delay time between the main switch and the clamp switch is given by \(\pi\sqrt{L_rC_r}/2\). If \(C_r\) is known, the value of \(L_r\) can be obtained by the following equation
\[
L_r \approx \frac{4t_r^2}{\pi^2C_r}
\]
(19)

In addition, half the resonant period is larger than the off time of the main switch \(Q\). Therefore, we get the Equation (20) for \(C_r\) as follows
\[
C_r = \frac{(1-D)^2T^2}{L_r\pi^2}
\]
(20)

Using the Equations (14) to (20), the values of \(L_r\), \(C_r\), \(C_o\), \(L_1\), \(L_2\) and \(D\) are obtained. Based on the voltage ripple, the output capacitor \(C_o\) is computed using Equation (21).

6. SIMULATION RESULTS

The proposed circuit with the specifications given in Table 1 was simulated using Pspice. Figure 4 shows the output voltage and output power waveforms for the load equivalent to 120V, 35W. Figure 5 shows the gate voltage, drain to source voltage and switch current of the main switch \(Q\). Here, the switch can be turned on when the drain to source voltage of the switch is approximately zero. This ensures ZVS of the main switch \(Q\). Figure 6 shows the gate and drain voltages and current through the clamp switch \(Q_a\). Before the switch is turned on, the current through the switch is negative and the voltage across it is near zero as soft switching also achieve for the clamp switch. From Figures 5 and 6, it is observed that the stress across the switches is found to be 100V which is less than the output voltage.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>12V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>120V</td>
</tr>
<tr>
<td>Output Power</td>
<td>35W – 350W</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>50kHz</td>
</tr>
<tr>
<td>(L_1)</td>
<td>500µH</td>
</tr>
<tr>
<td>(L_2)</td>
<td>4mH</td>
</tr>
<tr>
<td>Resonant Inductor (L_r)</td>
<td>15µH</td>
</tr>
<tr>
<td>Capacitors (C_1)</td>
<td>220µF</td>
</tr>
<tr>
<td>Resonant Capacitor (C_r)</td>
<td>600pF</td>
</tr>
<tr>
<td>Clamp Capacitor (C_c)</td>
<td>800nF</td>
</tr>
<tr>
<td>Output Capacitor (C_o)</td>
<td>20mF</td>
</tr>
<tr>
<td>Switches (Q) and (Q_a)</td>
<td>IRF740 (400V, 10A, 0.55Ω)</td>
</tr>
<tr>
<td>Diodes (D_1), (D_2) and (D_3)</td>
<td>MUR860 (200V, 8A)</td>
</tr>
</tbody>
</table>

![Figure 4. Output voltage and output power plots](image-url)
7. EXPERIMENTAL RESULTS

The experimental set up of the proposed converter with the specifications mentioned in Table 1 was built and tested for verifying its performance. Figure 10 shows the gate pulses applied to the main and auxiliary switches. The converter duty cycle, complementary nature of the gate pulses and the voltage across the switches can be verified from Figure 10. The application and removal of gate pulse to the main switch causes energy storage and dissipation across the inductor, respectively. This behaviour of the proposed converter is verified from Figure 11. The proposed converter provided the required voltage gain of 10. As a result, the output voltage was 123 V which closely matches with the theoretical design and simulation results. Further, based on the output current waveform, it can be verified that the output power obtained at the output was 320W which explains the operating range of the proposed converter. Figure 12 confirms the wide operating range of the proposed converter along with its ability to provide the required output voltage and output current. The voltage stress across the main and auxiliary switches is within acceptable limits and is shown in Figures 13 and 14, respectively.
8. CONCLUSION

The operational details, analysis and experimental results of a high gain DC-DC converter with clamp circuit have been presented in this paper. By addition of resonant elements $L_r$ and $C_r$, soft switching of both the main and auxiliary switches has been achieved. Experimental results obtained from the proposed circuit prove that the converter operates under ZVS condition over a wide load range. Further, the converter is capable of providing the required voltage gain of 10 and delivers the required load power. In addition, the voltage stress across the switches is within acceptable limits due to soft switching of the main and auxiliary switches.

9. REFERENCES

13. Ismail, E. H., Al-Saffar, M. A. and Sabzali, A. I., "High conversion ratio DC–DC converters with reduced switch stress".  

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