New Hybrid Cascaded Multilevel Inverter

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**Abstract**
This paper proposes a single-phase five-level inverter with a modified pulse width-modulated (PWM) control scheme. The modified pulse width-modulation technique is developed to reduce switching losses. Also, the proposed multilevel inverter can reduce the requirement of power switches compared to a conventional cascaded multilevel inverter. The modes of operation, control signals, and operating principle of the proposed inverter are analyzed.

The inverter is capable of producing five levels of output-voltage ($V_s$, $V_s/2$, 0, $-V_s$, $-V_s/2$) from the dc supply voltage. In particular, aspects of total harmonic distortion (THD) for the proposed multilevel converters are discussed. The hybrid cascaded H-Bridge inverter with very low switching losses is ideal for such operations. The behaviour of the inverter has been analyzed with the simulation and experimental results. In this paper a new five level inverter with reduced number of switches is proposed and MATLAB/SIMULINK results are presented.

**1. Introduction**

The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonic applications [1]. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs that can be batteries, fuel cells, capacitors, etc. [2]. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multi level inverter is higher output quality, lower harmonic component, better electromagnetic compatibility, and lower switching losses. The most common topologies are the cascaded H-bridge inverter and its derivatives, the Diode-clamped multilevel inverter, and Flying Capacitor multilevel inverter [3].

The main advantage of common topologies is that the rating of the switching devices is highly reduced to the rating of each cell [4]. However, they have the drawback of the required large number of switching devices which equals $2(k-1)$ where $k$ is the number of levels [5]. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency. Multilevel voltage source inverters have unique structure which allows them to extent high voltages and to reduce individual device switching frequency without the use of transformers [6]. For high-power applications, multilevel inverter structures have the particular advantages of operation at high dc bus voltages, achieved using series connections of switching devices and a reduction in output voltage harmonics, achieved between multiple voltage levels [7]. Moreover, multilevel converters present several other advantages: Generate better output waveforms with a lower $dv/dt$ than the standard converters (power quality) [8].

This paper proposes a new converter topology, presented as a block diagram in Figure 1. This topology includes an H-bridge stage with a bidirectional switch, drastically reducing the power circuit complexity [9].

The new converter topology shown in block diagram offers an important improvement in terms of lower component count and reduced layout complexity when compared with the five-level converters presented in the diode clamped and flying capacitor multilevel inverter [10]. Hybrid converters are converters that present semiconductor switching at different frequencies. Symmetrical converters are converters with symmetric
dc sources [11]. The new topology achieves almost a 40% reduction in the number of main power switches required and uses no more diodes or capacitors.

2. CIRCUIT CONFIGURATION

The proposed cascaded multilevel inverter as shown in Figure 2 consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four diodes and one IGBT. The inverter produces output voltage in five levels: zero, 0.5\( V_s \), \( V_s \), -0.5\( V_s \) and -\( V_s \). In this circuit configuration the two capacitors in the capacitive voltage divider are connected directly across the dc bus, the dynamic voltage balance between the two capacitors is automatically restored.

2.1. Modes of Operation

Figure 2 shows the complete power circuit used in the five-level inverter. The H-bridge is formed by the four main power devices, namely Disp1 to Disp4, capacitor voltage divider provides a half of the supply voltage, at node A, formed by C1 and C2. The bidirectional switch formed by the controlled switch Disp5 and the four diodes, D5 to D8, which connects to node A. A resistive load and the same output waveform were considered in all the cases. The required five voltage output levels 0, \( V_s/2 \), \( V_s \), -\( V_s/2 \), -\( V_s \) are generated as follows:

**MODE 1.** When the two main switches Disp3 and Disp4 are ON, it short-circuits the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Figure 5 shows the current paths that are active at this stage.

\[
0 < t < \pi/6 \\
V_{out} = 0 \\
\pi/6 < t < 7\pi/6 \\
11\pi/6 < t < 2\pi
\]

**MODE 2.** When the auxiliary switch, Disp5 is ON, it connects the positive terminal of load to node A, through diodes D5 and D8, and when the main switch Disp4 is ON, it connects the negative terminal of load to ground. All other controlled switches are OFF; the voltage applied to the load terminals is \( V_s/2 \). Figure 4 shows the current paths that are active at this stage.

\[
V_{out} = V_s/2 \\
\pi/6 < t < \pi/3 \\
2\pi/3 < t < 5\pi/6
\]

**MODE 3.** When the main switch Disp1 is ON, it connects the positive terminal of load to \( V_s \), and when Disp4 is ON, it connects the negative terminal of load to
ground. All other controlled switches are OFF; then the voltage applied to the load terminals is $V_s$. Figure 3 shows the current paths that are active at this stage.

$$V_{out} = V_s \quad ; \quad \frac{2}{3} < t < \frac{2\pi}{3}$$

**MODE 4:** When the auxiliary switch, Disp5 is ON, it connects the positive terminal of load to node A, through diodes D6 and D7, and when the main switch Disp2 is ON, it connects the negative terminal of load to $V_s/2$. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_s/2$. Figure 6 shows the current paths that are active at this stage.

$$V_{out} = -\frac{V_s}{2} \quad ; \quad \frac{5\pi}{3} < t < \frac{11\pi}{6}$$

**MODE 5:** When the main switch Disp2 is ON, it connects the negative terminal of load to $V_s$ and when Disp3 is ON, it connects positive terminal of load to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_s$. Figure 7 shows the current paths that are active at this stage.

$$V_{out} = -V_s \quad ; \quad \frac{8\pi}{6} < t < \frac{5\pi}{3}$$

<table>
<thead>
<tr>
<th>Disp 1</th>
<th>Disp 2</th>
<th>Disp 3</th>
<th>Disp 4</th>
<th>Disp 5</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>$V_s$</td>
</tr>
<tr>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>$V_s/2$</td>
</tr>
<tr>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>0</td>
</tr>
<tr>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>$-V_s/2$</td>
</tr>
<tr>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>$-V_s$</td>
</tr>
</tbody>
</table>

**3. SWITCHING LOSS CALCULATIONS**

Consider a MOSFET switch connected across a dc voltage of value $V_{dc}$. During on time, the current through switch is $I_{dc}$. The figure shows the waveforms of the voltage and current through switch when it is operated at a switching frequency of $F_s=1/T_s$, where $T_s$ is the switching period. In the figure, $V_M$, $I_M$ are the
voltage across and the current through the MOSFET [12].
Switching losses can be calculated from the turn on and turn off characteristics of the switch. Instantaneous voltage and current during on time \( t_{c(on)} \) are:

\[
v(t) = V_{dc} - (V_{dc} - V_{on}) \cdot \left( t / t_{c(on)} \right)
\]

\[
i(t) = I_{dc} \cdot \left( t / t_{c(on)} \right)
\]

where,
\( v(t) \), \( i(t) \) : instantaneous voltage and current
\( V_{dc} \) : voltage across switch when turned on
\( V_{on} \) : voltage across switch when turned on
\( t \) : time in sec
\( t_{c(on)} \) : turn-on cross over interval
\( I_{dc} \) : current through switch when turned on
\( T_s \) : sampling time in sec

Instantaneous power during the interval \( t_{c(on)} \) is:

\[
p(t) = v(t) \cdot i(t)
\]

Energy dissipated during this interval is \( E_{con} \):

\[
E_{con} = \int_{0}^{t_{c(on)}} \left( V_{dc} \cdot I_{dc} + \left( \frac{t}{t_{c(on)}} \right) - (V_{dc} - V_{on}) \cdot \frac{t^2}{t_{c(on)}} \right) dt
\]

\[
E_{con} = \frac{V_{dc} \cdot I_{dc} \cdot t_{c(on)} + \frac{1}{2} \cdot I_{dc} \cdot \left( \frac{t}{t_{c(on)}} \right)^2 - (V_{dc} - V_{on}) \cdot \left( \frac{1}{2} \cdot \left( \frac{t}{t_{c(on)}} \right)^2 \right)}{3}
\]

During turn off transition, of \( t_{c(off)} \), the current falls from \( I_{dc} \) to zero and the \( V_{on} \) increases linearly to \( V_{dc} \). The instantaneous voltage and current during this period are:

\[
v(t) = V_{on} + (V_{dc} - V_{on}) / t_{c(off)}
\]

\[
i(t) = I_{dc} - I_{dc} / t_{c(off)}
\]

where,
\( t_{c(off)} \) : turn off cross over interval
\( T \) : The instantaneous power dissipated during the interval is \( E_{con} \):

\[
p(t) = v(t) \cdot i(t) = \frac{V_{on} \cdot I_{dc} + (V_{dc} - V_{on}) \cdot I_{dc} \cdot \left( \frac{t}{t_{c(on)}} \right)}{T} - \frac{V_{on} \cdot I_{dc} \cdot \left( \frac{t}{t_{c(on)}} \right)^2}{2} - \frac{(V_{dc} - V_{on}) \cdot I_{dc} \cdot \left( \frac{t}{t_{c(on)}} \right)^2}{2} / T_s
\]

The average switching loss \( P_{sw} \) in the switch is:

\[
P_{sw} = \frac{1}{2} \cdot V_{dc} \cdot I_{dc} \cdot \left( \frac{t_{c(on)} + t_{c(off)}}{T_s} \right) + \frac{1}{2} \cdot V_{on} \cdot I_{dc} \cdot \left( \frac{t_{c(on)} + t_{c(off)}}{T_s} \right)
\]

4. PROPOSED PWM TECHNIQUE

Figure 9 shows the relationship between the sinusoidal reference signal and the triangular carrier signal which is used to create the PWM signal. The output of the PWM signal is either 1, when \( V_{ctrl} > V_{tri} \) or 0, when \( V_{ctrl} < V_{tri} \), and the PWM signal width can be written as Equation (9)

\[
T_{PWM} = A_{ctrl} \cdot T_{tri} \quad 0 \leq A_{ctrl} \leq 1
\]

where,
\( T_{PWM} \) : Width of the PWM signal
\( A_{ctrl} \) : Height of the control signal
\( T_{tri} \) : Period of the triangular signal
\( V_{ctrl} \) : Output voltage of the control signal
\( V_{tri} \) : Output voltage of the triangular signal

Modulated signal is created as per Equations (11) and (12), and amplitude modulation index \( m_a \) can be found in the Equation (13).

\[
f(t) = m_a \sin (\omega t)
\]

\[
A_1 = 1; \quad f(t) \geq 0
\]

\[
0; \quad f(t) < 0
\]

\[
A_2 = 1; \quad |f(t)| \geq \frac{1}{2}
\]

\[
0; \quad |f(t)| < \frac{1}{2}
\]

\[
m_a = V_{ctrl} / V_{tri}
\]

The hybrid multilevel inverter consists of one full H-bridge and bidirectional switch. The one leg of full H-bridge operates at square wave mode and remaining switches operate at PWM mode. The modulated signals PWM, A2, and A1 as shown in Figure 13 are the parameters used in digital process to generate the control signals as shown in Table 2.
5. SIMULATION RESULTS

The control signals are generated and the output voltage evaluated by using the MATLAB/SIMULINK platform. Output voltage can be controlled using the modulation index and output frequency controlled by adjusting the frequency. The simulation results of the proposed hybrid multilevel inverter are illustrated in Figure 17. The simulation results based on switching losses analysis are also performed for the proposed hybrid multilevel inverter as shown in Figure 14.

<table>
<thead>
<tr>
<th>Electronic Switch Devices</th>
<th>Digital Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>PWM((A2\cdot A1)+(A2\cdot A1))</td>
</tr>
<tr>
<td>S2</td>
<td>A1</td>
</tr>
<tr>
<td>S3</td>
<td>PWM((A2\cdot A1)+(A2\cdot A1))</td>
</tr>
<tr>
<td>S4</td>
<td>A1</td>
</tr>
<tr>
<td>S5</td>
<td>PWM</td>
</tr>
</tbody>
</table>
TABLE 3. Simulation parameters for new hybrid cascaded multilevel inverter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>100V</td>
</tr>
<tr>
<td>Frequency of the carrier</td>
<td>12,000Hz</td>
</tr>
<tr>
<td>Dc bus utilisation voltage</td>
<td>93.01V</td>
</tr>
<tr>
<td>Modulation index</td>
<td>0.75</td>
</tr>
</tbody>
</table>

TABLE 4. Comparison between different topologies

<table>
<thead>
<tr>
<th></th>
<th>Diode clamped</th>
<th>Flying capacitor</th>
<th>Cascaded H-bridge</th>
<th>New hybrid cascaded</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of switches</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td>No. dc supply</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Main diodes</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td>Clamping diodes</td>
<td>12</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Dc bus capacitors</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Balancing capacitors</td>
<td>0</td>
<td>0</td>
<td>6</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 4 shows the comparison between different topologies for a five level multilevel inverter based on requirement of main switches, dc supply, main diodes, clamping diodes, balancing capacitors, and DC bus capacitors.

6. EXPERIMENTAL RESULTS

The block diagram shown in Figure 19 explains the hardware which consists of power supply, DC source, Microcontroller, Driver circuit and the power switches. To experimentally validate the new hybrid cascaded MLI using the proposed modulation technique, a prototype of five-level inverter has been built using IRF460 MOSFET for the full bridge inverter and power diode for the auxiliary switch as shown in Figure 20. The gating signals are generated using PIC16F877A microcontroller which is shown in Figures 21-24. The output voltage for the five level is shown in Figure 25.
7. CONCLUSION

In conclusion, a single-phase five-level inverter with a modified pulse width-modulated (PWM) control scheme has been developed. The proposed multilevel inverter can reduce the requirement of power switches compared to a conventional cascaded multilevel inverter. The modes of operation, control signals, and operating principle of the proposed inverter were analyzed. The inverter is capable of producing five levels of output-voltage ($V_s$, $V_s/2$, 0, $-V_s$, $-V_s/2$) from the dc supply voltage. Aspects of total harmonic distortion (THD) for the proposed multilevel converters have been discussed. The behaviour of the inverter has been analyzed with the simulation results and experimental results.

8. REFERENCES

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In this paper, a new hybrid cascaded multilevel inverter (PWM) is proposed. The inverter is designed to have a reduced total harmonic distortion (THD) compared to traditional cascaded multilevel inverters. The proposed inverter uses a modified pulse width modulation (PWM) technique to achieve a lower THD. The paper includes simulation results using MATLAB/SIMULINK to verify the performance of the proposed inverter.