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An Ultra-low-power Static Random-Access Memory Cell Using Tunneling Field Effect Transistor

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A B S T R A C T

In this research article, an Ultra-low-power 1-bit SRAM cell is introduced using Tunneling Field Effect Transistor (TFET). This paper investigates feasible 6T SRAM configurations on improved N-type and P-type TFETs integrated on both InAs (Homojunction) and GaSb-InAs (Heterojunction) platforms. The voltage transfer characteristics and basic parameters of both Homo and Heterojunctions are examined and compared. The proposed TFET based SRAM enhances the stability in the hold, read, and write operations. This work evaluates the potential of TFET which can replace MOSFET due to the improved performance with low-power consumption, high speed, low sub-threshold slope, and supply voltage (VDD = 0.2 V). The results are correlated with CMOS 32nm technology. The proposed SRAM TFET cell is implemented using 30nm technology and simulated using an H-SPICE simulator with the help of Verilog-A models. The proposed SRAM TFET cell architecture achieves low power dissipation and attains high performance as compared to the CMOS and FINFET.

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NOMENCLATURE

C_d	Depletion layer capacitance	Q	Elementary charge
C_{ox}	Gate oxide capacitance	Const	Device dimensions and materials parameter
T	Temperature	Vgs	Gate source voltage
k	Boltzmann constant		

1. INTRODUCTION

In the present scenario, several researchers are working towards reducing the size of the transistors to make miniature Integrated Chip (IC) [1]. The silicon CMOS technology has become an effective fabrication process for high performance and lucrative VLSI circuits. Most of the VLSI industries are using CMOS, which is having a high sub-threshold slope and high-off current at room temperature [5]. Due to this factor, the leakage current and heat of the system is also increased [7]. In SRAM cell, thick gate oxide present in the long channel device is used to reduce the leakage current. OFDM transceiver IC is used to provide high-speed data transmission in wideband wireless communication [8]. TFET is a forthcoming transistor that is studied extensively on the way towards power-efficient integrated circuits as a replacement of CMOS in the supply voltage regime below VDD = 0.3 V [3-5].

In this work, the TFET characteristics are briefly explained and TFET based SRAM cell is designed with two different types: Homojunction and Heterojunction [9-12]. These results are compared with the 32 nm CMOS SRAM design. The sub-threshold slope, power and supply voltages are reduced. The switching speed of the system can also be increased by using TFETs [10].

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This paper methodized the Tunneling Field Effect Transistor in Section 2. Homojunction and Heterojunction TFETs are presented in Section 3. Section 4 portrays the proposed TFET based SRAM design. The results of SRAM design are discussed in Section 5. The article concluded in Section 6.

2. TUNNELING FIELD EFFECT TRANSISTOR

For achieving low energy electrons, a new type of transistor TFET is proposed, which is used in the family of Field Effect Transistor (FET) under the division of MOSFET [2]. The MOSFET is working based on the thermionic emission principle but TFET operates based on the quantum tunneling mechanism, because of this sub-threshold slope of TFET is less than 60mV/dec at room temperature [6].

2. 1. Structure and Operation of TFET The TFET structure is analogous to the MOS transistor excluding the source and drain terminals shown in Figure 1. In TFET, the source terminal is doped with a p-type material and the drain terminal is doped with an n-type material. The TFET structure also named as P-I-N (P-type source terminal, intrinsic region, and N-type drain terminal) structure [3].

The tunneling process occurs at the sufficient gate bias where the electron moves from the lower band of the p-type source terminal to the upper band of drain terminal [5]. If the gate bias is reduced, the current cannot flow a long time because of band misalignment [13-14]. When the transistor attains off condition it is in the same mode and there are no electrons will move from p-type to n-type terminal [15-17].

The NTFET Tunneling process is shown in Figure 2. The operation of NTFET is the same as the operation of PTFET but the difference attains only the majority carriers. In NTFET, the majority carriers are electrons and holes are the majority carriers in PTFET. The gate voltage is a negative voltage for PTFET, it is same as the MOSFET but there is no body bias in TFET [11]. In the N-channel case, the Fermi level is very close to the valence band edge due to high density of states for holes. In the P-channel, the Fermi level degeneracy is quite high due to low density of states for electrons. This causes a high energy tail, which limits the sub-threshold slope and gives rise to a strong temperature dependence similar to that of a MOSFET [23].

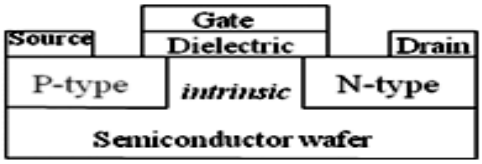

Figure 1. Basic Structure of TFET

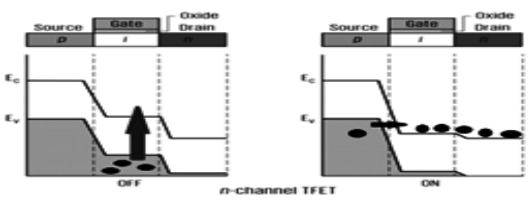

Figure 2. NTFET Tunneling Process

2. 2. Sub-threshold Swing The sub-threshold swing is the reciprocal value of the sub-threshold slope. The sub-threshold slope is a slope of logarithmic drain current and gate voltage characteristic of MOSFET. The sub-threshold swing of MOSFET is given below:

$$SS_{MOSFET} = \ln(10)\left(\frac{kT}{q}\right)\left(1+\frac{C_d}{C_{ox}}\right) \text{ [mV/dec]} \quad (1)$$

Based on Equation (1), the leakage current of the conventional device lies in the sub-threshold region. The above equation is used only for MOSFET. For calculating the sub-threshold swing of TFET, another equation is used as the mechanism depends on the tunneling barrier width [4] which is given by:

$$SS_{TFET} = \frac{V_{gs}^2}{5.75(Vgs+Const)} \text{ [mV/dec]} \quad (2)$$

If the sub-threshold swing of a device is small, then the leakage current, power dissipation and the threshold voltage of a device will also occur quite low [18]. Field Programmable Gate Array (FPGA) provides more flexible, accurate in simulating, testing and gives end to end solutions for reprogramming the proposed designs in the hardware [19].

3. HOMOJUNCTION AND HETEROJUNCTION TUNNEL FIELD EFFECT TRANSISTORS

The sub-threshold slope, power consumption and delay of the TFET are reduced based on the band-gap of the materials which is used for TFET fabrication. TFET is divided into two categories based on semiconducting materials.

3. 1. InAs Homojunction A Homojunction is a semiconductor material that has equal band gaps in between two layers of similar semiconductors with different doping concentrations. InAs is used for high electron mobility and it is a direct band-gap material [12]. The values of basic parameters for InAs are energy gap=0.354 eV, Intrinsic carrier concentration=1.1015 cm-3, Intrinsic resistivity=0.16 Ω.cm, Effective conduction band density of states =8.7x1016 cm-3, Effective valence band density of states=6.6x1018 cm-3.

3. 2. GaSb-InAs Heterojunction A Heterojunction is a semiconductor material which is having unequal band gaps in between two layers of dissimilar semiconductors. The energy band diagram of Heterojunction types is shown in Figure 3. It works at high frequency and also used in High Electron Mobility Transistors (HEMT). TFET operates at minimum voltage when the band gaps of crystalline semiconductors are unequal [20]. The Heterojunction semiconductor alignment is divided into three types. Those are a Straddling gap, Staggered gap and Broken gap [12].

In this paper, the two types of TFETs, Homojunction and Heterojunction are simulated. these two TFETs are compared with its basic parameters based on the results. When it is in contact, GaSb and InAs have non-overlapping band-gap, which forms more interesting phenomena in heterostructure from those materials. In an intrinsic heterostructure, the carriers are generated by the migration of charges from GaSb to InAs layers. Here the sheet densities of mobile electrons and holes are the same [11].

For a large number of experiments, it is useful to control the electron-hole ratio. In the broken band-gap arrangement of GaSb-InAs heterostructure, InAs conduction band occurs lower in energy than the GaSb valence band, it causes charge. Mobilization from the GaSb to the InAs layers [21]. Due to this arrangement, intrinsic populations of mobile electrons and holes are generated in the absence of doping. For thin InAs wells, quantization of the confinement energy becomes significant at low temperature, leading to quasi-two-dimensional behavior as the carrier wave functions are restricted in growth to the direction for a number of states corresponding to discrete sub-band energies [22].

4. PROPOSED TUNNEL FIELD EFFECT TRANSISTOR BASED STATIC RANDOM-ACCESS MEMORY DESIGN

Static Random-Access Memory (SRAM) is a volatile semiconducting memory, which is used to store on condition without periodic data as long as the power supply is refreshed. SRAM is a high-speed memory cell in the RAM family. The 6T TFET SRAM circuit is shown in Figure 4.

4. 1. SRAM Cell Operation The SRAM cell contains six TFET transistors which are X1, X2, X3, X4, X5, and X6. Here two TFET inverters (X1, X2, X3 and X4) are cross-coupled. During read and write operations the access is controlled by two additional TFET transistors X5 and X6. Because of this architecture, the supply voltage of a cell is less than 0.25 V, the power dissipation is also very low and it has high noise immunity. There are three stages present in SRAM named as read, write and hold mode operations. The working of these stages is given below.

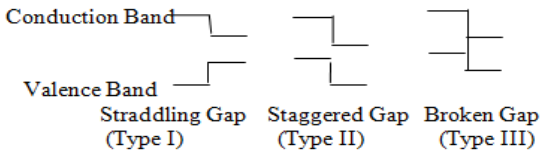

Figure 3. Heterojunction Types

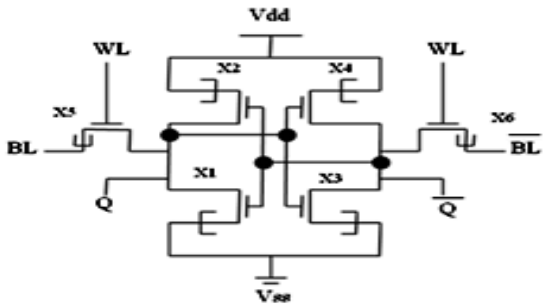

Figure 4. 6T TFET SRAM Circuit

4. 1. 1. Hold For the hold operation the word line should be 0 (WL = 0). So, the access transistors X5 and X6 are not able to connect with the bit lines because of this SRAM keeps the present data in the cross-coupled inverters (X1, X2, X3, and X4) as long as the supply voltage is ON.

4. 1. 2. Reading To read the data from SRAM cell Word Line (WL) is always in the ON condition and both the bit lines should be recharged. The sense amplifier is used to sense the data from the SRAM cell. The output of the SRAM cell is given as input of sense amplifier. The Q and $\overline{Q}$ are the inputs of sense amplifier, if Q < $\overline{Q}$ then the output of sense amplifier is 0, and if Q > $\overline{Q}$ then the output is 1.

4. 1. 3. Writing To write a 1 into the SRAM cell, first WL and BL (Bit Line) should be 1 and $\overline{BL}$ should be 0. If 0 is written to the SRAM cell, then the value of BL should be inverted.

5. RESULTS AND DISCUSSION

5. 1. SRAM Write Operation by using TFET In Homojunction TFET when the word line is ON (WL=1), the SRAM circuit allows the external input inside the cell to store the data. If WL=0, then SRAM circuit keeps the previous data which is shown in Figure 5. The power of the Homojunction SRAM is 17.8 nW.

In Heterojunction TFET, when the word line is ON (WL=1), the SRAM circuit allows the external input, inside to store the data. If WL=0, then the GaSb-InAs

SRAM circuit keeps the previous data which is shown in Figure 6. The power of the Heterojunction SRAM is 0.38nW.

5. 2. SRAM Read Operation by using TFET In 6T TFET SRAM Read Operation, the sense amplifier is connected to read the stored data from SRAM cell. For read operation, the word line should be 0 (WL=0). The output of the Homojunction TFET SRAM read operation result is shown in Figure 7. The power of the Homojunction SRAM cell is 208.2 nW.

For a read operation, the word line should be 0 (WL=0). The output of the Hetrojunction TFET SRAM read operation result is shown in Figure 8. The power of Heterojunction SRAM cell is 1.87 nW.

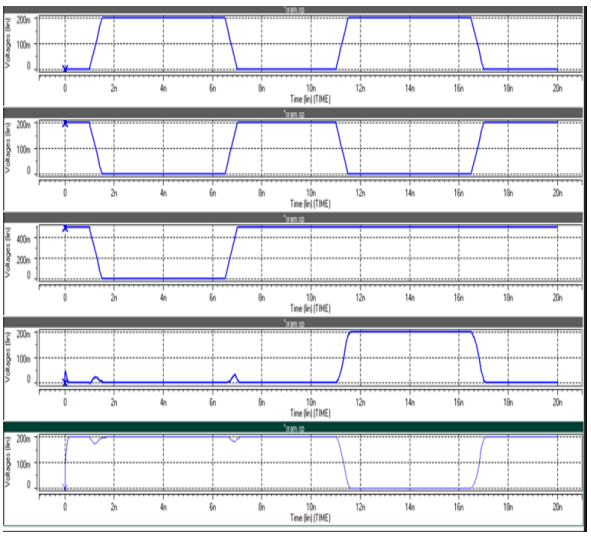

Figure 5. Homojunction 6T SRAM write operation result

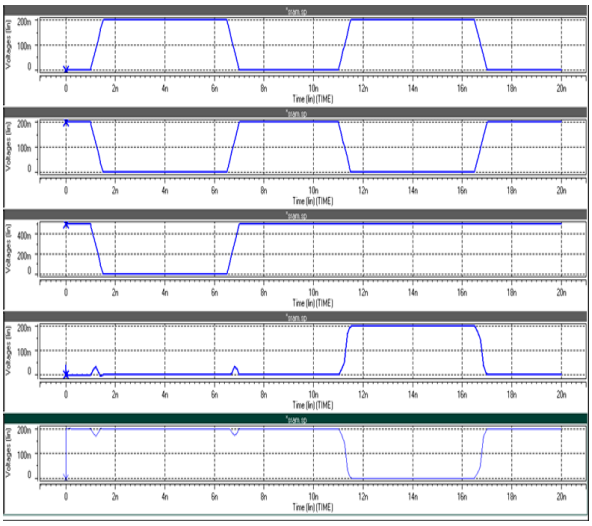

Figure 6. Heterojunction 6T SRAM write operation result

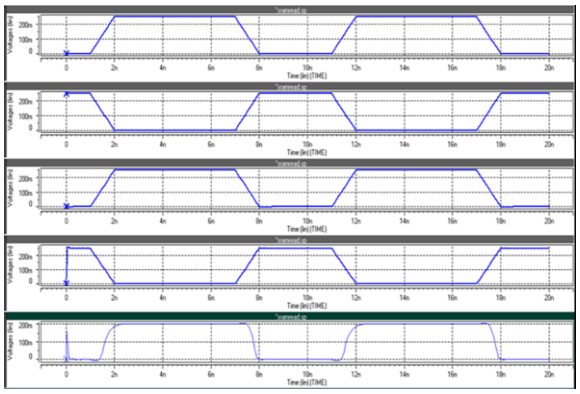

Figure 7. Homojunction TFET SRAM read operation result

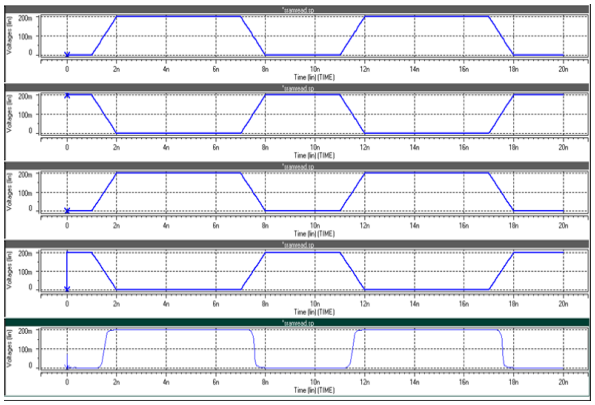

Figure 8. Heterojunction TFET SRAM read operation result

5. 3. Heterojunction vs Homojunction The sub-threshold slope of the device is very low if we use Heterojunction GaSb-InAs TFET. Heterojunction TFET has a small band-gap, when compared to the Homojunction TFET. Due to the small band-gap the charge carriers can move easily which enhances the speed of the transistor. Hence GaSb-InAs Heterojunction TFET is best for device fabrication because the power consumption and the propagation delay are very low is given in Table 1.

TABLE 1. Performance Comparison of Homojunction Vs Heterojunction

Circuit	Homo junction			Hetrojunction		
	Power (nW)	tpLH (ns)	tpHL (ns)	Power (nW)	tpLH (ns)	tpHL (ns)
SRAM Write	17.8	10.1	15.1	0.38	10.1	9.9
SRAM Read	208.2	9.9	0.18	1.87	0.0007	0.0128

5. 4. SRAM Operation Using 32nm Technology

5. 4. 1. Write Operation In the CMOS 32 nm SRAM write operation circuit, when the word line is ON (WL=1), the SRAM circuit allows the external input, to store the data. If WL=0, then the SRAM circuit keeps the previous data which is shown in Figure 9. The power of the 32nm CMOS SRAM is 0.704 nW.

5. 4. 2. Read Operation The CMOS 32nm SRAM read operation is done by using a sense amplifier which is used for reading the stored data from the memory device. For read operation the word line should be 0 (WL=0). Then, the output of the SRAM cell is connected as an input to the sense amplifier. The power of 32nm CMOS SRAM cell is 14.1 nW. Q and $\overline{Q}$ are the inputs of a sense amplifier and also the output of the SRAM cell. After writing the data into SRAM memory cell, the reading operation will take place. The simulation result of CMOS SRAM read operation is shown in Figure 10.

5. 4. 3. CMOS Vs TFET The heterojunction TFET SRAM and CMOS SRAM parameters are compared because it has already proved that Heterojunction is better than Homojunction. From Table 2, it is concluded that the TFET is better than the CMOS by comparing the parameters like power and propagation delay.

After comparison of CMOS, TFET and FINFET Technologies in Table 3, it is concluded that TFET is better than CMOS and FINFET. TFET gives very low sub-threshold swing at room temperature compared with CMOS and FINFET. TFET transistor shows higher performance than FINFET-based logic due to its lower parasitic capacitance. In addition, the leakage power of TFET is also reduced compared to FINFET and CMOS. Hence, TFET operates on high speed with low power, and low supply voltage.

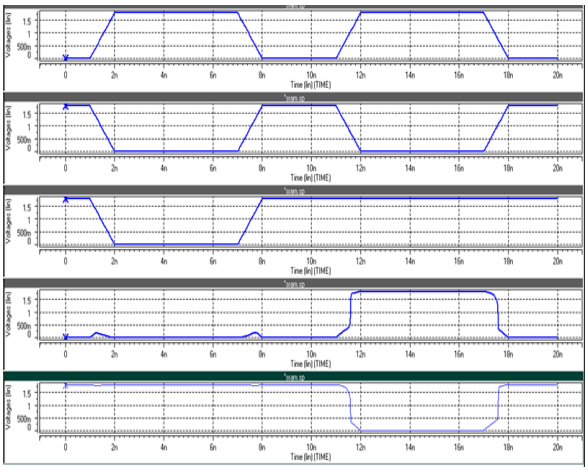

Figure 9. 6T CMOS SRAM write operation result

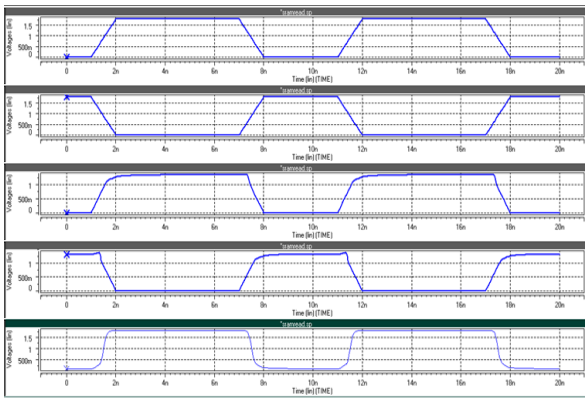

Figure 10. CMOS SRAM read operation result

TABLE 2. Performance Comparison of CMOS Vs TFET

Circuit	CMOS			TFET (Hetrojunction)		
	Power (nW)	tpLH (ns)	tpHL (ns)	Power (nW)	tpLH (ns)	tpHL (ns)
SRAM Write	0.704	10.2	10	0.38	10.1	9.9
SRAM Read	14.1	0.00095	0.0024	1.87	0.0007	0.0128

TABLE 3. Basic parameters values for CMOS, TFET and FINFET

Parameters	CMOS	TFET	FINFET
Channel Length	32 nm	30nm	22nm
Supply Voltage	1.8V	0.25V	0.9V
Threshold Voltage	0.53V	0.05V	0.36
Sub-threshold Slope	60mV/dec	17mV/dec	>70mV/dec
Leakage Power	1.74pW	0.39pW	0.98pW
I_{ON} (uA/um)	HVT 90 LVT 380	400	850

6. CONCLUSIONS

In this paper Heterojunction and Homojunction 6T SRAM cell is designed and simulated using TFET and it is observed that the Heterojunction SRAM cell performs better than the Homojunction in terms of speed and power consumption. Also, the performance of 30 nm TFET is compared with the 32 nm CMOS technology based on the various parameters such as channel length, supply voltage, threshold voltage, power and sub-threshold slope. Hence the proposed 6T-TFET SRAM offers better results than 6T-CMOS SRAM.

7. REFERENCES

1. Dhanasekar S, Ramesh J, "VLSI Implementation of Variable Bit Rate OFDM Transceiver System with Multi-Radix FFT/IFFT Processor for wireless applications", ***Journal of Electrical Engineering***, Vol. 3, No. 1, (2018), 1-10.
2. Emanuele Baravelli, Elena Gnani, Antonio Gnudi and Susanna Reggiani, "TFET Inverters with n-/p-devices on the same technology platform for low-voltage/low-power applications", ***IEEE Transactions on Electron Devices***, Vol. 61, No. 2, (2014), 473-478, doi: 10.1109/TED.2013.2294792
3. Anthony Villalon, Gilles Le Carval, Sebastien Martinie, Cyrille Le Royer, Marie-Anne Jaud and Sorin Cristoloveanu, "Further insights in TFET operation", ***IEEE Transactions on Electron Devices***, Vol. 61, No. 8, (2014), 2893-73-2898, doi: 10.1109/TED.2014.2325600
4. Yingxin Qiu, Runsheng Wang, Qianqian Huang and Ru Huang, "A comparative study on the impacts of interfece traps on tunneling FET and MOSFET", ***IEEE Transactions on Electron Devices***, Vol. 61, No. 5, (2014),1284-1291, doi: 10.1109/TED.2014.2312330
5. Siyuranga O. Koswatta, Mark S. Lundstrom and Dmitri E. Nikonov, "Performance comparison between p-i-n tunneling transistors and conventional MOSFETs", ***IEEE Transactions on Electron Devices***, Vol. 56, No. 3, (2009), 456-465, doi: 10.1109/TED.2008.2011934
6. Sung Hwan Kim, Sapan Agarwal, Zachery A Jacobson, Peter Matheu, Chenming Hu and Tsu-Jae King Liu, "Tunnel field effect transistor with raised germanium source", ***IEEE Electron Device Letters***, Vol. 31, No. 10, (2010), 1107-1109, doi: 10.1109/LED.2010.2061214
7. Ramanathan Gandhi, Zhixian Chen, Navab Singh, Kaustav Banerjee and Sungjoo Lee, "Vertical Si-Nanowire n-type tunneling FETs with low sub-threshold swing(<=50mV/decade) at room temperature", ***IEEE Electron Device Letters***, Vol. 32, No. 4, (2011), 437-439, doi: 10.1109/LED.2011.2106757
8. Dhanasekar S, Ramesh J, "FPGA Implementation of Variable Bit Rate OFDM Transceiver System for Wireless Applications", Proceedings of IEEE International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology, (2017), 343-346, doi: 10.1109/ICIEEIMT.2017.8116863
9. Chun-Hsing and Nguyen Dang Chien, "Sub-10-nm tunnel field-effect transistor with graded Si/Ge heterojunction", ***IEEE Electron Device Letters***, Vol. 32, No. 11,(2011), 1498-1500, doi: 10.1109/LED.2011.2164512
10. Rui Li, Yeqing Lu, Guangle Zhou, Qingmin Liu, Soo Doo Chae, Tim Vasen, Wan Sik Hwang, Qin Zhang, Patrick Fay, Tom Kosel, Mark Wistey, Huili Xing and Alan Seabaugh, "AlGaSb/InAs tunnel field-effect transistor with on-current of 78μA/μm at 0.5V", ***IEEE Electron Device Letters***, Vol. 33, No. 3, (2012), 363-365, doi: 10.1109/LED.2011.2179915
11. Ram Asra, Mayank Shrinivastava, Kota V. R. M. Murali, Rajan K. Pandey, Harald Gossner and V. Ramgopal Rao, "A tunnel FET for Vdd Scaling Below 0.6V with a CMOS-comparable performance", ***IEEE Transactions on Electron Devices,*** Vol. 58, No. 7,(2011), 1855-1863, doi: 10.1109/TED.2011.2140322
12. Lining Zhang and Mansun Chan, "SPICE modelling of double-gate tunnel-FETs including channel transports", ***IEEE Transactions on Electron Devices,*** Vol. 61, No. 2, (2014), 300-307, doi: 10.1109/TED.2013.2295237
13. Yoonmyung Lee, Daeyeon Kim, Jin Cai and Isaac Lauer, "Low-power circuit analysis and design based on hetero- junction tunneling transistors (HETTs)", ***IEEE Transactions Very Large Scale Integration Systems***, Vol. 21, No. 9, (2013), 1632–1643, doi: 10.1109/TVLSI.2012.2213103
14. Y.-N. Chen, M.-L. Fan, V. P.-H. Hu, P. Su, and C.-T. Chuang, "Design and analysis of robust tunneling FET SRAM", ***IEEE Trans. Electron Devices***, Vol. 60, No. 3, (2013), 1092–1098, doi: 10.1109/TED.2013.2239297
15. N. Hossain, A. Iqbal, H. Shishupal, and M. H. Chowdhury, "Tunneling transistor based 6T SRAM bitcell circuit design in sub-10nm domain",Proc. Midwest Symp. Circuits Syst., (2017), doi: 10.1109/MWSCAS.2017.8053215.
16. A. Sharma, A. G. Akkala, J. P. Kulkarni, and K. Roy, "Source-underlapped GaSb-InAs TFETs with applications to gain cell embedded DRAMs", ***IEEE Transactions on Electron Devices***, Vol. 63, No. 6, (2016), 2563–2569, doi: 10.1109/TED.2016.2555627
17. Ming-Hsien Tu, Jihi-Yu Lin, Ming-Chien Tsai and Chien-Yu Lu "A single-ended disturb-free 9T sub-threshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing", ***IEEE Journal of Solid-State Circuits***, Vol. 47, No. 6, (2012), 1469–1482, doi: 10.1109/JSSC.2012.2187474
18. Sebastiano Strangio, Pierpaolo Palestri, David Esseni, Luca Selmi and Felice Crupi, "Impact of TFET unidirectionality and ambipolarity on the performance of 6T SRAM cells", ***IEEE Journal of Electron Devices Society***, Vol. 3, No. 3, (2015), 223–232, doi: 10.1109/JEDS.2015.2392793
19. Dhanasekar S, Malin Bruntha P,Martin Sagayam K, "An Improved Area Efficient 16-QAM Transceiver Design using Vedic Multiplier for Wireless Applications", ***International Journal of Recent Technology and Engineering***, Vol.8, No. 3, (2019), 4419-4425, doi: 10.35940/ijrte.C5535.098319
20. Alan C. Seabaugh and Qin Zhang, "Low-voltage tunnel transistors for beyond low-voltage tunnel transistors for beyond CMOS logic", Proc. IEEE, Vol. 98, No. 12, (2015), 2095–2110, doi: 10.1109/JPROC.2010.2070470
21. Mahmood Uddin Mohammed and Masud H. Chowdhury, "Reliability and Energy Efficiency of the Tunneling Transistor-Based 6T SRAM Cell in Sub-10 nm Domain", ***IEEE Transactions on Circuits and Systems-II,*** Vol. 65, No. 12, (2018),1829-1833, doi: 10.1109/TCSII.2018.2874897
22. Jheng-Sin Liu,, Michael B. Clavel and Mantu K. Hudait, "An Energy-Efficient Tensile-Strained Ge/InGaAs TFET 7T SRAM Cell Architecture for Ultralow-Voltage Applications", ***IEEE Transactions On Electron Devices***, Vol. 64, No. 5, (2017), 2193-2200, doi: 10.1109/TED.2017.2675364
23. Sayeed Ahmad, Syed Afzal Ahmad, Mohd Muqeem, Naushad Alam and Mohd Hasan "TFET-Based Robust 7T SRAM Cell for Low Power Application", ***IEEE Transactions on Electron Devices***, Vol. 66, No. 9, (2019), 3834-3840, doi: 10.1109/TED.2019.2931567

Persian Abstract

چکیده

در این مقاله تحقیقاتی ، یک سلول ۱ بیتی SRAM بسیار کم مصرف با استفاده از ترانزیستور تاثیر Tunneling Field Effect (TFET) معرفی شده است. در این مقاله پیکربندی های SRAM٦T امکان پذیر در TFET های نوع N و P از نوع یکپارچه شده در هر دو سیستم عامل) InAsهم سازگاری) و GaSb-InAs (Heterojunction) بررسی شده است. مشخصات انتقال ولتاژ و پارامترهای اساسی هر دو همو و توابع هتروژن بررسی و مقایسه می شوند. SRAM مبتنی بر TFET پایداری در عملیات نگه داشتن ، خواندن و نوشتن را افزایش می دهد. این کار پتانسیل TFET را ارزیابی می کند که می تواند به دلیل بهبود عملکرد با مصرف کم انرژی ، سرعت زیاد ، شیب زیر آستانه کم و ولتاژ تغذیه (VDD = 0.2 ولت) جایگزین MOSFET شود. نتایج با فناوری CMOS 32nm در ارتباط است. سلول پیشنهادی SRAM TFET با استفاده از فناوری nm۳۰ پیاده سازی شده و با استفاده از شبیه ساز H-SPICE با کمک مدلهای Verilog-A شبیه سازی شده است. معماری سلول پیشنهادی SRAM TFET باعث اتلاف انرژی کم و عملکرد بسیار بالاتر در مقایسه با CMOS و FINFET می شود.