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# A Fast Processing Discontinuous Control Strategy for Vienna Rectifier

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In this paper, Vienna rectifier has been inspected as one of the prominent topologies among three-level switched-mode rectifiers. A fast processing discontinuous modulation strategy has been proposed with the aim of improving the rectifier's performance. The proposed method not only takes advantage of special properties available in three-phase three-level rectifiers, but also reduces the control design complexity and the switching loss. Moreover, neutral point voltage balancing is inherently realized. To achieve these goals, the rectifier is decoupled into two 2-level boost converters in every defined region, leading to simple modulation algorithm and fast processing control strategy. The validity of the proposed technique has been verified via simulation and experimental results conducted on a laboratory prototype.

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## 1. INTRODUCTION

Nowadays, power electronics is widely used in power conversion and power generation applications. Conventional power electronics converters have the disadvantages of low power factor and high current total harmonic distortion (THD), which are of significant concern in power quality aspect. Hence, Three-phase power factor correction active rectifiers are increasingly used in applications such as high voltage DC systems, uninterruptable power supplies, variable speed drives, etc. So far, several structures of three-phase active rectifiers have been introduced, all presenting some advantages and disadvantages in various applications [1-4]. Amongst three-phase active converters, Vienna rectifier, a non-regenerative three-level boost converter has been one of the most popular topologies due to its good performance and simple structure. The rectifier presents high power factor correction (PFC) performance, low electromagnetic interference (EMI), low voltage stress and low cost. Therefore, it can be used in medium voltage/high power applications such as telecommunication and wind energy conversion systems [3-6]. In addition, electric or hybrid vehicles, in which both power density and reduced weight are of the most importance, have been the potential applications of Vienna rectifier. The whole system configuration is shown in Figure 1.

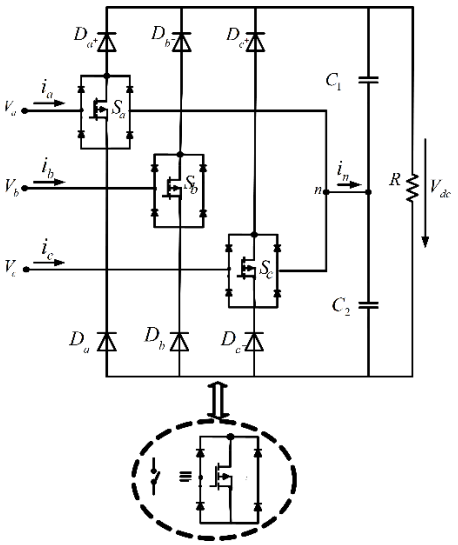


**Figure 1.** Vienna rectifier schematic diagram

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Up to now, various switching methods and control techniques have been addressed in the literature for Vienna rectifier, which are completely different from the conventional strategies, used for three-level rectifier structures. Space vector modulation (SVM) control strategy for Vienna rectifier is developed [7-9]. The voltage vector selection and calculation of the duration time are much more complicated than other strategies. The complexity and the computation burden is further increased due to the dependency of phase voltage to the input current direction.

In Carrier-based pulse width modulation (CB-PWM) method reported in literature [7, 8], two carrier waves are employed to realize the pulse width modulation (PWM). Neutral point potential is also balanced by adding offset signals to the phase reference voltages, which leads to continuous switching method, known as continuous PWM. Reference voltage generation is much easier compared with SVM strategy. However, its practical implementation is complicated in terms of synchronization of two carrier waves with same frequencies. Single-carrier wave PWM is realized to overcome the problem existing in CB-PWM, but still balancing DC-link voltage remains a challenge [10]. Hysteresis current controller introduced by Foureaux et al.[11], has the merit of fast dynamic response and simple implementation allowing the usage of minimum hardware. However, the controller presents inherent disadvantage of variable switching frequency, which is an issue in converter protection.

Most of the continuous PWM strategies can considerably satisfy the control objectives of Vienna rectifier. However, in case of Vienna rectifier, with satisfactory operational characteristics in high power applications, applying discontinuous approaches can significantly decrease the switching loss [12-14]. Discontinuous PWM (DPWM) methods are advantageous with respect to efficiency. When high efficiency is of the most importance, employing methods with lower switching loss seems practical [13]. SVM-based DPWM method is introduced within a limited range of modulation index [12]. Implementation of DPWM method based on SVM seems complicated using low performance microcontroller units, while high performance is achieved in the expense of more cost. Lee and Lee [14] developed a carrier-based DPWM strategy for Vienna rectifier. In this method, DC-link voltage balancing is realized through injection an offset to the phase reference voltages. This strategy offers simpler implementation than SVDPWM techniques. Yet, to satisfy the important requirement (IR) existing in Vienna rectifier, that is; the sign of the current should be the same as that of the input voltage, an additional offset calculation has to be performed to modify the reference voltage. A discontinuous space vector modulation (DSVM) method is proposed by Zhu et al. [15] for Vienna rectifier, in which the clamping area to the neutral point is varied by adding a clamping factor. In this condition, the optimum clamping area is defined and low-order harmonic contents in input currents will be reduced effectively.

In Vienna rectifier, the neutral point (NP) is connected to the input inductors via semiconductor switches. Though, DC-link voltage unbalance is the most challenging problem in converter control, since it results in high voltage stress on semiconductor devices and input current distortion. Hence, some considerations should be introduced to overcome the unbalance problem in the rectifier structure. A virtual space vector is introduced by Choudhury et al. [16] to control the fluctuations in the neutral point. The voltage of the capacitors in the DC-link is measured and an optimal switching sequence is selected and applied to three-level neutral-point clamped (NPC) inverter, based on a lookup table (LUT). Redundant switching states are used to control the NP voltage [17]. Here, voltage in the capacitors are measured and based on the current of the NP and an active or passive vector is selected; then, a switching table is proposed for the selection of the switching state to the NPCVSI for smooth switching criteria. However, an extra sensor in the experimental setup is still necessary. In most conventional control strategies for Vienna rectifier, an offset voltage injection or an extra feedback control loop including PI controller is modified to provide DC-link voltage regulation. An additional balancing leg including two extra MOSFET switches and an inductor, has been applied to the space vector modulated Vienna rectifier [18]. The relationship between the controlled duty cycle and the voltage unbalance is established through the state-space model of the system and based on this relationship, an optimal zero-sequence component for the duty cycle is found to achieve zero current injection to the DC-link neutral point [19]. Ma et al. [20] introduced a high-frequency model based on the relationship between the neutral point voltage and the AC currents. Here, the neutral point voltage balance is effectively managed by regulating the time of SVM redundant small vector pair during a duty cycle.

Another limitation existing in Vienna rectifier is the current distortion occurring at current zero-crossing points due to the dependency of the rectifier voltage to the current polarity. If one of the phase currents crosses zero during a switching period, any phase in which the corresponding switch is off, will produce an erroneous voltage of opposite polarity from what was intended by the control. Consequently, a current spike will appear at the vicinity of current zero-crossing, which results in grid current distortion and EMI Interference. The challenge will be avoided by clamping the related phase to zero. To achieve this goal, Johnson and Aliprantis [21] proposed a modified SVPWM scheme by using the certain state

combinations of short vectors in each sector. In this method, the calculation of duty ratio will not be affected by the direction of phase, current near the zero-crossing point and therefore the current distortion will be eliminated.

A control technique is proposed, based on an analysis of the switching dynamics near current zero crossing for Vienna rectifier in Wind Turbine application [22]. Here, the current ripple, induced by PWM, is calculated and the maximum angular deviations of the current space vector from the fundamental are found. Hence, the timing of the clamping signal will be determined. An improved optimal switching sequence model predictive control (OSS-MPC) strategy based on SVM is presented for Vienna rectifier, in which the control objective is shaping of the rectifier input currents [23]. Since rectifier side voltages are dependent on input currents direction, hence, applying appropriate switching sequence and voltage vectors are inevitable. Moreover, DC-link voltage regulation and the neutral-point voltage balancing are realized by a PI control and a redundant vector pre-selection technique, respectively. However due to SVM switching method, the implementation of the controller still remains as a challenge.

In this paper, a novel discontinuous PWM method, based on circuit level decoupling (CLD) concept is introduced for Vienna rectifier. In the proposed method, Vienna rectifier is decoupled into two two-level separately controlled boost converters in every 60˚ region, in which the closed loop controller design can be simplified to the control of DC-DC converters. The salient features of the proposed strategy are as follow: 1) In the proposed method, Vienna rectifier is decoupled into two two-level separately controlled boost converters in every *60˚* region, in which the closed loop controller design can be simplified to the control of DC-DC converters. 2) The proposed strategy has the merit of using just one carrier-wave for modulation action. 3) Since one of three switches are not operated at any instant, the switching loss is reduced by one-third. 4) The DC-link capacitor voltages are inherently balanced with no requirement for extra control action. Hence, a fast processing controller is achieved. In section 2, the detailed analysis of the proposed PWM modulation strategy for Vienna rectifier is given. The effect of the proposed control on the capacitor voltage balancing is discussed in section 3. Finally, simulation and experimental verification is presented in section 4.

## 2. PRINCIPLE OF THE PROPOSED PWM MODULATION STRATEGY

Vienna rectifier structure consists of three semiconductor switches ($S_a$, $S_b$ and $S_c$), low loss silicon carbide diodes and DC-link capacitors ($C_1$ and $C_2$) as shown in Figure 1. The detailed operations of the Vienna rectifier is discussed in literature [24]. Sinusoidal input current, desired output voltage, and balanced capacitor voltages are achieved based on the switching pattern applied on $S_a$ , $S_b$ and $S_c$. The rectifier side voltages ($V_{an}$ , $V_{bn}$ and $V_{cn}$) depend on the switching states of switches and polarity of the input currents and are expressed as follows:

$$V_{an}=\frac{V_{dc}}{2}\text{sgn}(i_a)(1-S_a)$$
$$V_{bn}=\frac{V_{dc}}{2}\text{sgn}(i_b)(1-S_b) \quad (1)$$
$$V_{cn}=\frac{V_{dc}}{2}\text{sgn}(i_c)(1-S_c)$$

where; and $V_{dc}$ is the rectifier's output voltage, $S_a$, $S_b$, and $S_c$ are the switching states of the switches ($S_a$; $S_b$; $S_c=1$ when switches are on and $S_a$; $S_b$; $S_c=0$ when switches are off).

In this paper, a discontinuous PWM method with the circuit-level decoupling concept has been proposed for Vienna rectifier, based on the existing strategy for three-level NPC inverters [25]. The proposed control method is described through the following sections.

**2. 1. Circuit-Level Decoupling Concept** Three-phase input voltages ($V_a$, $V_b$ and $V_c$) are shown in Figure 2. According to the figure, each phase voltage can be divided into 6 regions per fundamental cycle. Inspecting three-phase voltages in each 60˚ region, one common fact is that, there is a sign transition in one phase voltage while the sign of the other two voltages is remained unchanged. Considering this fact, the switch with transitional phase voltage is always kept on during the whole 60˚ region, whereas the remaining phase switches will be modulated with duty cycles ($d_p$ and $d_n$). That means; just two of the three switches in the converter is pulse width modulated at any instant. Hence, compared with continuous strategies, the number of turning-on and turning-off times of each switch and its corresponding diode in bridge structure, will decrease by a factor of 1/3. Applying the above analysis, the rectifier equivalent circuit for region I, is presented in Figure 3. As seen in the figure, since the voltage of phase ($a$) has transitional sign, its corresponding switch ($S_a$) is kept on during the entire period. Likewise, the voltage in phase ($c$) is positive during the whole region and $S_1$ is switched

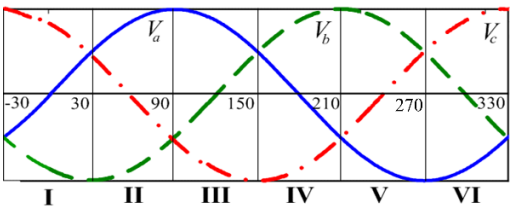


**Figure 2.** Three phase input voltages

between *p* and *n*. While, the voltage of phase (*b*) is always negative and $S_2$ will be switched between *N* and *n*.

Since the switching frequency is much higher than the fundamental frequency, Vienna rectifier circuit can be decoupled into two two-level DC-DC boost converters during each *60°* region as in Figure 4. Duty cycles for switches in phase (*c*) and (*b*) can be defined as $d_p$ and $d_n$:

$$d_p = \frac{T_{0S_1}}{T_{sw}} \quad , \quad d_n = \frac{T_{0S_2}}{T_{sw}} \tag{2}$$

where; $T_{0_{Si}}\,(i=1,2)$ is the on-time of each switch and $T_{sw}$, is the switching period.

**2. 2. Analysis of Decoupled Converters** As shown in Figure 2, for the period *(-30°~0°)*, the absolute value of phase (c) voltage is higher than that of phase (b) and thus, $(d_p < d_n)$. The opposite is found during *(0°~30°)*. Regarding the above relation between $d_p$ and $d_n$, two different switching sequences must be applied on decoupled converters, during each switching cycle; 1,2,4 for ($d_p < d_n$) and 1,3,4 for ($d_p > d_n$). The switching sequences and the resulting inductor voltages in region I are summarized in Table 1.

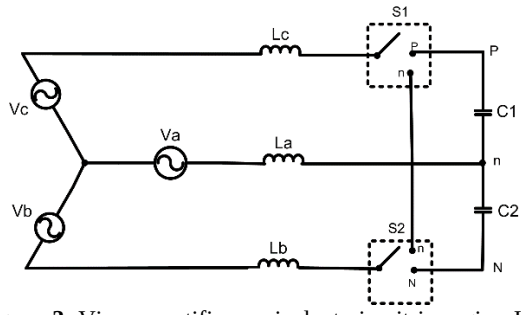


**Figure 3.** Vienna rectifier equivalent circuit in region I; (-30°~30°)

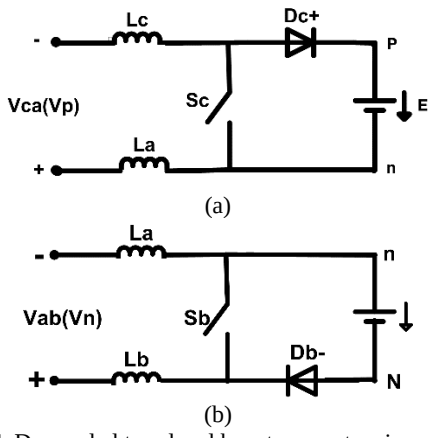


**Figure 4.** Decoupled two-level boost converters in region I; (-30°~30°)

**TABLE 1.** Switching states and inductor voltages in region I

| Switching States | $S_b$ | $S_c$ | $V_{Lb}$ | $V_{Lc}$ | $V_{La}$ |
|---|---|---|---|---|---|
| 1 | on | on | $V_b$ | $V_c$ | $V_a$ |
| 2 | on | off | $V_b+\frac{1}{3}E$ | $V_c-\frac{2}{3}E$ | $V_a+\frac{1}{3}E$ |
| 3 | off | on | $V_b+\frac{2}{3}E$ | $V_c-\frac{1}{3}E$ | $V_a-\frac{1}{3}E$ |
| 4 | off | off | $V_b+E$ | $V_c-E$ | $V_a$ |

To give a better illustration of the analysis carried out, the extraction process of inductor voltages is presented below.

Considering the decoupled circuits in Figure 4, KVL equations for switching state (2) are written as follow:

$$-V_c + L\frac{di_c}{dt} - L\frac{di_a}{dt} + V_a + E = 0 \tag{3}$$

$$-V_a + L\frac{di_a}{dt} - L\frac{di_b}{dt} + V_b = 0 \tag{4}$$

In above equations, parameter '*E*' represents DC-link voltage and $i_i(i=a,b,c)$ are the rectifier input currents.

Assuming the three-phase input voltages and currents to be symmetrical, the inductor voltages, are extracted for region I:

$$V_{La} = V_a + \frac{1}{3}E\,,\, V_{Lb} = V_b + \frac{1}{3}E\,,\, V_{Lc} = V_c - \frac{2}{3}E \tag{5}$$

Accordingly, duty cycles of the switches will be obtained through applying volt-second balance to the inductors during a switching cycle, as:

$$\begin{cases} V_c d_n + \left(V_c - \frac{1}{3}E\right)\left(d_p - d_n\right) + \left(V_c - E\right)\left(1 - d_p\right) = 0 \\ -V_b d_n + \left(-V_b - \frac{2}{3}E\right)\left(d_p - d_n\right) + \left(-V_b - E\right)\left(1 - d_p\right) = 0 \\ V_a d_n + \left(-V_a - \frac{1}{3}E\right)\left(d_p - d_n\right) + V_a\left(1 - d_p\right) = 0 \end{cases} \tag{6}$$

$$\Rightarrow \begin{cases} d_p = \dfrac{E - (2V_c + V_b)}{E} \\ d_n = \dfrac{E - (-V_c - 2V_b)}{E} \end{cases}$$

The same analysis has been extended to other switching states and regions, which are eliminated here to avoid tedious calculations.

**2. 3. Implementation of the Proposed Switching Strategy** Implementation process of the proposed method is illustrated in Figure 5 and is divided into 4 major blocks: Region selector, Modulation Signal Selector (MSS), PWM unit, Duty Cycle Allocator (DCA). The active operating region is determined

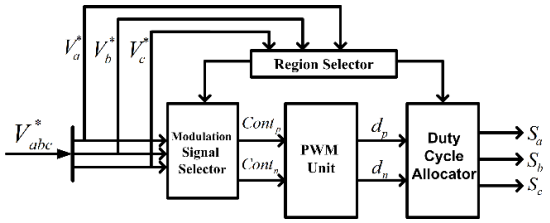


**Figure 5.** Schematic diagram of the proposed CLD-DPWM switching strategy

through observation of the input reference voltages ($V^*_{abc}$) in region selector. $Cont_p$ and $Cont_n$ signals are derived from MSS block based on the active operating region number and the information listed in Table 2. The resulting modulation signals are then compared with carrier wave in PWM unit and the duty cycle signals $d_p$ and $d_n$ are obtained. The duty cycles are evaluated through applying a simple PWM technique on two decoupled boost converters in each region. These signals are then allocated to the switches $S_a$, $S_b$ and $S_c$ in DCS block, according to the information acquired from region selector. Assignment of duty cycles ($d_p$, $d_n$ *and* $d_t$) along with the derivation of the modulation signals ($Cont_p$ and $Cont_n$) are listed in Table 2 for each region. $d_t$=1 is allocated to the switch with on state during each region. Taking into account the analysis conducted in Table 2, algorithm of the modulator is so simple and the modulation is performed using just one carrier wave. Accordingly, the implementation can be processed very quickly in comparison to the conventional methods such as SVPWM and CB-PWM strategies. It is worth mentioning that the proposed control algorithm imposes more boosting voltage than other modulation strategies. For instance, considering region I in Figure 2, the following condition should be met:

$$\frac{V_{dc}}{2} > V_{ca_{\max}} \tag{7}$$

which occurs at $\omega t=30°$ and minimum voltage over positive boost converter (Figure 4 (a)) is obtained as:

$$\left.\frac{V_{dc}}{2}\right|_{\min} = V_m \sin(\omega t+120) - V_m \sin(\omega t) = \frac{3}{2}V_m \tag{8}$$

Thus, the minimum output DC voltage will be:

$$V_{dc_{\min}} = \sqrt{3}V_{LL_{\max}} \tag{9}$$

where, $V_m$ is the peak phase voltage and $V_{LLmax}$ is the peak line voltage. As in Equation (9), $V_{dcmin}$ is 73% more than the line voltage obtained through other existing modulation strategies for Vienna rectifier presented in literature [7-11,14,15], which makes the structure compliant with high voltage industrial installations.

### 2. 4. Implementation of the Closed-Loop Control

The whole closed-loop control structure is presented in Figure 6, which consists of two control loops; the inner current loop providing sinusoidal input current and the outer voltage loop applied to achieve fixed voltage at the rectifier output. As observed in Figure 6, in the proposed method the feedback control loop for capacitor voltage regulation is remove due to the inherent self-balancing capability of the method. In Figure 6, the reference current amplitude is derived based on the error between the DC voltage reference ($V^*_{dc}$) and its measured value ($V_{dc}$) in voltage controller block, which then is passed through a PI controller. The angle of the three-phase grid voltage is derived through the PLL block, which is used to generate the current reference ($i^*_{abc}$) in phase with $V_{abc}$.

Input current error is then passed through a proportional controller, providing the reference signals ($V^*_{abc}$) for the proposed CLD-DPWM method. The controller parameters are chosen based on error and trial method as: $K_{pv}$=*0.016*, $K_{iv}$=*3*, $K_{pi}$=*0.2*. where, $K_{pv}$ and $K_{iv}$ are the voltage controller and $K_{pi}$ is the current controller parameters. It should be mentioned that under the above controller design, the rectifier output voltage can be reached in the range of:

$$1.73V_m < V_{dc} < 6.7V_m \tag{10}$$

As for the closed-loop controller design, the design methods for DC-DC converters can be utilized easily to implement the output voltage control of the three-level Vienna rectifier, due to the circuit decoupling concept.

## 3. NUETRAL POINT SELF-BALANCING ABILITY

Referring to decoupled circuit for Vienna rectifier in Figure 4, it can be found that positive boost rectifier will transfer its energy to $C_1$, while the negative boost rectifier will transfer its energy to $C_2$. As a result, an equal power is transferred to $C_1$ and $C_2$ during a fundamental cycle and though, DC-link capacitors will be naturally balanced. The following mathematical analysis is carried out as a proof to the fact. When a switch is turned on and clamped to the neutral point, the corresponding phase current is conducted into or drawn out from the neutral point. In consequence, the neutral point voltage will deviate from zero. The mean value of the neutral point current during a modulation period can be obtained as follows:

$$i_n = d_{a0}i_a + d_{b0}i_b + d_{c0}i_c \tag{11}$$

here, $d_{i0}$ *(i=a,b,c)*; is the time ratio of the associated switch. For instance, in region I, switches in phase (*b*) and (*c*) are controlled via $d_p$ and $d_n$. While, the switch in phase (*a*) is always kept on and connected to the neutral point for the entire period, that is; $d_{a0}$=1. Taking into account Table 2 and Equation (11), the following formula will be met in region I:

**TABLE 2.** Derivation of switching signals

| Region | $V_p$ | $V_n$ | Control Signal Selector | | Gate Signal Distributor | | |
|---|---|---|---|---|---|---|---|
| | | | $Cont_p$ | $Cont_n$ | $d_p$ | $d_n$ | $d_t=1$ |
| **I** | $V_{ca}$ | $V_{ab}$ | $E-(2V_c+V_b)$ | $E-(-V_c-2V_b)$ | $S_c$ | $S_b$ | $S_a$ |
| **II** | $V_{ac}$ | $V_{cb}$ | $E-(2V_a+V_b)$ | $E-(-V_a-2V_b)$ | $S_a$ | $S_b$ | $S_c$ |
| **III** | $V_{ab}$ | $V_{bc}$ | $E-(2V_a+V_c)$ | $E-(-V_a-2V_c)$ | $S_a$ | $S_c$ | $S_b$ |
| **IV** | $V_{ba}$ | $V_{ac}$ | $E-(2V_b+V_c)$ | $E-(-V_b-2V_c)$ | $S_b$ | $S_c$ | $S_a$ |
| **V** | $V_{bc}$ | $V_{ca}$ | $E-(2V_b+V_a)$ | $E-(-V_b-2V_a)$ | $S_b$ | $S_a$ | $S_c$ |
| **VI** | $V_{cb}$ | $V_{ba}$ | $E-(2V_c+V_a)$ | $E-(-V_c-2V_a)$ | $S_c$ | $S_a$ | $S_b$ |

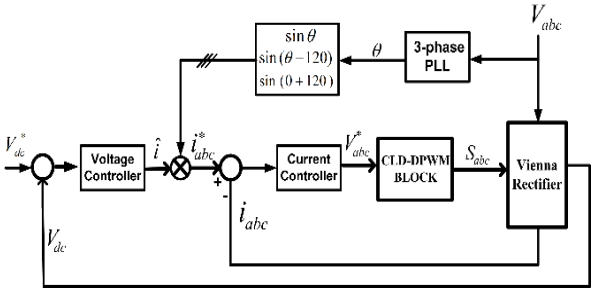


**Figure 6.** The whole closed-loop control system

$$\begin{aligned} i_{n_I} &= d_p \times i_c + i_a + d_n i_b \\ &= \left[1-(2V_c+V_b)\right]\times i_c + 1\times i_a + \left[1-(-V_c-2V_b)\right]\times i_b. \end{aligned} \quad (12)$$

where; $i_{nI}$ is the average neutral point current during region I. The above equation can be generalized for regions (II-VI). The summation of average neutral point currents related to all six regions ($i_n$), is given below:

$$i_n = \sum_{x=I}^{VI} i_{n_x} = 0 \quad (13)$$

Equation (13) indicates that due to the proposed method, no current is injected into the neutral point during a fundamental cycle and hence, DC-link capacitors are naturally balanced with no requirement for an extra feedback loop.

## 5. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the performance of the proposed CLD-DPWM technique, a 600 W Vienna rectifier is simulated in MATLAB/Simulink and the simulation parameters are listed in Table 3. Rectifier's 3-phase input current and its harmonic spectrum are illustrated in Figures 7 and 8, respectively. It can be observed from the figure that the input current is completely spike-free specially at zero-crossing points, since the phase with near-zero current is clamped to the neutral point by keeping its switch on and hence, the impact of current direction on rectifiers voltage will be eliminated. The rectifier input current in the proposed method, like other existing discontinuous approaches, is subjected to distortion and its THD is slightly increased in comparison to the continuous strategies [14]. According to Figure 8, the input current harmonic distortion in the proposed method is 2.87%, which satisfies IEEE 519 (i.e. max. of THD for each order: 5%). Consequently, taking into account the aforementioned advantages of the proposed method, this minor increase in THD can be justified. It should be noted that in Figure 8, the fundamental component bar exceeds the limits due to the better illustration of other harmonic contents. The corresponding waveforms of single phase input voltage/current and DC output voltage are shown in Figure 9. In the presence of the proposed discontinuous switching strategy, the unity power factor is achieved and IR is satisfied with no need for additional actions. Moreover, the DC bus voltage accurately tracks the reference and the voltage ripple will be kept within less than 1%. Phase (a) voltage on both the grid side and the switch side are shown in Figure 10. As in the figure, the switch side voltage is clamped to *(-Vdc/2), 0, (+Vdc/2)*.

**TABLE 3.** Parameters used in simulation

| | |
|---|---|
| **Input line voltage** | $V_{L\text{-}L}$=122 V |
| **Input inductor** | L=3 mH |
| **DC-link capacitor** | $C_1$,$C_2$=1300 μF |
| **DC-link reference voltage** | $V_{dc}$=300 V |
| **Switching frequency** | $f_s$=10 kHz |
| **Line frequency** | $f_m$=50 Hz |
| **Load resistance** | $R_L$=150 Ω |

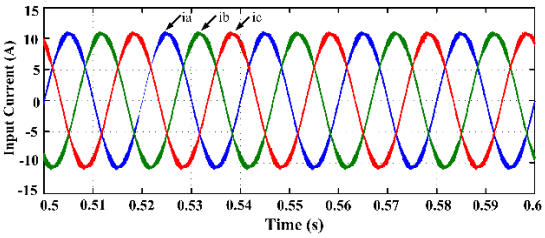


**Figure 7.** Three phase grid current

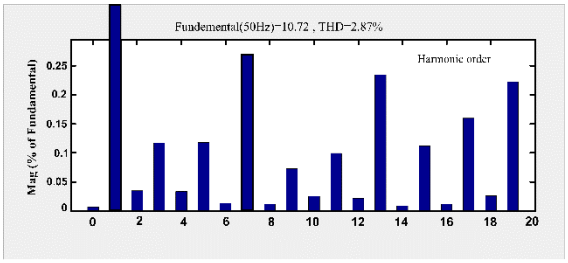


**Figure 8.** FFT analysis of the proposed DPWM method

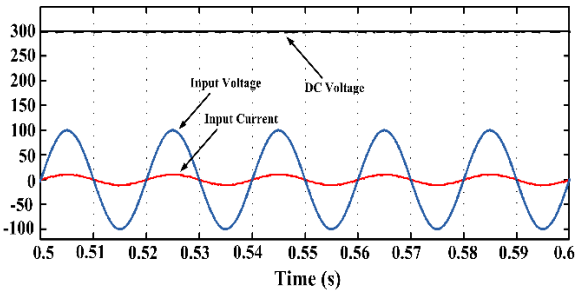


**Figure 9.** Simulation results for: (a) input current and voltage, (b) DC-link voltage

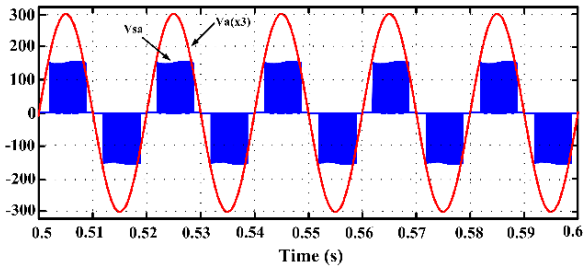


**Figure 10.** Waveform of (a) input phase voltage and phase voltage over switches

Furthermore, since the phase with transitional state is clamped to zero during each 60˚ region, two zero intervals occur in the switch side voltage waveform during each switching cycle. DC-link voltages $V_{C1}$ and $V_{C2}$ are also presented in Figure 11. As in the figure, the capacitor voltages are essentially well-balanced without any balancing feedback loop. Figure 12 shows the dynamic balancing process in which the initial voltages on DC-link capacitors are unbalanced as $V_{C1} = 200\ V$ and $V_{C2} = 100\ V$, which converge after a very short time interval. To further verify the effectiveness of the proposed control strategy, a 253 W experimental prototype is built at laboratory scale. The power stage consists of Dual Common Cathode Ultrafast Rectifiers (FEP30J) and Si MOSFETs (IRFP260N), and the control system is executed in MCU TMS320F28335 DSP with the switching and sampling frequency of 10 kHz. The input voltage is 40 Vrms/50 Hz and the input inductors are 5 mH. The two DC-link capacitors connected in series at the DC-side are 1360 µF, and the load resistance is 145 Ω. Moreover, the DC reference voltage is 190 V. Figure 13 presents grid voltage and input current in phase (*a*). The figure verifies the simulation results in terms of power factor and current distortion at zero-crossing points. The current THD of 4.46% under modulation index of 0.5968 have been achieved from experimental prototype, which also assures IEEE519 standard.

Moreover, as seen in the figure, under the proposed modulation algorithm the unity power factor is realized without applying any modifications on switching signal. Figure 14, illustrates the experimental results of phase (*a*) current, line to line voltages at the grid side ($V_{ab}$) and the switch side ($V_{AB}$). The five-level characteristic of $V_{AB}$ is apparent from the waveform. As in the figure, the voltage levels of $\pm 95\ V$, $0$, $\pm 190\ V$ are obtained under $190\ V$ reference voltage. Figure 15 shows the experimental results of DC-link voltages; $V_{c1}$, $V_{c2}$ and $V_{dc}$. The waveforms well prove the self-balancing behavior of the proposed method, since the output voltage is controlled in $190\ V$ reference voltage and the capacitor voltages are both balanced in $95\ V$.

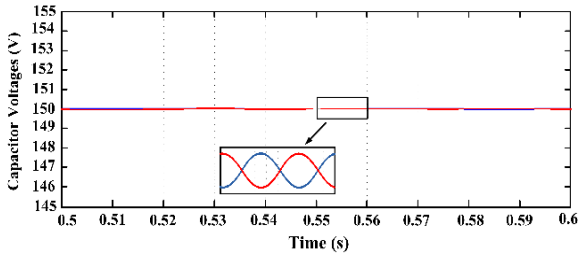


**Figure 11.** Averaged voltages across the capacitors $C_1$ and $C_2$ along with their ac voltage ripple

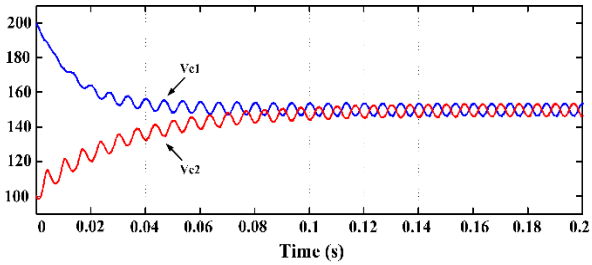


**Figure 12.** Dynamic balancing process of capacitors with initial voltage $V_{C1} = 200\ V$ and $V_{C2} = 100\ V$

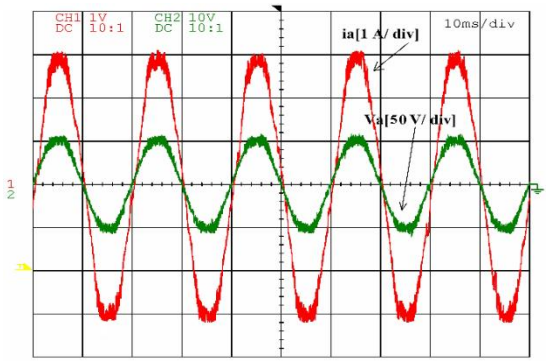


**Figure 13.** Experimental results of grid voltage and input current in phase (*a*)

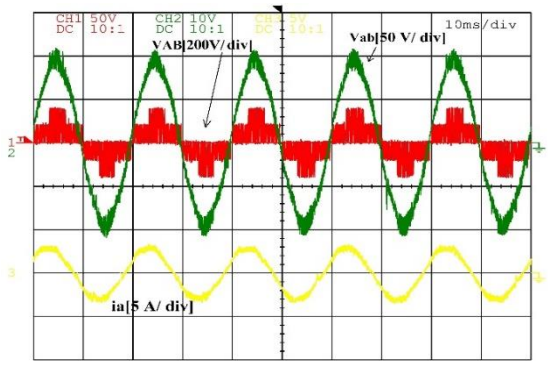


**Figure 14.** Experimental results of phase (*a*) current, line to line voltage at the grid side ($V_{ab}$) and the switch side ($V_{AB}$)

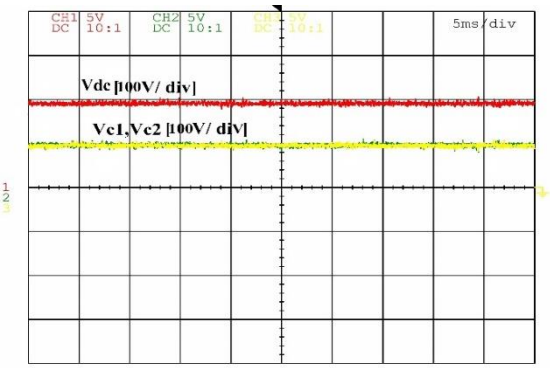


**Figure 15.** Experimental waveforms of DC-link voltages; $V_{c1}$, $V_{c2}$ and $V_{dc}$

## 6. CONCLUSION

This paper has developed a simple and fast-processing modulation strategy for three-phase three-level Vienna rectifier. The proposed strategy employs circuit-level decoupling concept and is able to decouple the rectifier structure into two 2-level boost converters in every predefined region. This method is fully compatible for industrial applications such as, variable speed drives, high voltage DC systems and renewable energy systems where high power and low switching loss are essential. The main features of this strategy compared to other conventional three level ones are its simple and fast implementation, average NP voltage self-balancing, and low switching loss. Furthermore, current zero crossing distortion, which is problematic due to the generation of erroneous voltage vectors in Vienna rectifier, is inherently removed due to the switching scheme. The above capabilities of the proposed method is well verified through simulation and experimental tests on a 253 W and 10 kHz laboratory prototype.

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## Persian Abstract


**چکیده**

در این مقاله، یکسوساز وینا، به عنوان یکی از ساختارهای محبوب در میان یکسوسازهای سه‌سطحی مبتنی بر کلیدزنی، مورد بررسی قرار گرفته‌است. یک استراتژی مدولاسیون ناپیوسته با قابلیت پردازش بسیار سریع و با هدف بهبود عملکرد یکسوساز وینا ارائه گردیده‌است. روش پیشنهادی، نه‌تنها از مزایای یکسوسازهای سه‌فاز سه‌سطحی بهره برده‌است، بلکه از پیچیدگی کنترل و تلفات کلیدزنی نیز کاسته و قابلیت متعادل‌سازی ذاتی ولتاژ نقطه خنثی را نیز دارا می‌باشد. به‌منظور دستیابی به اهداف فوق‌الذکر، ساختار یکسوساز در هر ناحیه تعیین شده، به دو مبدل بوست دوسطحی تجزیه می‌گردد که در نتیجه آن، الگوریتم مدولاتور ساده شده و حلقه کنترلی با سرعت بالاتری پردازش خواهد شد. صحت روش پیشنهادی، به‌واسطه شبیه‌سازی و نتایج تست عملی برروی نمونه آزمایشگاهی مورد راستی‌آزمایی قرار گرفته‌است.