International Journal of Engineering

Journal Homepage: www.ije.ir

A High Gain Bipolar Pulse Generator with Low Voltage Input Source

H. Gholamalitabar[a], J. Adabi*[a], M. Rezanejad[b]

[a] *Department of Electrical and Computer Engineering, Babol Noshirvani University of Technology, Babol, Iran*
[b] *Department of Electrical and Computer Engineering, University of Mazandaran, Babolsar, Iran*

PAPER INFO

Paper history:
Received 30 May 2019
Received in revised form 21 July 2019
Accepted 28 July 2019

Keywords:
Bipolar Pulsed Power Generator
Switched-Capacitor
Modular
Marx Generator

ABSTRACT

This paper proposes a pulsed power generator which consists of two types of switched-capacitor booster modules. A doubling mode module employed to elevate the input voltage to a specified level and, constant mode module is used to increase the elevated voltage into the finally intended bipolar output voltage. Also, the proposed modular structure does not utilize any switches across the load. Other advantage of the proposed structure is its lower current stress on source and every circuit component near it. In comparison with Marx Generator (MG) based topologies, the number of circuit components has been significantly reduced, which led to cost-saving and prevention of circuit control complexity. Calculation of the capacitors is presented. Experimental tests and simulations are performed on a five-module system which confirms the high performance of the proposed topology.

***doi**: 10.5829/ije.2019.32.08b.08*

1. INTRODUCTION

The major concept of the pulsed power technology is receiving energy from input sources, storing it in energy storage components and generating high voltage/current pulses for the loads which requires high instantaneous power pulses [1]. Gradually, various industrial and environmental applications led to the development of this complicated technology [2, 3]. Marx generator pulsed power supplies [4], magnetic pulse compressors [5], pulse formation network [6] and multistage Blumlein [7] are among the famous conventional pulse generation methods.

The invention of the power electronics semiconductor devices has led to the introduction of new pulsed power supplies. More accurate pulse magnitude and frequency regulation is one of their most important features. However, restrictions in tolerable voltage of semiconductor elements should be considered as one of their drawbacks [8]. Boost [9, 10], Buck-boost [8], Push-pull [11], Fly back [12] DC-DC converters are the main categories of the pulsed power generating topologies using semiconductor devices. These structures are simple but the high volume cores of its transformers and inductors may make it excessively heavy and large. Resonance converters [13] are also applied in this field of applications. One of the advantages of these type of converters is its higher efficiency compared to other power electronics based pulse generators, while low precision in controlling performance and output voltage is its major limitation.

In order to cover these limitations, multi-stage and modular switched-capacitor structures were developed as a solution that can provide design and control simplicity as well as the low nominal voltage of semiconductor components. Therefore, modular switched capacitor generators are highly considered due to their lack of transformers or inductors [14]. The main topologies of this type of switched- capacitor structures are mentioned below: MG based topologies is the main subset of modular switched-capacitor structures in which components tolerate the same voltage as the input voltage source [15-17]. This structure is practical and cost-efficient for medium and high voltage input sources (depending on the voltage rating of circuit components especially power semiconductors). Additionally, capacitor switched voltage multiplier (CSVM) were introduced to boost the low input voltage source and

*Corresponding Author Email: *j.adabi@nit.ac.ir* (J. Adabi)

Please cite this article as: H. Gholamalitabar, J. Adabi, M. Rezanejad, A High Gain Bipolar Pulse Generator with Low Voltage Input Source, International Journal of Engineering (IJE), IJE TRANSACTIONS B: Applications Vol. 32, No. 8, (August 2019) 1126-1133

achieve a high voltage output pulse. Decreasing the number of power semiconductors is the main advantage of CSVM topologies. They are mainly used for the applications with lower voltage input sources where employing Marx structure may lead to an increment of a number of circuit components [18]. On the other hand, Modular Multilevel Converters (MMC) based circuits is also used for pulsed power generation. The main advantages of these topology are low current spike resulted from sequential charging, the flexibility of control over the maximum reverse voltage of the semiconductors. However, the urge for utilizing high voltage switch across the load is their main drawback [19].

After studying the requirements of a standard structure, it seems that MG based structures is the best-switched capacitor topology. However, for the applications with low voltage input sources, MG structures may utilize a large number of modules which lead to control complexity and also higher costs. The most convenient solution for these kind of problems is using multipliers which not only leads to a remarkable reduction of circuit devices but also facilitates the control process. In order to propose a new structure, a combination of MG structure, multipliers, and modular multilevel converters is used to sum up all of their advantages. Of course, unlike MG structures, the reverse voltage on switching components may be several times of the input voltage. This is not a problem until it does not exceed the rated voltage value of the circuit elements. For this purpose, a new structure is presented whose modules have the capacity of increasing voltage with a gain greater than one.

The rest of the paper is organized as follows. In section 2, the proposed module is introduced and the method of achieving the modular structure is discussed. In section 3, the proposed structure will be compared with the other structures in terms of their advantageous and disadvantageous. Finally, the simulation, experimental results, and conclusion are covered in section 4.

2. PROPOSED TOPOLOGY: STRUCTURE AND OPERATING PRINCIPLES

2. 1. Proposed Module Figure 1 shows the basic structure of the proposed SC module for voltage doubling, which includes two capacitors, two switches, and two diodes. The related charging strategy for this module makes the voltage of the $(k+1)^{th}$ module twice as much as the voltage of the k^{th} module. Thus, as shown in Figure 2, each capacitor of the $(k+1)^{th}$ module should be charged by two capacitors of the k^{th} module. For charging upper (lower) capacitors of $(k+1)^{th}$ module, lower (upper) switches of this module have to be turned on.

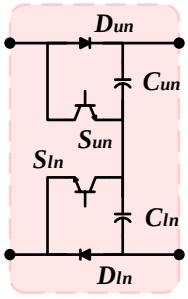


Figure 1. Proposed SC module for voltage doubling

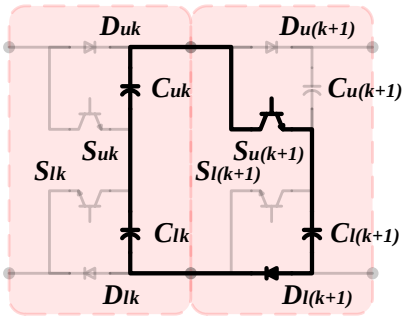
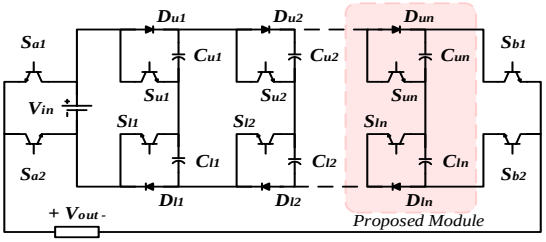


Figure 2. The charging paths for voltage doubling

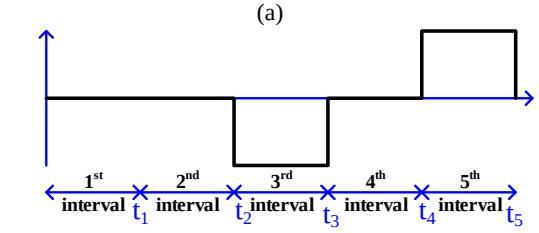
It should be considered that in each module, the voltage of each capacitor cannot drop to less than 50% of the intended voltage. Also, during the charging procedure one switch and one diode of the module is in the path.

2. 2. Operating Principles Figure 3.a shows the configuration of the proposed pulsed power generator for n modules. This structure consists of two half-bridge converters and a few switched capacitors cells in between which are connected together in series. The capacitors' charging method for the proposed structure is in a way that its current stress is lower than MG structures. Using the input voltage source in forming output pulse is another feature of this topology. Moreover, the switches do not tolerate negative voltage when they are off. As a result, there is no need to use any series diodes along with the switches.

Figure 3.b shows the output voltage pulse of a three-module system in a switching cycle and the switching states of all switches. Note that based on the shape of the required pulse, the order of switching can be rearranged. There are two charging (see Figures 4.b and 4.c) and two discharging states (see Figure 5) which have to be inserted in a switching cycle. In order to show the performance of the proposed structure, a three-module sample is investigated (see Figure 4.a). Figure 4.b shows the upper capacitors charging paths. All upper capacitors are simultaneously charged in a way that the voltage of each capacitor is the sum of two capacitors voltages from the previous module. Similarly, lower capacitors are charged with the equivalent circuit of Figure 4.c.



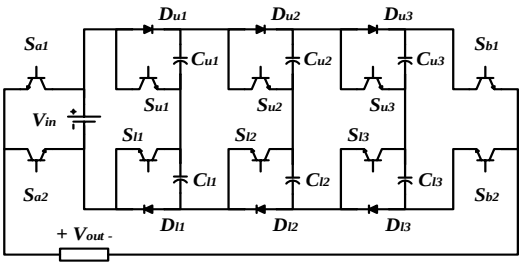
(a)



S_{a_1}	1	0	0	0	1
S_{a_2}	0	1	1	1	0
S_{u_1}	0	1	1	0	0
S_{l_1}	1	0	0	0	1
S_{u_2}	0	1	1	0	0
S_{l_2}	1	0	0	0	1
S_{u_3}	0	1	1	0	0
S_{l_3}	1	0	0	0	1
S_{b_1}	1	0	1	0	0
S_{b_2}	0	1	0	1	1

(b)

Figure 3. (a) proposed pulsed power system with n modules (b) output voltage pulse of a three-module system in a switching cycle and their switching states



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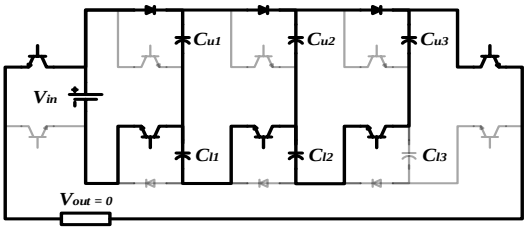

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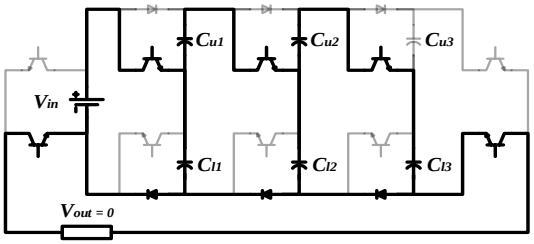
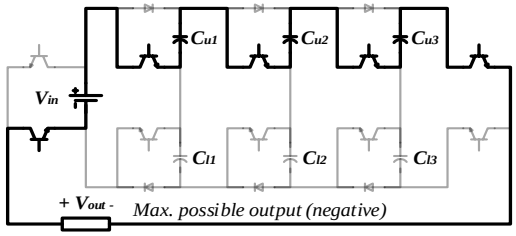
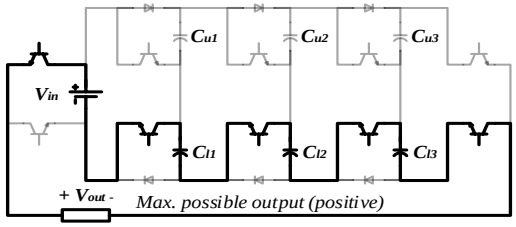


(c)

Figure 4. (a) a three-stage pulse generator and charging paths of (b) upper and (c) lower capacitors



(a)



(b)

Figure 5. Discharging paths of the capacitors to achieve (a) negative (b) positive output pulse

After capacitors are charged, they should be discharged according to the load properties. According to Figure 5.a (5.b), from the sum of upper (lower) capacitors' voltages, negative (positive) pulse is created with a magnitude of -8Vin (+8Vin).

3. DISCUSSION

3. 1. Multiplication Limit Increasing the voltage ratings of power electronic elements is the main disadvantage of the proposed multiplier topology. Once the capacitors' voltage has reached the specified limitation of the elements, voltage doubling should stop and the constant charging mode should be used. Henceforth, the circuit modules of Figure 3 need to be changed into Figure 6.a. In this module, diodes D_{ui} and D_{li} are replaced with switches. As shown in Figure 6.b, each of the two capacitors in $(k+1)^{th}$ module are simultaneously charged by two capacitors of K^{th} module.

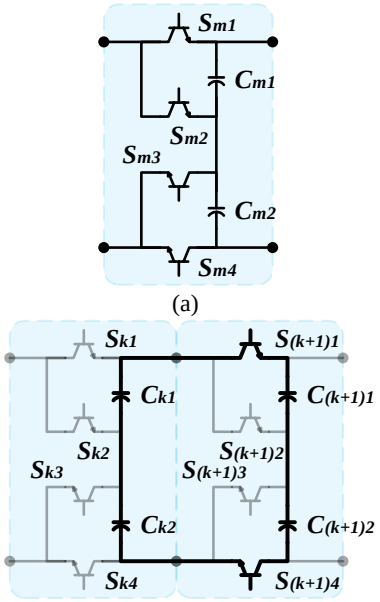


Figure 6. (a) proposed module for constant charging mode and (b) its capacitors' charging path

For the applications with low input voltage sources (such as a battery, fuel cells and etc.), multiplication is allowed until peak inverse voltage (PIV) reaches $x\%$ of V_{rated}^{SW}. It should be considered that x is the ratio between acceptable switch's voltage and its rated value (V_{rated}^{SW}). This implies that the charging mode (doubling or constant) must be chosen in a way that PIV of the circuit component is kept below a certain percentage of the switches nominal voltage.

3. 2. Determinations of the Capacitances and Output Voltage

3. 2. 1. Calculation of Capacitances As previously mentioned (see Figure 2), the capacitors of $(k+1)^{th}$ module are charged by the ones at k^{th} module. To achieve the desired output voltage, the voltage of each capacitors is assumed to be (1-p) percent of its initial voltage (p is the capacitors' voltage drop percentage due to parallel charging of the capacitors). Note that capacitors calculation is performed for (1,2,4, …, 2^{n-1}) × V_{in} charging mode for the worst-case scenario. From the charge conservation law, one can have:

$$q_{total}(t_0^-) = q_{total}(t_0^+) \quad (1)$$

The net charge of the system before connection of the capacitors of k^{th} and $(k+1)^{th}$ modules is :

$$q_{total}(t_0^-) = (\frac{C_{k1}}{2})2V_{C-k1}(t_0^-) + C_{(k+1)eq}V_{C-(k+1)eq}(t_0^-) = C_{k1}V_{C-k1}(t_0^-) \quad (2)$$

After charging of next module by previous one, the net charge of the system becomes:

$$q_{total}(t_0^+) = (\frac{C_{k1}}{2})2V_{C-k1}(t_0^+) + C_{(k+1)eq}V_{C-(k+1)eq}(t_0^+) \quad (3)$$

Considering the capacitor voltage at $(k+1)^{th}$ module as $V_{C-k1}(t_0^+) = (1-p)V_{C-k1}(t_0^-)$ and equalizing Equations (2) and (3), the following equation can be achieved.

$$C_{(k+1)eq} = \frac{p}{2(1-p)}C_{k1} \Rightarrow C_{(k+1)1} = \frac{p}{(1-p)}C_{k1} \quad (4)$$

Eventually, the equivalent capacitance (C_{eq}) of the circuit resulted from the serial connection of all the capacitors (as shown in Figure 5.a) is calculated by the following equation:

$$\frac{1}{C_{eq}} = \frac{1}{C_{u1}} + \frac{1}{C_{u2}} + ... + \frac{1}{C_{uk}} = \frac{1}{C_{u1}}\sum_{k=1}^{n}\left(\frac{(1-p)}{p}\right)^{k-1} \quad (5)$$

In accordance with load properties, during discharging process (time intervals of $[t_2\text{-}t_3]$ and $[t_4\text{-}t_5]$ in Figure 3.b), an α percent voltage drop is occurred for equivalent voltage of series capacitors.

$$C_{eq} = \frac{\Delta q}{\Delta V} = \frac{\Delta q}{\alpha \times V_{eq}} \quad (6)$$

Considering equal discharging intervals for positive and negative pulses ($T_0=t_2\text{-}t_3=t_4\text{-}t_5$), the charge variation of the C_{eq} during the discharging process can be calculated as:

$$\Delta q = \int_0^{T_0} i_{load}.dt = \int_0^{T_0} \frac{V_{eq}}{R_{load}}.e^{\frac{-t}{R_{load}C_{eq}}}.dt = C_{eq}.V_{eq} \times (1 - e^{\frac{-T_0}{R_{load}C_{eq}}}) \quad (7)$$

Finally:

$$C_{eq} = \frac{-T_0}{R_{load}.\ln(1-\alpha)} \quad (8)$$

Hence, every capacitance in the structure can be calculated using Equations (4)-(8), in a way that demonstrated as follows:

$$C_k = \frac{-T_0\left(\frac{p}{(1-p)}\right)^{k-1} \times \sum_{k=1}^{n}\left(\frac{(1-p)}{p}\right)^{k-1}}{R_{load}.\ln(1-\alpha)}, \; k = 1,2,\ldots,n \quad (9)$$

3. 2. 2. Maximum Output Voltage Calculation Figure 7 shows the charging paths of the lower capacitors in different modules considering non-idealities for all circuit components (Figure 4.c with real components). The same process is carried out for the upper capacitors. Considered non-ideal elements are :

V_{on}^{SW} : Forward voltage of the switch

R_{on}^{SW} : ON-state resistance of the switch

V_{on}^{D}: Forward voltage of the Diode

R_{on}^{D}: ON-state resistance of the Diode

ESR: Equivalent series resistance of capacitor

The voltage drop of each module can be defined as follows:

$$x = (V_{on}^{SW} + R_{on}^{SW} I) + (V_{on}^{D} + R_{on}^{D} I) - ESR \times I \tag{10}$$

Considering (1, 2, 4, …, 2n-1)×Vin charging mode, capacitors' voltages of modules can be written as:

$$\begin{aligned} V_1 &= 2(V_{in} - x)(1-p) \\ V_2 &= 2\left[2(V_{in} - x)(1-p) - x\right](1-p) \\ &\vdots \\ V_k &= 2^k (V_{in} - x)(1-p)^k - x\left(\sum_{k=1}^{n-1} 2^k (1-p)^k\right) \end{aligned} \tag{11}$$

Maximum output voltage, in this case, can be achieved by calculating the summation of the voltage of the capacitor in all modules as:

$$V_{out-\max}^{Non\ Ideal} = \sum_{k=1}^{n}\left(2^k (V_{in} - x)(1-p)^k - x\left(\sum_{m=1}^{k-1} 2^m (1-p)^m\right)\right) \tag{12}$$

3. 2. 3. Calculation of Maximum Start-up Current

High overshoot current is one of the drawbacks of switched capacitor structures such as Marx and other CSVM topologies. In this section, the worst-case scenario is calculated for start-up current and then a switching strategy is presented to reduce the magnitude of this current. Note that the analysis is for a 3-module structure of voltage doubler type.

The maximum amount of the input current occurs when the capacitors are totally discharged and their initial charging leads to increasing its current. It is clear that the amount of input current is low during steady state (if the capacitor is not fully discharged). According to Figure 7, input current is calculated as follows:

$$I_{in} = I_{Cl1} + I_{Cl2} + I_{Cl3} \tag{13}$$

Each capacitor's current can be calculated by solving the following equation.

$$\begin{bmatrix} R_0 + R_1 + \frac{1}{sC_{l1}} & R_0 & R_0 \\ -R_1 - \frac{1}{sC_{l1}} & \frac{1}{sC_{u1}} + \frac{1}{sC_{l2}} + R_2 + R_3 & \frac{1}{sC_{u1}} + R_2 \\ 0 & -\frac{1}{sC_{l2}} - R_3 & \frac{1}{sC_{u2}} + \frac{1}{sC_{l3}} + R_4 \end{bmatrix} \begin{bmatrix} I_{Cl1}(s) \\ I_{Cl2}(s) \\ I_{Cl3}(s) \end{bmatrix} \tag{14}$$

$$= \begin{bmatrix} \frac{V_{in} - V_{on}^{SW} - V_{on}^{D} - V_{Cl1}(0)}{s} \\ \frac{V_{Cl1}(0) + V_{Cu1}(0) - V_{Cl2}(0) - V_{on}^{SW} - V_{on}^{D}}{s} \\ \frac{V_{Cl2}(0) + V_{Cu2}(0) - V_{Cl3}(0) - V_{on}^{SW} - V_{on}^{D}}{s} \end{bmatrix} \tag{14}$$

In which:

$$\begin{aligned} R_0 &= R_{on}^{SW} + R_{on}^{D} \\ R_1 &= ESR_{Cl1} \\ R_2 &= R_{on}^{SW} + R_{on}^{D} + ESR_{Cu1} \\ R_3 &= ESR_{Cl2} \\ R_4 &= R_{on}^{SW} + R_{on}^{D} + ESR_{Cu2} + ESR_{Cl3} \end{aligned} \tag{15}$$

With the parameters specified in Table 2 and extracting the values of Equation (15) from semiconductors datasheet, input current can be calculated from the solution of Equation (14).

$$I_{in} = 540.e^{-4602t} + 33.e^{-25418t} + 3.e^{-15511t} \tag{16}$$

Above mentioned calculation is for the simultaneous parallel charging of the capacitors (as shown in Figure 7). It seems that a little delay in capacitors' charging (maximum for a time constant at each stage) causes reducing the maximum value of input current. After connecting switch Su1, only capacitor Cl1 is charged from the source (0<t< T1). Then, switch Su2 would be connected (T1<t<T2). At this time, in addition to voltage increase of capacitor Cl1, Cl2's charging begins. Finally, switch Su3 is connected (T2<t). As a result, the input current relation in each stage would be as follows:

$$I_{in} = \begin{cases} I_{Cl1} = 446.e^{-4762t} & 0 < t < T_1 \\ I_{Cl1} + I_{Cl2} = (282.\cosh(9953t) + 167.\sinh(9953t)).e^{-14572t} & T_1 < t < T_2 \\ I_{Cl1} + I_{Cl2} + I_{Cl3} = 114.e^{-4602t} - 16.27.e^{-25418t} + 18.339.e^{-15511t} & T_2 < t \end{cases} \tag{17}$$

Figure 8 shows the input current of a 3-module system with simultaneous (mode1, Equation (16)) and non-simultaneous charging of the capacitors (mode 2, Equation (17)). It can be seen from this figure that second charging strategy leads to almost 25% reduction of input current. It is worth noting that with both charging modes, the amount of input current is too high. Therefore, following issues has to be considered to avoid high start-up (or any transient state) current.

1) During start-up with fully discharged capacitor, it is necessary to increase the input voltage source gradually to avoid high current spike (it requires variable DC source). Otherwise, limiting resistors (or inductors) during start-up are required to limit the input current. Another option can be initializing the circuit with switching of the switches in linear mode which make the switch as resistor. During start-up or transient, the amount of current reduces to a great extent and after reaching steady state, it returns back to switch mode.

2) During normal operation of the converter, it is necessary to keep the capacitors voltage at a certain voltage level in order to avoid fully discharging the capacitors. This case is considered in Equations (6)-(9) for capacitors calculation and their charging intervals knowing the load amount and also duration of discharging intervals.

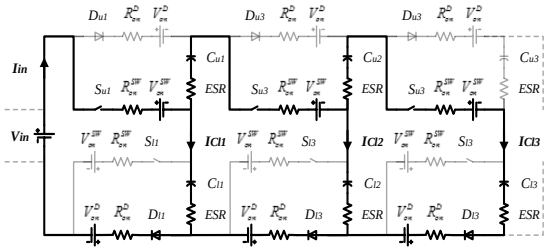


Figure 7. Charging Paths for lower capacitors

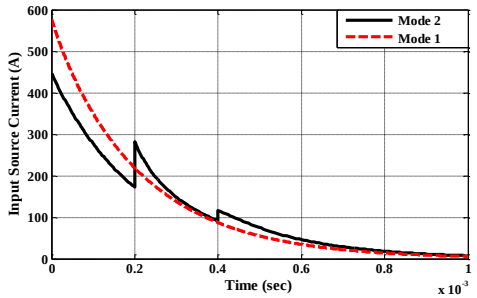


Figure 8. Start-up current for the case with fully discharged capacitors with simultaneous charging of all capacitors (mode 1) and non-simultaneous charging of the capacitors (mode 2)

3. 3. Comparison Study By examining the pros and cons of the basic structures, it is evident that the best structure is the one which has better evaluation indicators than the others. These indicators are divided into two groups of power circuit and control circuit. The number of power semiconductor devices, the number of capacitors, and the Total Standing Voltage (TSV) are among the most important indicators of power circuit assessment. Because the driver circuits have a significant effect on the volume, weight, complexity, and cost of the final circuit, the number of the driver circuits is considered as one of the most important indicators among the control parameters. Table 1 shows different comparison parameters based on input and output voltages ratios in topologies. Two types of modules, doubling and constant, are proposed to take advantage of the both Marx-based and multiplier circuits at the same time.

All of the comparison indices (except for the number of capacitors) in the constant charging mode are better (or at least similar) than other topologies. The number of capacitors is twice as many as in the other topologies, which is the main drawback of this topology in this mode. However, the number of series diodes is zero which improves the problem. According to Table 1, the proposed doubling topology has better performance for all comparison indices except for the PIV. It means that this topology is appropriate for low-input sources, which were the main focus of this paper. Also these two types of modules have the capability to be combined with each other.

4. SIMULATION AND EXPERIMENTAL RESULTS

In this section, to prove the accurate performance of the designed converter, simulation and experiments are carried out. To examine the performance of the proposed topology, a simulation has been done for a prototype consisting of 5 modules with the charging mode of (1, 2, 4, 4, 4)×V_{in}. Notice that the first three modules are of the doubling kind and the other two are of the constant voltage kind. Considering this charging mode and by a 100 V input source, a maximum output voltage of 1.6 kV is attained, at the frequency of 200 Hz. In the simulation, the MATLAB software has been used. Figure 9 shows the simulated output pulse, a few selected capacitors voltage of the circuitand current respectively.

As shown in Figure 10, the laboratory experimental setup has been implemented using both proposed modules combined together and parameters of the Table 2. The IGBTs utilized in the prototype are 15n120 (1200 V) without any series or antiparallel diodes. The switching scheme has been generated by utilizing a AVR ATmega16A. Figure 11 shows the experimental output voltage of the circuit and capacitors voltages of the first three modules. Note that capacitor voltage ripples follow the aforementioned theoretical basis in part B of the section 3.

TABLE 1. Comparison between the Proposed Converter and Other Marx Topologies (N=$\frac{V-out}{V-in}$)

Items	Proposed (doubling mode)	Proposed (constant mode)	[17]	[16]	[15]
IGBT	$2+2log_2 2N$	4N	5N	4N	5N
Diodes	$-2+2log_2 2N$	0	7N	6N	4N
Driver	$2+2log_2 2N$	4N	5N	4N	5N
Capacitors	$-2+2log_2 2N$	2N	N	N	N
TSV (*Vin)	6N-2	8N	12N	10N	9N

TABLE 2. Simulation and experimental parameters

Items	Values
Input voltage	100 V
Output voltage	1.6 kV
C_{11}, C_{12}	1000 µF (150 V)
C_{21}, C_{22}	100 µF (250 V)
C_{31}, C_{32}	10 µF (450 V)
Load	10 KΩ
IGBT	15n120 (1200 V)
Diode	RHRP15120 (1200 V)

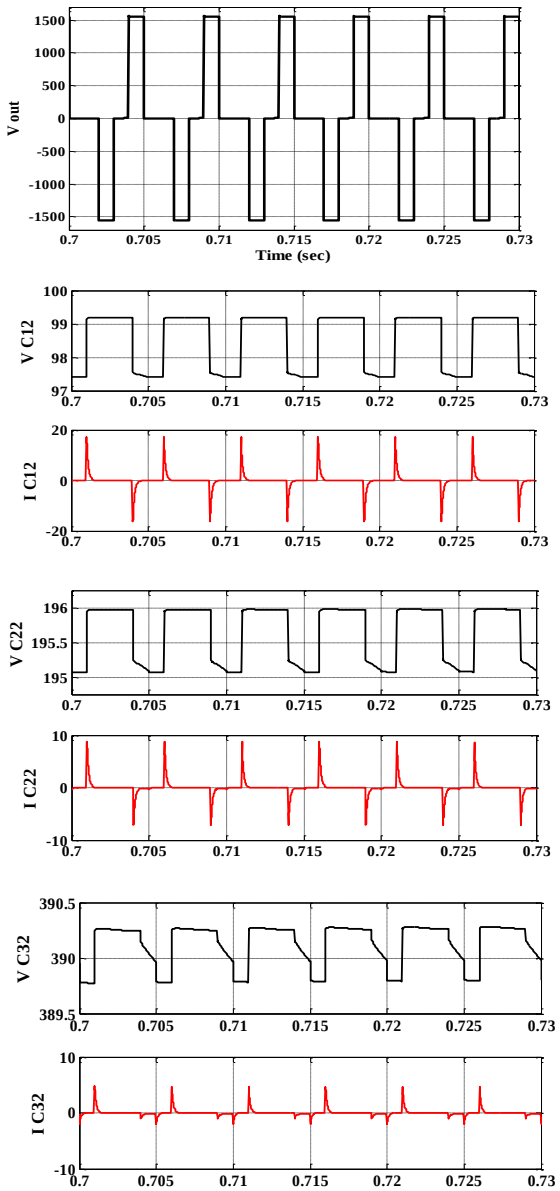


Figure 9. Simulation results: Output voltage, capacitors voltage and currents for different modules

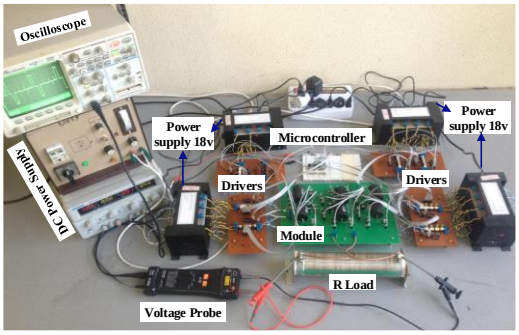


Figure 10. A laboratory test setup

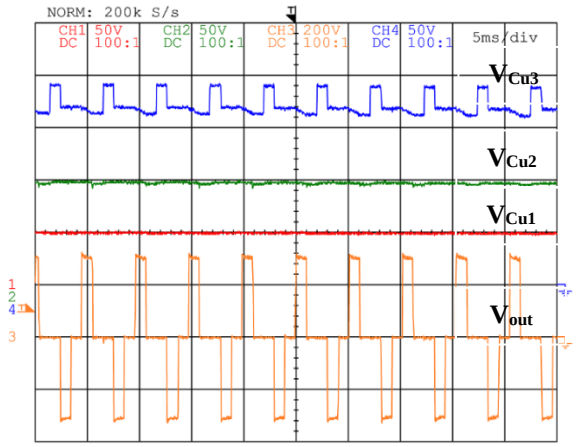


Figure 11. Experimental waveforms for output voltage, upper capacitors voltage at modules 1,2 and 3 (V_{cu1}, V_{cu2}, V_{cu3}) (Differential Probes are set at × 500 for CH_3 and × 200 for CH_1, CH_2 and CH_4. The internal probe of the oscilloscope is set at × 100.)

5. CONCLUSION

This paper proposed a modular SC structure for generating a bipolar high voltage pulsed power. Due to its boosting capability, the presented structure can be an appropriate replacement of Marx structures in applications with low input voltage sources. Two different modules are investigated for the proposed topology with voltage doubling and constant voltage capabilities. The doubling charging mode is used whenever the low input voltage is needed to be boosted with high gain till the rated value of the switches permits. Afterwards, a constant charging mode is applied. The theoretical foundation of the topology and the practical results of the simulation prove that the proposed topology has the capability to produce bipolar combined wide and narrow pulses.

6. ACKNOWLEDGEMENTS

The authors acknowledged the funding support of Babol Noshirvani University of Technology through grant program No. BNUT/ 389051 /97.

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A High Gain Bipolar Pulse Generator with Low Voltage Input Source

H. Gholamalitabar[a], J. Adabi[a], M. Rezanejad[b]

[a] *Department of Electrical and Computer Engineering, Babol Noshirvani University of Technology, Babol, Iran*
[b] *Department of Electrical and Computer Engineering, University of Mazandaran, Babolsar, Iran*

PAPER INFO

Paper history:
Received 30 May 2019
Received in revised form 21 July 2019
Accepted 28 July 2019

Keywords:
Bipolar Pulsed Power Generator
Switched-Capacitor
Modular
Marx Generator

چکیده

در این مقاله، دو نوع ماژول سوییچ خازنی افزاینده جهت تولید منابع توان پالسی معرفی شده است. در ماژول پیشنهادی نوع اول، ولتاژ خروجی نسبت به ولتاژ ورودی دو برابر است و در ماژول نوع دوم، ولتاژ ورودی و ولتاژ خروجی با هم برابرند و در نهایت، با کنار هم قرار دادن این ماژول‌ها، ولتاژ نهایی مورد نظر حاصل می‌گردد. علاوه بر این که ساختار ماژولار پیشنهادی از سوییچ سربار استفاده نمی‌کند، استرس جریانی کمتر بر روی منبع و عناصر نیمه هادی نزدیک به آن به عنوان مزیت این ساختار محسوب می‌شود. همچنین، تعداد عناصر مداری نیز به طور چشم‌گیری در مقایسه با ساختار مارکس کاهش یافته که منجر به کاهش هزینه تمام شده و پیچیدگی مدار کنترل شده است. در ادامه، محاسبات خازن بیان شده و تست آزمایشگاهی و شبیه‌سازی به منظور تایید کارآیی ساختار پیشنهادی بر روی یک نمونه پنج ماژوله انجام گردید.

***doi**: 10.5829/ije.2019.32.08b.08*