IJE TRANSACTIONS A: Basics Vol. 32, No. 4, (April 2019) 528-535

International Journal of Engineering

Journal Homepage: www.ije.ir

Voltage Differencing Buffered Amplifier based Voltage Mode Four Quadrant Analog Multiplier and its Applications

P. Gupta*, R. Pandey

Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India

P A P E R I N F O

Paper history:
Received *25 July 2018*
Received in revised form *20 January 2019*
Accepted *07 March 2019*

Keywords:
Analog Building Blocks
Voltage Differencing Buffered Amplifier
Four Quadrant Analog Multiplier
Quarter Square Algebraic Identity

A B S T R A C T

In this paper a voltage mode four quadrant analog multiplier (FQAM) using voltage differencing buffered amplifier (VDBA) based on quarter square algebraic identity is presented. In the proposed FQAM the passive resistor can be implemented using MOSFETs operating in saturation region thereby making it suitable for integration. The effect of non idealities of VDBA has also been analyzed in this paper. Theoretical propositions are verified through SPICE simulations at 0.18µm CMOS technology node and the simulation results are found in close agreement with theoretical values. The supply voltage is taken as ± 1V and the value of the bias current is set to 40µA. The simulated total harmonic distortion (THD) is observed to be under 3% and the total power dissipation is found as 627µW. The workability of the proposed FQAM is also tested through two applications, namely, an amplitude modulator and a rectifier. The simulated results corroborate the theoretical propositions.

doi: *10.5829/ije.2019.32.04a.10*

NOMENCLATURE

V	Volt	**Greek Symbols**	
R	Resistance	ε	Tracking error
n	nano	$\alpha_{p,n}$	$1\text{-}\varepsilon_{gmp,n}$
A	Ampere	$\beta_{p,n}$	$1\text{-}\varepsilon_{p,n}$
µ	Micro	Ω	Ohms

1. INTRODUCTION

The FQAM performs multiplication of two bipolar signals and preserves the polarity relationship. Analog multiplier is used extensively for nonlinear applications such as a modulator, equalizer, frequency doublers, and neural computing [1]. A large number of analog multipliers are available in literature [2-14] using different analog building blocks (ABBs) having there own pros and cons.

On the other hand, researchers are continuously striving to explore different ABBs with attributes like higher bandwidth, higher slew rate, lower power consumption, and better linearity [15]. This journey initiated way back in 1966 with current conveyor [16] and still continues. As a result numerous applications using different ABBs have already being developed [17-23]. The voltage differencing buffered amplifier (VDBA) has emerged as an outcome of this consistent effort relatively recently [17]. Apart from possessing the above mentioned attributes the VDBA also provides electronic tunability through its transconductance. Various applications based on VDBA and their variants are available in the literature [15,18-21]. However, limited literature is available on VDBA based non linear applications. So the aim of this study is to present VDBA-based FQAM using the quarter square technique. All available analog multipliers [2-14] are summarized in Table 1 to identify the gap in the previous research and to justify the proposition of voltage mode VDBA based FQAM. Some of the inferences from Table 1 are:

*Corresponding Author Email: *priyankagupta09@gmail.com* (P. Gupta)

TABLE 1. Comparison of previously reported analog multipliers

Reference No.	ABB	Number of ABBs	Numberof extra transistors	Passive resistors	Four quaqrant	Input range	output range	Supply voltage	Type of Input signal	Type of ouput signal	Power dissipation (mW)	3 dB Frequency
[2]	CCCII+	2	0	0	No	-	-	±5V	Current	Current	-	20 MHz
[3]	OTA	3	0	0	Yes	±.8mA	±.8mA	±10V	Current	Current	-	155 MHz
[4]	Op-Amp	5	0	8	Yes	2.62V	±200mV	±2.4V	Voltage	Voltage	-	840 KHz
[5]	CCCII	1	0	1	No	-	-	±2.5V	Current	Current	3.82	-
		1	0	1	Yes			±2.5V	Current	Current	3.82	
[6]	OTRA	1	6	0	Yes	±200mV	±350mV	±1.5V	Voltage	Voltage	-	25 MHz
[7]	CDBA	1	6	0	Yes	±250mV	±180mV	±5V	Voltage	Voltage	-	82.3 MHz
[8]	CDBA	1	4	0	Yes	±1V	±0.6V	±5V	Voltage	Voltage	-	10 MHz
[9]	CDTA	2	0	0	Yes	-	-	±5V	Current	Current	-	30 MHz
[10]	OTA	4	16	0	Yes	±0.1V	±0.015V	±1V	Voltage	Voltage	0.588	3.96 GHz
[11]	CTTA	1	0	0	Yes	±150uA	±40uA	±1.5V	Current	Current	1.83	53.1MHz
[12]	OTA	3	0	0	Yes	±1mA	±1mA	±10V	Current	Current	-	162 MHz
[13]	VSDVG	3	6	0	Yes	±150mV	±600mv	±1.5V	Voltage	Voltage	0.550	10 MHz
[14]	OTRA	1	4	0	Yes	±300mV	±100mV	±1.5V	Voltage	Voltage	0.830	8 MHz
Proposed	VDBA	2	10	0	Yes	±50mV	±15mV	±1V	Voltage	Voltage	0.627	220 MHz

- The structures discussed in literature [2-9, 12] are not suitable from portability view point due to higher power supply requirements. Structures discussed in literature [2-4, 10, 12 and 13] use a large number of ABBs.
- The bandwidth of all the listed configurations other than reported value [10] is smaller as compared to the proposed configurations.
- Multipliers reported literature [4, 5] use passive components which is not suitable for integrated circuit.
- Voltage output is available at a high impedance in literature [10] making a buffer necessary to drive the voltage input circuits.
- The work presented in literature [2] is a two quadrant, while the multiplier designed in another paper [5] can work as a two or four quadrant multiplier.

Thus the intention of this paper is to propose a VDBA based FQAM which operates at the low power supply consumes less power and provides higher bandwidth.

2. CIRCUIT DESCRIPTION

In this section, the generalized quarter square algebraic identity based FQAM [1] is described first which has been adapted for implementation with VDBA.

2. 1. Generic FQAM based on Quarter Square Algebraic Identity An FQAM can be implemented using well known quarter square algebraic identity given below:

$$(V_{in1}+V_{in2})^2-(V_{in1}-V_{in2})^2=4V_{in1}V_{in2} \tag{1}$$

It may be observed from Equation (1) that FQAM based on quarter square algebraic identity can be designed with the help of adder, subtractor and squarer circuits arranged as depicted in Figure 1

2. 2. Proposed VDBA based FQAM The circuit symbol of VDBA is shown in Figure 2, the terminals *p* and *n* are high impedance input voltage differencing terminals. The *z* represents a high impedance output current terminal and the *w*-(*w*+) is the low impedance buffered inverted (non inverted) output terminal. Due to the high input and low output impedances, this block is well suited for voltage mode operation. The port relationship of the VDBA is described in Eq. (2).

$$\begin{bmatrix} I_z \\ V_{w+} \\ V_{w-} \\ I_p \\ I_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & g_m & -g_m \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_{w+} \\ I_{w-} \\ V_p \\ V_n \end{bmatrix} \tag{2}$$

where g_m represents the transconductance of VDBA and is g_m is expressed as follows:

$$g_m = \sqrt{\frac{\mu n \, Cox \, W}{L} I_b} \tag{3}$$

It may be observed that the value of g_m can be controlled through bias current I_b.

The proposed VDBA based FQAM is shown in Figure 3. The circuit comprising of VDBA I and resistance R_1 represents an adder whereas VDBA II along with resistance R_1 performs the subtraction operation.

The current and voltage outputs of VDBA I are expressed in Equations (4) and (5), respectively: Similarly, for VDBA II Equations (6) and (7) represent the current and voltage outputs.

$$I_{z1} = g_{mv}(V_{in1} + V_{in2}) \tag{4}$$

$$V_{w1+} = -V_{w1-} = g_{mv} R_1 (V_{in1} + V_{in2}) \tag{5}$$

$$I_{z2} = g_{mv}(V_{in1} - V_{in2}) \tag{6}$$

$$V_{w2+} = -V_{w2-} = g_{mv} R_1 (V_{in1} - V_{in2}) \tag{7}$$

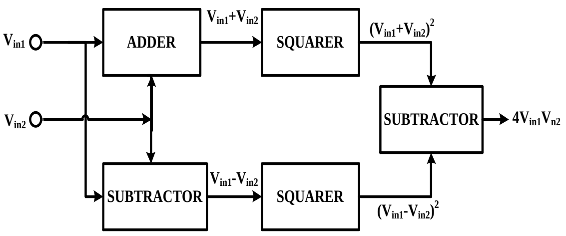


Figure 1. Block diagram of Quarter square algebraic identity [1]

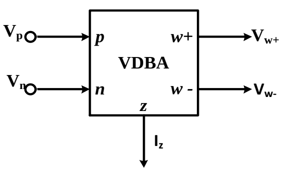


Figure 2. The VDBA Circuit Symbol

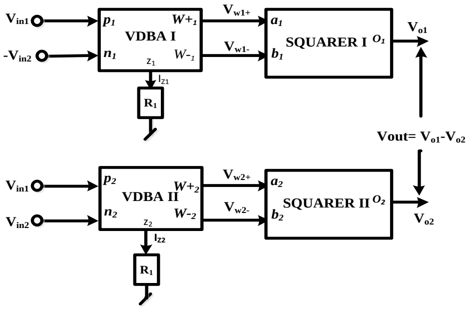


Figure 3. Proposed VDBA based FQAM

where g_{mv} represents the transconductance of VDBA

It may be seen from Equation (5) that V_{w1+} is proportional to the sum of the input voltages whereas V_{w1-} is an inversion of V_{w1+} Equation (7) shows that buffered outputs of VDBA II are proportional to the difference of input voltages with opposite polarities. The squarer block [13] having *a* and *b* as two inputs and *O* as the output terminalis shown in Figure 4. Using routine analysis the output voltage of the squarer circuit (V_{SQ}) may be derived and expressed as Equation (16) provided transistors M_{s1} and M_{s2} are perfectly matched and all the transistors are biased in the saturation region. Further aspect ratio of M_{s3} is considered to be twice as that of M_{s1} and M_{s2}.

For the nmos transistor in saturation region, the drain current is given as follows:

$$I_d = \frac{K}{2}\left[(V_{gs} - V_{TH})^2\right] \tag{8}$$

where K is transconductance parameter.

From Figure 4 Current through MS3 can be written as follows:

$$I_{MS3} = I_{MS1} + I_{MS2} \tag{9}$$

As $K_{MS1}=K_{MS2}=K=0.5K_{MS3}$ (10)

$$\frac{2K}{2}(V_{SQ} - V_{SS} - V_{TH})^2 = \frac{K}{2}[(+V_x - V_{SQ} - V_{TH})^2 + (-V_x - V_{SQ} - V_{TH})^2] \tag{11}$$

$$V_{SQ} = -\frac{V_x^{\,2}}{2(V_{SS} + 2V_{TH})} + \frac{V_{SS}}{2} \tag{12}$$

where V_x is the applied input voltage. V_{SQ} is the output of the squarer circuit. Using Equations (8) and (10) current through respectively can be written as follows:

$$I_{MS3} = K(V_{SQ} - V_{SS} - V_{TH})^2 \tag{13}$$

Now putting the value of V_{SQ} from Equation (12) into Equation (13),

$$I_{MS3} = \frac{K(V_x^4 + 2V_x^2(V_{ss} + 2V_{TH})^2 + (V_{ss} + 2V_{Th}))}{4(V_{ss} + 2V_{TH})^2} \tag{14}$$

For small signals, $V_x^4 \approx 0$

$$I_{MS3} = \frac{K}{2}V_x^{\,2} + \frac{K}{4}(V_{SS} + 2V_{TH})^2 \tag{15}$$

$$V_{SQ} = \frac{I_{MS3}}{g_{ms}} = \frac{K}{2g_{ms}}V_x^2 + \frac{K}{4g_{ms}}(V_{ss} + 2V_{TH})^2 \tag{16}$$

Equation (16) suggests that the output voltage of the squarer circuit (V_{SQ}) is proportional to the square of the input voltage (V_x). The outputs of VDBA I and VDBA II as expressed by Equations (5) and (7) serve as inputs to the squarer blocks of Figure 3. Using Equation (16) the output voltages of the squarer I and squarer II, may be written as Equations (17) and (18), respectively.

$$V_{o1} = \frac{K_s}{2g_{ms}} V_{w1}^2 + \frac{K_s}{4g_{ms}} (V_{ss} + 2V_{TH})^2 \tag{17}$$

$$V_{o2} = \frac{K_s}{2g_{ms}} V_{w2}^2 + \frac{K_s}{4g_{ms}} (V_{ss} + 2V_{TH})^2 \tag{18}$$

Where g_{ms} represents the transconductance of squarer. The output voltage (V_{out}) can be determined as follows:

$$V_{out} = V_{o1} - V_{o2} = \frac{K_s}{2g_{ms}} (V_{w1}^2 - V_{w2}^2) \tag{19}$$

From Equations (5), (7) and (19)

$$V_{out} = \frac{K_s}{2g_{ms}} g_{mv}^2 R_1^2 ((V_{in1} + V_{in2})^2 - (V_{in1} - V_{in2})^2) = CV_{in1}V_{in2} \tag{20}$$

Where , $C = \frac{2K_s}{g_{ms}} g_{mv}^2 R_1^2$ (21)

Thus, it may be concluded from Equation (21), the output voltage is proportional to the multiplication of the two input signals. The passive resistors consume a large chip area as compared to active resistors. Thus from integration view point, it is always preferred to implement a passive resistor using MOSFETs operating in the linear region.

The resistance R_1 in Figure 3 can be realized using MOSFETs as shown in Figure 5 where both the transistors (M_{R1} and M_{R2} with aspect ratio as W_{MR}/L_{MR}) are operating in saturation. The equivalent resistor R may be expressed as follows:

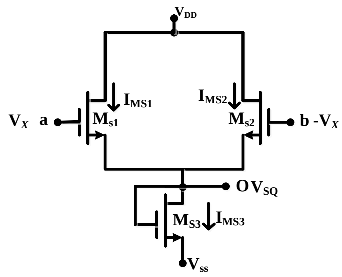


Figure 4. Squarer Circuit [13]

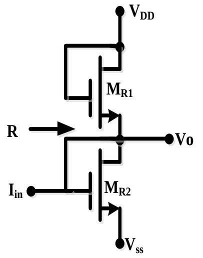


Figure 5. The NMOS based resistor (R) realization

$$R = \frac{V_o}{I_{in}} = \frac{L_{MR}}{2\mu C_{ox} W_{MR}(V_{DD} - V_{TH})} = \frac{1}{2K_R(V_{DD} - V_{TH})} \tag{22}$$

Substituting the value of R_1 from Equation (22) into Equation (20) the V_{out} may be expressed as follows:

$$V_{out} = \frac{2K_s}{g_{ms}} \left(\frac{g_{mv}}{2K_R(V_{DD} - V_{TH})} \right)^2 \left((V_{in1} + V_{in2})^2 - (V_{in1} - V_{in2})^2 \right) = CV_{in1}V_{in2} \tag{23}$$

and the C of Equation (21) modifies to following expression:

$$C = \frac{2K_s}{g_{ms}} \left(\frac{g_{mv}}{2K_R(V_{DD} - V_{TH})} \right)^2 \tag{24}$$

3. NON-IDEAL ANALYSIS

In the analysis so far, the VDBA characteristics are considered to be ideal. However, in CMOS implementation of VDBA transconductance and voltage tracking errors may exist due to device mismatch which may lead to deviation from the ideal behavior. Therefore, the effect of non-idealities of VDBA needs to be considered on the performance of the proposed FQAM configuration. Taking the tracking errors into consideration Equation (2) modifies to following expression:

$$\begin{bmatrix} I_z \\ V_{w+} \\ V_{w-} \\ I_p \\ I_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \alpha_p g_m & -\alpha_n g_m \\ \beta_p & 0 & 0 & 0 & 0 \\ -\beta_n & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_{w+} \\ I_{w-} \\ V_p \\ V_n \end{bmatrix} \tag{25}$$

where $\alpha_p(\alpha_n)$ represents transconductance transfer ratio from p(n) to z terminal and similarly $\beta_p(\beta_n)$ represent voltage transfer ratio from z to w+(w-) terminal. The non-idealities of VDBA have been summarized in Table 2.

Including the non-idealities of VDBA the outputs of VDBA I and VDBA II of Figure 3 represented by Equations (5) - (7) get modified as Equations (26)-(29):

$$V_{w1+\_n} = \frac{\beta_p g_{mv}(\alpha_p V_{in1} + \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} \tag{26}$$

TABLE 2. VDBA Non-Idealities

Parameter	Value from *p* to *z*	Value from *n* to *z*	Value from *z* to *w+*	Value from *z* to *w-*
Voltage transfer ratio	-	-	$\beta_p=(1-\varepsilon_p)$	$\beta_n=(1-\varepsilon_n)$.
Transconductance transfer ratio	$\alpha_p=(1\varepsilon_{gmp})$	$\alpha_n=(1-\varepsilon_{gm})$	-	-
Tracking error	ε_{gmp} ($\lvert\varepsilon_{gmp}\rvert<<1$)	ε_{gmn} ($\lvert\varepsilon_{gmn}\rvert<<1$)	ε_p ($\lvert\varepsilon_p\rvert<<1$)	ε_n ($\lvert\varepsilon_n\rvert<<1$)

$$V_{w1-\_n} = -\frac{\beta_n g_{mv}(\alpha_p V_{in1} + \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} \tag{27}$$

$$V_{w2+\_n} = \frac{\beta_p g_{mv}(\alpha_p V_{in1} - \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} \tag{28}$$

$$V_{w2-\_n} = -\frac{\beta_n g_{mv}(\alpha_p V_{in1} - \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} \tag{29}$$

Considering $\beta_n = \beta_p = \beta$,

$$V_{w1+\_n} = \frac{\beta g_{mv}(\alpha_p V_{in1} + \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} = -V_{w1-\_n} \tag{30}$$

$$V_{w2+\_n} = \frac{\beta g_{mv}(\alpha_p V_{in1} - \alpha_n V_{in2})}{2K_R(V_{DD} - V_{TH})} = -V_{w2-\_n} \tag{31}$$

Using Equations (16), (30) and (31), the output voltage of the FQAM can be written as follows:

$$V_{out\_n} = \left(\frac{K_s}{2g_{ms}}\left(\frac{\beta g_{mv}}{2K_R(V_{DD} - V_{TH})}\right)\right)^2 \left((\alpha_p V_{in1} + \alpha_n V_{in2})^2 - (\alpha_p V_{in1} - \alpha_n V_{in2})^2\right) \tag{32}$$

$$V_{out\_n} = \frac{K_s}{2g_{ms}}\left(\frac{\beta g_{mv}}{2K_R(V_{DD} - V_{TH})}\right)^2 \left(4\alpha_p \alpha_n V_{in1} V_{in2}\right) \tag{33}$$

For $\alpha_p = \alpha_n = \alpha$, the resultant output voltage may be expressed as follows:

$$V_{out\_n} = (\alpha\beta)^2 C V_{in1} V_{in2} \tag{34}$$

However, the deviation caused in the output due to tracking errors may be ignored as the values of ε_{gmp}, ε_{gmn}, ε_n and ε_p are much smaller than unity.

4. SIMULATION RESULTS

The working of the proposed FQAM circuit is confirmed through SPICE simulations. The CMOS implementation of the VDBA [21] shown in Figure 6 is used and 0.18µm technology node is used for simulations.

The supply voltage used is ±1V. The value of the bias current is set to 40µA. The aspect ratios for the transistors used in VDBA, squarer circuit, and R_1 implementation are given in Table 3.

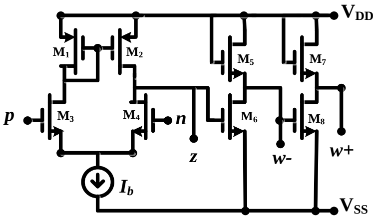


Figure 6. CMOS Implementation of VDBA [21]

TABLE 3. Aspect Ratio of the transistors

Transistor	M_1-M_4	M_5 - M_8	M_{S1}-M_{S2}	M_{S3}	M_{R1}-M_{R3}
(W/L)µm	0.36/0.18	21.6/0.72	5.4/0.27	10.8/0.27	0.27/0.27

The values of α_p and α_n are found 0.934 and 0.933, respectively. Similarly, β_p and β_n were obtained as 0.95 and 0.97, respectively.

4. 1. The DC Characteristics

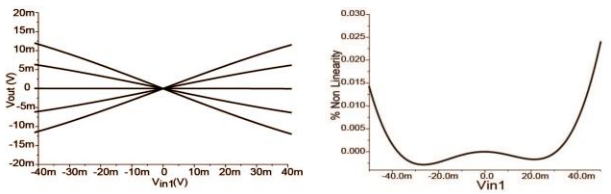
The DC transfer characteristics for the proposed FQAM is depicted in Figure 7(a) with the variation of V_{in2} from -40 mV to 40 mV. It is observed from Figure 7(a) that the proposed circuit is an FQAM. The output voltage varies linearly with V_{in1} as observed from Figure 7(a). The nonlinearity curve for the proposed FQAM is shown in Figure 7(b) which depicts that over the entire input range maximum nonlinearity is less than 0.03%. The simulated power consumption is found to be 627µW when V_{in1} and V_{in2} are kept grounded.

4. 2. AC Characteristics

The simulated frequency response for output voltage is presented in Figure 8. A DC voltage source is applied to V_{in2} while V_{in1} is taken as AC source of 100 mV. The 3dB bandwidth of the proposed FQAM circuit is found to be 220 MHz.

4. 3. Total Harmonic Distortion

The Total Harmonic Distortion (THD) is a measure to estimate the degree to which a system is nonlinear. Therefore the variation in THD as a function of input signal amplitude is observed. For this, a constant DC voltage of 50 mV is applied to V_{in2} while a sinusoidal signal of 100 kHz is applied to V_{in1} with amplitude varying. The measured THD is plotted in Figure 9.



(a) (b)

Figure 7. (a) DC characteristics of proposed multiplier (b) % Nonlinearity curve

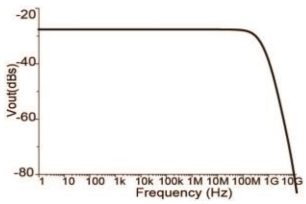


Figure 8. AC characteristics

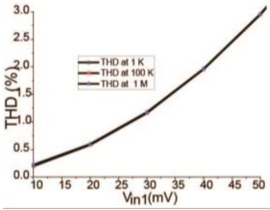


Figure 9. THD vs V_{in1} of proposed multiplier

The similar measurements are obtained for two other input signals having frequencies 1 kHz and 1 MHz, respectively and found that for input signals < 50 mV the maximum THD remains under 3% for the proposed FQAM for all three cases.

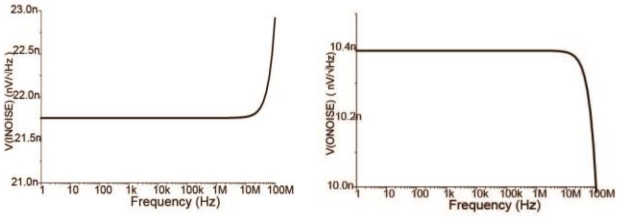
4. 4 Noise Analysis The noise limits the minimum signal level that a circuit can process with acceptable quality. Therefore, the effect of noise on the proposed circuit is examined through SPICE simulations. The equivalent input noise and the equivalent output noise are plotted in Figures 10(a) and 10(b), respectively with varying input frequency. For simulations, V_{in1} is taken as a 100 mV AC signal whereas V_{in2} is chosen as 80 mV DC value. The obseved Vinoise and Vonise are 21.75 nV/√Hz and 10.38 nV/√Hz, respectively.

5. APPLICATIONS

5. 1. Amplitude Modulator An amplitude modulator can be designed provided the carrier and modulating signals are applied to the two inputs of an FQAM, respectively. To validate the functionality of proposed FQAM as an amplitude modulator, two sinusoids of 100 mV/100 kHz and 100 mV/10 kHz frequencies were applied at $V_{in1}$and V_{in2}, respectively. The input transient and corresponding spctrum are shown in Figures 11(a) and 11(b), respectively. Similarly, Figure 12(a) depicts the amplitude modulated output with its spectrum in Figure 12(b). The output frequency spectrum has two frequency components of 90 kHz and 110 kHz thereby confirming the modulation operation.

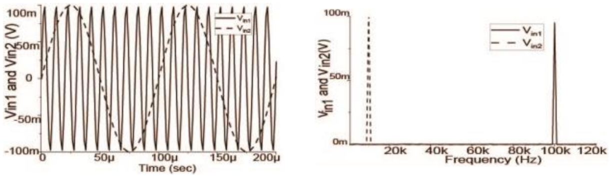
5. 2. Rectifier The rectifier can be implemented using multiplier by taking one of the inputs as pulse type having frequency same as that of the signal which is to be rectified. To verify the workability of rectifier two inputs namely a sinusoidal signal and a square wave of 100 kHz/100 mV each were applied to the respective inputs of FQAM.

The input transient is shown in Figure 13(a) and the rectified output is presented in Figure 13(b). The simulated ripple factor curve is plotted in Figure 13 (c).



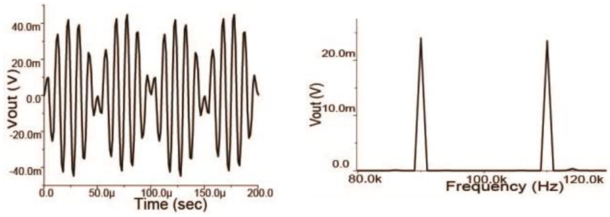
(a) (b)

Figure 10. (a) Input Noise (b) Output Noise



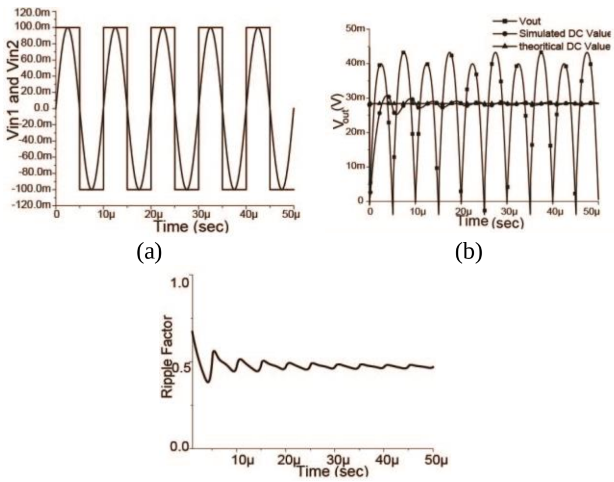
(a) (b)

Figure 11. (a) Input transient (b) Frequency spectrum



(a) (b)

Figure 12. (a) output transient (b) Frequency spectrum



(a) (b)

(c)

Figure 13. Time domain representation of (a) input signals (b) output signal (c) ripple factor

The maximum value of the ripple factor is observed to be less than 0.5.The DC value is found to be 28.54 mV which is in close agreement of the calculated value of 28.42 mV.

6. CONCLUSION

A voltage mode FQAM based on quarter square - algebric identity employing VDBA is proposed in this paper. The circuit is suitable for integration as passive resistor may suitably be implemented using MOSFETs. The theoretical propositions have been verified through SPICE simulations using 0.18μm CMOS process parameters. The power dissipation is found low as compared to other available structures and the simulated THD is well below 3%. Applications like amplitude modulator and rectifier are predesigned using proposed structure to show its applicability and results are in total agreement with the theory.

7. REFERENCES

1. Hsiao, S.Y., and Wu, C.Y., "A 1.2 V CMOS four-quadrant analog multiplier",Proceedings of 1997 IEEE International Symposium on Circuits and Systems, (1997), 241–244.
2. Abuelma'atti Muhammad, M.T., "A current-mode current-controlled current-conveyor-based analogue multiplier/divider",***International Journal of Electronics***, Vol. 85, No. 1, (1998), 71–77.
3. Kaewdang, K., Fongsamut, C. and Surakampontorn, W., "A wide-band current-mode OTA-based analog multiplier-divider",Proceedings of the 2003 IEEE International Symposium on Circuits and Systems, (2003).
4. Riewruja, V. and Rerkratn, A., "Four-quadrant analogue multiplier using operational amplifier", ***International Journal of Electronics***, Vol. 98, No. 4, (2011), 459–474.
5. Yuce, E., "Design of a Simple Current-Mode Multiplier Topology Using a Single CCCII+", ***IEEE Transactions on Instrumentation and Measurement***, Vol. 57, No. 3, (2008),631–637.
6. Chadha, U. and Arora, T., "Four quadrant analog multiplier/divider employing single OTRA", Proceedings of the International Conference on Communication and Computing Systems,(2016),635–639.
7. Pathak, J.K., Singh, A.K. and Senani, R. "New Multiplier/Divider Using a Single CDBA",***American Journal of Electrical and Electronic Engineering***, Vol. 2, No. 3,(2014), 98–102.
8. Keskin, A. Ü.,"A Four Quadrant Analog Multiplier Employing Single CDBA",***Analog Integrated Circuits and Signal Processing***,Vol.40, No. 1,(2004), 99–101.
9. Tangsrirat, W., Pukkalanun, T., Mongkolwai, P., and Surakampontorn, W.,"Simple current-mode analog multiplier, divider, square-rooter and squarer based on CDTAs",***AEU - International Journal of Electronics and Communications***, Vol. 65, No. 3,(2011), 198–203.
10. Hidayat, R., Dejhan, K., Moungnoul, P. and Miyanaga, Y.,"OTA-based high frequency CMOS multiplier and squaring circuit:, IEEE2008 International Symposium on Intelligent Signal Processing and Communications Systems,(2009),1-4.
11. Surakampontorn, W.,Kaewdang, K. and Fongsamut, C..,"A Simple Current-Mode Analog Multiplier- Divider Circuit Using OTAs", 2002 International Technical Conference on Circuits, Computers and Communications, Thailand,(2002), pp. 658–61.
12. Pisutthipong, N. and Siripruchyanun, M.,"A novel simple current-mode multiplier/divider employing only single multiple-output current controlled CTTA". TENCON 2009 IEEE Region 10 Conference, (2009), 1–4.
13. Boonchu, B. and Surakampontorn, W.,"Power Detector Voltage-Mode CMOS Squarer/Multiplier Circuit,"International Technical Conference on Circuits,(2002),8–11.
14. Pandey, R., Pandey, N., Sriram, B. and Paul, S. K., "Single OTRA Based Analog Multiplier and Its Applications",***ISRN Electronics***, Vol. 2012,(2012),1–7.
15. Kaçar, F., Yeşil, A. and Noori, A., "New CMOS realization of voltage differencing buffered amplifier and its biquad filter applications",***Radioengineering***, Vol.21, No. 1,(2012), 333–339.
16. Toumazou, C., Lidgey, F. J. and Haigh, D.,"Analogue IC design: the current-mode approach", IET, (1993), 1st Ed. London.
17. Biolek, D., Senani, R. and Biolková, V., "Active Elements for Analog Signal Processing: Classification , Review , and New Proposals", ***Radioengineering***, Vol. 17, No. 4, (2008), 15-32
18. Herencsar, N., Cicekoglu, O., Sotner, R., Koton, J. and Vrba, K., "New resistorless tunable voltage-mode universal filter using single VDIBA", ***Analog Integrated Circuits and Signal Processing***, Vol.76, No. 2,(2013), 251–260.
19. Guney, A., Alaybeyoglu, E. and Kuntman, H.,"New CMOS realization of Z Copy Voltage Differencing Buffered Amplifier and its current-mode filter application", IEEE 8th International Conference on Design & Technology of Integrated Systems in Nanoscale Era, (2013), 68–71.
20. Khatib, N. and Biolek, D.,"New voltage mode universal filter based on promising structure of Voltage Differencing Buffered Amplifier", IEEE 23rd International Conference Radioelektronika, (2013),177–181. 25.
21. Sotner, R., Jerabek, J. and Herencsar, N.,"Voltage Differencing Buffered/Inverted Amplifiers and Their Applications for Signal Generation", ***Radioengineering***,Vol. 22, No. 2, (2013), 490–504.
22. Farshidi, E. and Keramatzadeh, A.,"A New Approach for low voltage CMOS based on current-controlled conveyors", ***International Journal of Engineering, Transactions B: Applications***, Vol. 27, No. 5, (2014),723-730.
23. Singh, S. V., Tomar, R. S. and Chauhan D. S., "A New Trans-Admittance-Mode Biquad Filter Suitable for Low Voltage Operation", ***International Journal of Engineering, Transactions B: Applications***, Vol. 28, No. 12, (2015), 1738-1745.

Voltage Differencing Buffered Amplifier based Voltage Mode Four Quadrant Analog Multiplier and its Applications

P. Gupta, R. Pandey

Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India

P A P E R I N F O

Paper history:
Received *25 July 2018*
Received in revised form *20 January 2019*
Accepted 07 March 2019

Keywords:
Analog Building Blocks
Voltage Differencing Buffered Amplifier
Four Quadrant Analog Multiplier
Quarter Square Algebraic Identity

چکیده

در این مقاله یک حالت ولتاژ چهار ضریب آنالوگ چهارگانه (FQAM) با استفاده از تقویت کننده بافر ولتاژ (VDBA) بر اساس هویت جبری مربع ارائه شده است. در FQAM پیشنهادی، مقاومت منفعل را می توان با استفاده از MOSFET های عامل در منطقه اشباع اجرا کرد و بنابراین آن را برای ادغام مناسب می کند. در این مقاله اثر غیر آرایشی VDBA نیز مورد تحلیل قرار گرفته است. گزاره های نظری از طریق شبیه سازی SPICE در گره فن آوری CMOS 0.18µm تایید شده و نتایج شبیه سازی در توافق نزدیک با مقادیر نظری یافت می شود. ولتاژ منبع تغذیه به عنوان ± V۱ محاسبه می شود و مقدار جریان تعادلی به µA۴۰ تنظیم می شود. اعوجاج هارمونیک کل تداخل (THD) کمتر از ۳٪ مشاهده می شود و کل قدرت تخلیه به µW۶۲۷ می رسد. کارایی پیشنهاد FQAM نیز از طریق دو برنامه کاربردی، یعنی یک مدولاتور دامنه و یک یکسو کننده، مورد آزمایش قرار می گیرد. نتایج شبیه سازی گزاره های نظری را تأیید می کند.

***doi**: 10.5829/ije.2019.32.04a.10*