



Process Optimization of Deposition Conditions for Low Temperature Thin Film Insulators used in Thin Film Transistors Displays

S. Rastani^{*a}, H. Babai^b

^a Department of Electrical Engineering, School of Technology and Engineering, University of Qom, Qom, Iran

^b Graduate Student, Department of Science, University of Qom, Qom, Iran

PAPER INFO

Paper history:

Received 12 July 2017

Received in revised form 16 November 2017

Accepted 14 January 2018

Keywords:

Plasma Deposition

Thin Film Transistor

Display

Process Optimization

Low Temperature Dielectric

ABSTRACT

Deposition process for thin insulator used in polysilicon gate dielectric of thin film transistors are optimized. Silane and N₂O plasma are used to form SiO₂ layers at temperatures below 150 °C. The deposition conditions as well as system operating parameters such as pressure, temperature, gas flow ratios, total flow rate and plasma power are also studied and their effects are discussed. The physical aspects of the yielded dielectrics such as layer thickness and uniformity are presented as well.

doi: 10.5829/ije.2018.31.05b.05

1. INTRODUCTION¹

Active matrix liquid crystal displays use thin film transistors (TFTs) to address liquid crystal pixels. The first generation TFTs were relying upon hydrogenated amorphous silicon (a-Si:H) as the gate electrode with silicon nitride as the dielectric material [1]. While this was suitable for small displays, for larger ones consisting of huge number of rows and columns, that required high speed addressing circuitry, the structure had to be improved. That is because the high speed addressing schemes normally use CMOS circuits which need high mobility materials to make TFT respond fast enough to these devices [2]. However, The small electron field effect mobility of amorphous material ($< 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), was not adequate and as a result, transition from amorphous to polysilicon with mobility of greater than $30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was inevitable [3]. This change helped with the addressing speed. However, the inherent issues of poly with nitride such as the mismatch between Si and Si₃N₄ due to their valence band offset as

well as the wide valence band tail of silicon nitride became the new impediments that had to be reckoned with literature [4]. Therefore, silicon nitride was considered less desirable insulator and had to be replaced. Even though other dielectrics [5-8] have been developed, but for the reasons of compatibility with the polysilicon gate, only SiO₂ was a practical alternative. Other reason for this choice was that CMOS technology tends to use SiO₂ as the insulator and with the advent of technology which called for integrating TFTs with their CMOS driving circuitry and addressing schemes on the same display substrate; SiO₂ became a universal dielectric material [9].

Since during fabrication of displays on glass substrate, SiO₂ deposition temperature of greater than 600 °C could not be tolerated, all attempts were made to reduce the deposition temperature and keep it below that upper limit. In 2005, Kim, et al. [10] deposited SiO₂ for TFT applications using atmospheric pressure chemical vapor deposition at 400 °C. Furthermore, Maeda and Nakamura [11] revealed the deposition kinetics of SiO₂ film formation at the same temperature.

^{*}Corresponding Author's Email: siroorastani@hotmail.com (S. Rastani)

In addition, since plasma utilization in processing of different materials was considered common place [12-15], Hattangady et al. [16] have made use of remote plasma to produce SiO₂ at 300 °C. Batey and Tierney [17] studied the deposition between 275-350 °C. However, for the more delicate and flexible plastic substrates such as polyethylene terephthalate (PET), the deposition temperature cannot exceed 150 °C.

This study therefore, aims to investigate the deposition of SiO₂ for TFT applications at and below 150 °C, and then to optimize the process conditions found so that they can be used in any established manufacturing environment. To achieve this goal, the system described below is used to produce the layers. Then the films were analyzed, and the data optimization performed. This paper is organized as follows. In section 2, experimental procedure and initial process conditions are presented. The effect of temperature on deposition rate which found to be an inverse relation is covered in section 3.1. Total flow rates of gases as well as the ratio of active gases are varied and results are discussed in sections 3.2. and 3.3. The curve for predicting the time required for any thickness desired and the effect of pressure an plasma power on film thickness are all presented in the following sections. Finally, the optimum process values are introduced.

The TFT structure is shown in Figure 1. It consists of usual polysilicon layer on top of silicon dioxide. The gate is located underneath (inverted) and source and drain overlap the gate by small amount (scattered), hence the name “inverted scattered TFT”.

The oxide formation constitutes the heart of this structure where the induction of channel development takes place. The followings are the stages of depositing SiO₂ layer.

2. EXPERIMENTAL PROCEDURE

The deposition of layers is accomplished inside a water cooled flat capacitive reactor 12 inches in diameter as depicted in Figure 2. The details of the system are described in another report [18] but the generalities of the system are presented here. The generalities of the system are presented here. The reacting gases are supplied through mass flow controllers as illustrated in Figure 2. However, due to its high reactivity with oxygen, silane was not allowed to mix with oxygen before reaching the chamber, i. e., it was introduced through a separate line. The SiH₄ gas cylinder consisted of 20% silane gas in the remaining N₂. There is also a nitrogen supply that acts as the carrier gas. As shown, the active gases are introduced through top electrode while the exhaust gases are vacuumed through underneath of the bottom electrode. To maintain an operating pressure, a throttle valve is employed right at the exit of the chamber before the rotary pump.

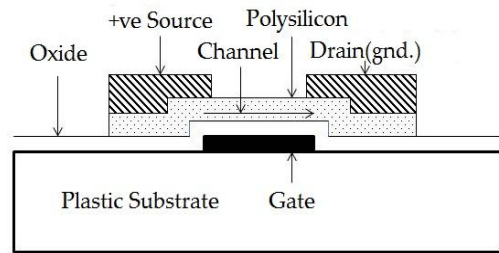


Figure1. Inverted scattered TFT Structure on flexible substrate

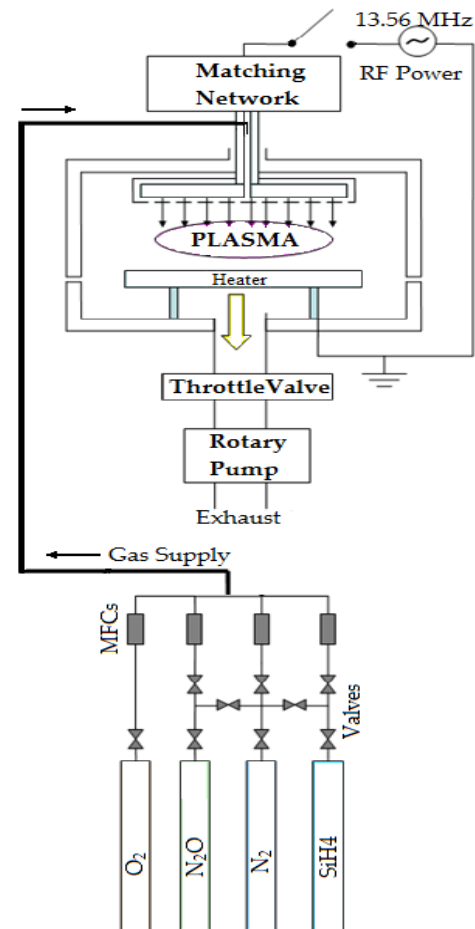


Figure 2. The plasma deposition system employed

Before each run, besides the usual nitrogen purging of the system, the internal parts and electrodes were cleaned by following a protocol summarized in Table 1. The procedure consists of employing CF₄ plasma to etch away any oxide/contamination remained from the pervious run. This cleaning should leave the system free of any observable oxide particles. In following with the procedure in Table 1, one has to note that an increase in chamber pressure above the mentioned value has a hindering effect on the effectiveness of the cleaning

procedure. Specifically, raising the pressure to 800 mTorr will completely cease the cleaning and contamination/oxide in the system remains intact.

Polyethylene terephthalate films are used as flexible plastic substrates. The substrates are placed on the lower flat electrode before running the system. In these experiments, N_2O is used as the source for oxygen and the active gases are accompanied by nitrogen as the carrier/diluents gas. The initial deposition protocol followed is given in Table 2.

As it would be discussed in the next section, each one of these deposition parameters is then varied around the mentioned initial value in Table 2 so that its effect on the resulting layer can be obtained. Therefore, using Table 2 different thicknesses of SiO_2 are deposited.

3. DISCUSSION

3. 1. Effect of Temperature on Deposition Rate

In order to determine the optimum point, various experiments were performed around the 150 °C. The results are shown in Figure 3.

As the data shows, the deposition rate decreases with increasing temperature and continues beyond 150 °C. To obtain this data, only temperature was varied and all other parameters such as pressure and flow rate are kept constant. As far as the quality of the films is concerned, it is found that the lower rates resulting from higher temperatures correspond to denser, less porous layers. These less porous dielectrics are further investigated for etch rate and it was observed that they have smaller etch rates. Therefore above 150 °C the qualities of the films

TABLE 1. CF4 system cleaning protocol

Plasma Power	Chamber Pressure	Duration	Temperature
100 W	250-350 mTorr	30 min	30 °C

TABLE 2. Initial deposition conditions

Temperature	Pressure	Power	Total Flow rate
150 °C	170 mTorr	70 W	92 sccm

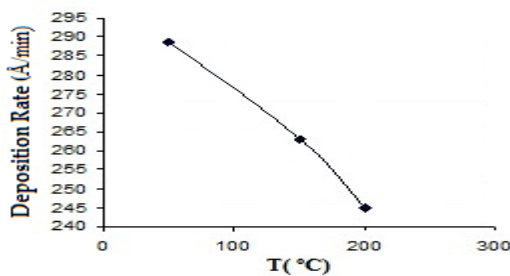


Figure 3. Deposition Rate versus temperature

were superior. The deposition rate at 150 °C was 263 Å/min as depicted.

From the above discussion, for the most optimized temperature, although below 150 °C the deposition rate would be higher, the quality of the oxide film will start to degrade. Thus, the highest temperature tolerable is the optimized temperature at 150 °C as well.

3. 2. Effect of Total Flow Rate The total flow mentioned in Table 2 is the calculated sum of the silane, N_2O and N_2 gases from the mass flow controllers (MFC) in the system. The mentioned total flow is very close to the maximum capacity of the system, generating about 170 mTorr of pressure when the throttle valve is completely open. To find the optimum values for N_2O/SiH_4 and total flow rate, one must know the relationship between total flow, gas ratios and the deposition rate.

Figure 4 shows the results of the experiments performed at total flow rates of 34, 47, 67 and 92 sccm. Although, the three curves on the right side of the graph show the same overall trend, but as the total flow rates change from 34 to 92 sccm, the deposition rate for each curve goes slightly higher. Unfortunately, above 92 sccm there is not much room left for the mass flow controllers on the system to increase total flow any further.

To obtain even higher deposition rates, as is discussed later, the N_2O/SiH_4 flow ratio instead of total flow must be studied.

3. 3. Effect of N_2O/SiH_4 Flow Ratio

Referring to the same Figure 4, it is clear that as the N_2O/SiH_4 ratio increases, the three curves on the right tend to go toward lower deposition rates. For example, on the 34 sccm curve when the gas ratio reaches to 105, the lowest deposition rate, namely; 28.3 Å/min is obtained. One explanation might be that at these low silane levels, the Si species of the gas mixture is about one hundredth of the oxygen level producing little film. It seems that for ratios higher than 105, deposition rate would reduce toward zero. It is obvious then that if there is no silane in the gas mixture, no layer is expected.

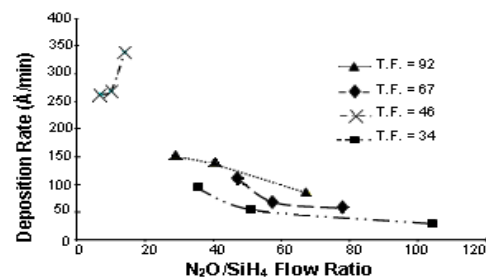


Figure 4. Deposition rate versus flow rate ratios for different total flows

Furthermore, it seems that increasing the total flow from 34 to 92 sccm, will have the effect of raising the whole curve by small amount. But overall trend will not change.

Conversely, on each of these curves, as the N_2O/SiH_4 ratio reduces in magnitude (going from 105 toward 30), the deposition rate increases. In other words if one continues toward even smaller ratios it is expected that the deposition rate should increase even further. The data points on the left of the three curves in Figure 4 are from experiments run at ratios of 14, 10 and 7. The rates are in the range of 250 to 350 Å/min which are about 100 Å/min higher than 3 curves on the right. Of course, these points were obtained from experiments performed with 46 sccm total flow, i.e., they are not run with total flows of 34, 67 or 92 sccm.

Therefore, this motivates one to look at deposition rate using a complete spectrum of N_2O to silane gas ratios. That is, in addition to parameters specified in Table 2, N_2O/SiH_4 ratios must be varied over the whole range as shown in Figure 5. These experiments were obtained with 92 sccm total flow.

The trend toward a maximum and then descending down is quite clear. One can see that the same general trend of curves in Figure 4 is recurring here as well. That is, for low ratios of N_2O/SiH_4 (4 to 15), high deposition rates of 46 sccm on the left side of Figure 4 were repeated here. Moreover, beyond the maximum as the N_2O/SiH_4 ratio was changed from 15 to 105, the same inclination of lowering deposition rate as seen in Figure 4, reappeared here too.

Therefore, regardless of what amount of total flow is being sent into the chamber, one obtains the same overall shape of Figure 5 for various gas ratios. That is, although the curves displace up or down slightly, their profile does not change much. On the contrary, N_2O/SiH_4 flow ratios have dramatic effect on the deposition rate.

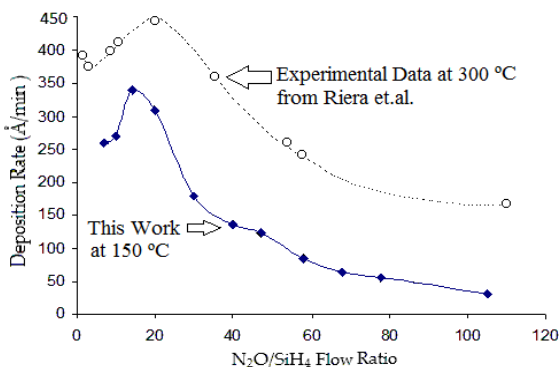


Figure 5. Deposition rate vs. N_2O/SiH_4 flow ratios at 150 °C and 92 sccm

It has to be noted that Figure 5 indicates that the results of this study is very similar to what has been reported by Riera et al. [18]. Even though their experiments were performed at 300 °C which is not acceptable for plastic substrates but nevertheless the same overall trend was observed in their work as well.

One possible explanation for this shape is that at high N_2O/SiH_4 ratios there is much more active oxygen species available in the chamber than Si active species, causing the surface to be covered by oxygen species. This coverage of the surface prevents the Si gas species to reach and react with the developing solid film. Hence, the deposition rate diminishes. This is clearly an example of classic **surface reaction rate limited** growth case.

On the other hand, at low N_2O/SiH_4 ratios the deposition rate increases and at about 15, it reaches to a maximum value. One explanation could be the fact that at small N_2O/SiH_4 ratios the active species of Si in the gas phase are enough to react with oxygen and develop the layer. This is obviously a **mass-transfer limited** process. Therefore, right at flow ratio of 15, the process transforms from surface reaction limited into mass transfer limited.

Therefore, for optimization purposes, the maximum deposition rate is obtained right at $N_2O/SiH_4 = 15$ or somewhere around that value. This ratio is occurring at total flow of 92 sccm which as mentioned before is the maximum capacity that the system can handle.

3. 4. Thickness Versus Time

The thickness obtained versus time along with the equation that models this relationship is illustrated in Figure 6. It is possible to calculate the time needed for depositing specific thickness of the oxide layer.

3. 5. Effect of Pressure on Deposition Rate

A series of experiments at different pressures, keeping the rest of parameters the same, were performed. The results are depicted in Figure 7.

The variations of pressure, at least in the range of 120 to 900 mTorr, does not seem to affect the deposition process. Deposition rate is revolving around 310 Å/min. However, other properties of layer changed with pressure. For example, Figure 8 shows an increase in the pressure decreases the uniformity. For this data, the usual definition of uniformity is used:

$$\text{Uniformity} = \frac{(d_{\max} - d_{\min})}{2d_{\text{ave}}} \times 100$$

where, d_{\min} , d_{\max} and d_{ave} are minimum, maximum and average thickness, respectively. Thickness is measured at 5 farthest points on the surface of the substrate and the average is calculated among them.

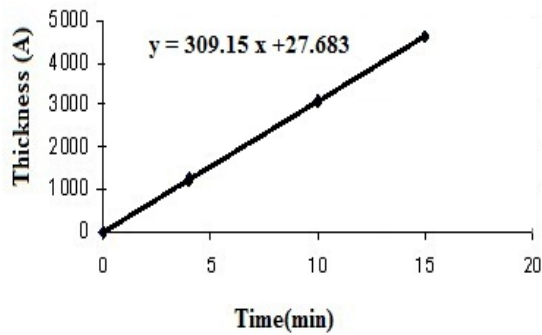


Figure 6. Thickness as a function of time

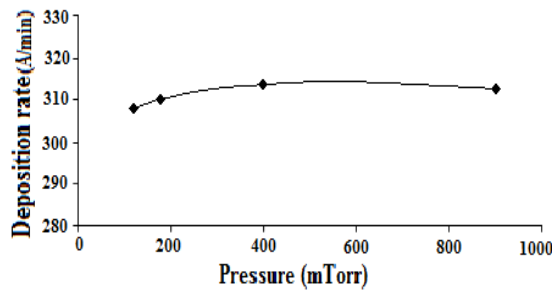


Figure 7. Deposition rate for different pressures

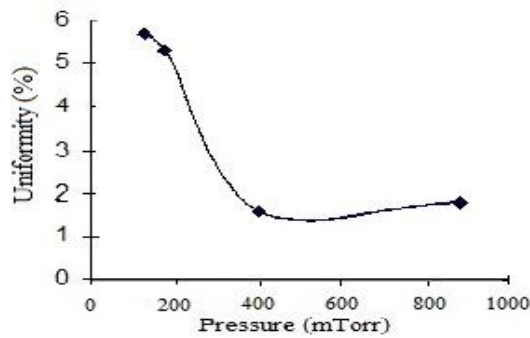


Figure 8. Uniformity as a function of pressure

The data also indicate that for optimum uniformity, the pressure must be kept above 400 mTorr.

Moreover, Figure 9 shows the effect of N_2O/SiH_4 ratio on the uniformity, the opposite is found. That is, as the ratio goes toward higher oxygen content and lower silicon species, uniformity goes from 5% to about 20%. In other words, the non-uniformity starts to take over.

Therefore, to have more uniform layer, one has to keep the N_2O/SiH_4 ratio below 67. This also satisfies the optimum point of $N_2O/SiH_4 = 15$ that was found in section 3.3.

3. 6. Effect of Plasma Power on Deposition Rate and Uniformity

Studying the deposition rate and uniformity show that with an increase in plasma power, these two factors of the thin film increases as well. Figure 10 illustrates that when power goes from 50 watts to 120 watts, for 140 mTorr of pressure, the deposition rate changes from 120 Å/min to 525 Å/min which is more than four folds. In addition, Figure 11 indicates that the uniformity for the same conditions varies from 1 to 3 percent. Considering the curve corresponding to 400m Torr pressure, it is clear that both graphs show the same trend of increase in these parameters. Both curves intercept at about 70 watts. Therefore, choosing this power level as the optimum point resulted in the same deposition rate and uniformity at different pressures.

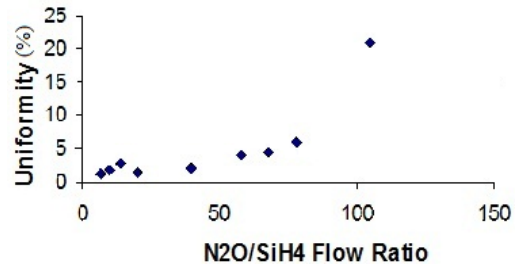


Figure 9. Effect of N_2O/SiH_4 ratio on uniformity (%)

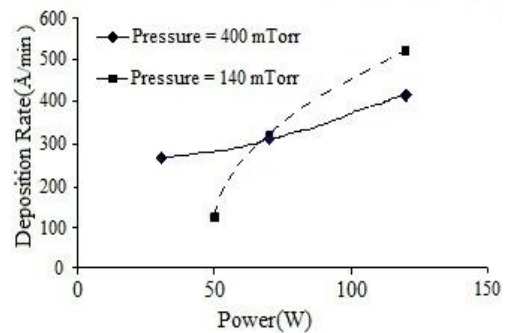


Figure 10. Effect of power on deposition rate

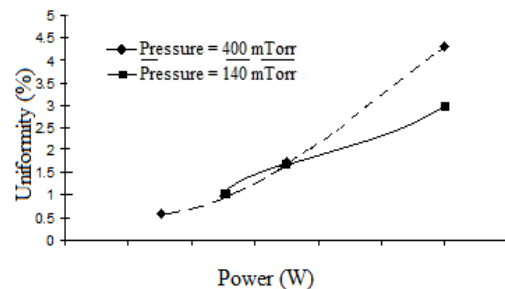


Figure 11. Uniformity versus power and pressure

5. CONCLUSION

Although the initial protocol of Table 2 was the starting point for experiments; however, for the manufacturing of TFT's the optimized process conditions are summarized in Table 3.

TABLE 3. Optimized process conditions

Deposition Temperature	Operating Pressure	N ₂ O/SiH ₄ Gas Ratio	Total Flow	Power rate
150 °C	>400 mTorr	15-67	92 sccm	70 W

6. ACKNOWLEDGEMENT

The authors would like to gratefully acknowledge the support from University of Qom.

7. REFERENCES

- Reita, C., "Integrated driver circuits for active matrix liquid crystal displays", *Displays*, Vol. 14, No. 2, (1993), 104-114.
- Brotherton, S., "Polycrystalline silicon thin film transistors", *Semiconductor Science and Technology*, Vol. 10, No. 6, (1995), 721-738.
- Edwards, M., "Nmos and cmos polysilicon drive circuits for liquid crystal displays", *IEE Proceedings-Circuits, Devices and Systems*, Vol. 141, No. 1, (1994), 50-55.
- Robertson, J., "Electronic structure of silicon nitride", *Philosophical Magazine B*, Vol. 63, No. 1, (1991), 47-77.
- Vaezi, M. and Zameni, M., "Synthesis of zinc oxide nanostructured thin film by sol-gel method and evaluation of gas sensing properties", *International Journal of Engineering-Transactions B: Applications*, Vol. 27, No. 5, (2013), 757-762.
- Nikzad, L., Vaezi, M., Alibeigi, S. and Esmailzadeh, K.A., "Preparation of cobalt oxide/zinc oxide nanocomposite", *International Journal of Engineering-Transactions B: Applications*, Vol. 27, No. 5, (2010), 131-135.
- Khalili, V., Khalil, A.J. and Maleki, G.H., "Titanium oxide (tio₂) coatings on niti shape memory substrate using electrophoretic deposition process", *International Journal of Engineering-Transactions A: Basics*, Vol. 26, No. 7, (2013), 707-712.
- Hossein, B.F. and Orvatinia, M., "Thickness dependence of sensitivity in thin film tin oxide gas sensors deposited by vapor pyrolysis", *International Journal of Engineering-Transactions B: Applications*, Vol. 16, No. 1, (2003), 33-40.
- Ohwada, J.-I., Takabatake, M., Ono, Y.A., Nagae, Y., Mimura, A., Ono, K. and Konishi, N., "Peripheral circuit integrated poly-si tft lcd with gray scale representation", in Display Research Conference, 1988., Conference Record of the 1988 International, IEEE. (1988), 215-219.
- Kim, J., Hwang, S. and Yi, J., "Sio₂ films deposited at low temperature by using apcvd with teos/o₃ for tft applications", *Journal of the Korean Physical Society*, Vol. 49, No. 3, (2006), 1121-1125.
- Maeda, M. and Nakamura, H., "Deposition kinetics of sio₂ film", *Journal of Applied Physics*, Vol. 52, No. 11, (1981), 6651-6654.
- Padmanabhan, K. and Prabhu, G., "Experimental investigation by cryogenic treatment of aluminium 6063 and 8011 and nicow coating to improve hardness and wear", *International Journal of Engineering-Transactions C: Aspects*, Vol. 29, No. 6, (2016), 827-833.
- Golbakhshi, H., Namjoo, M. and Estabragh, E.R., "Evaluating the effects of ceramic layer and thermal dam on optimizing the temperature gradient of a gasoline engine piston", *International Journal of Engineering-Transactions A: Basics*, Vol. 28, No. 10, (2015), 1525-1532.
- Azadia, M., Rouhaghdam, A.S. and Ahangarani, S., "Effect of temperature and gas flux on the mechanical behavior of tic coating by pulsed dc plasma enhanced chemical vapor deposition", *International Journal of Engineering-Transactions B: Applications*, Vol. 27, No. 8, (2013), 1243-1250.
- Akhondzadeh, M., FOOLADI, M.M., Mansouri, S. and Rezaeizadeh, M., "A new procedure of impact wear evaluation of mill liner", *International Journal of Engineering-Transactions A: Basics*, Vol. 28, No. 4, (2015), 593-598.
- Hattangady, S., Alley, R., Fountain, G., Markunas, R., Lucovsky, G. and Temple, D., "Effect of rf power on remote-plasma deposited sio₂ films", *Journal of Applied Physics*, Vol. 73, No. 11, (1993), 7635-7642.
- Batey, J. and Tierney, E., "Low-temperature deposition of high-quality silicon dioxide by plasma-enhanced chemical vapor deposition", *Journal of Applied Physics*, Vol. 60, No. 9, (1986), 3136-3145.
- Riera, M., Rodriguez, J., Barreto, J. and Domínguez, C., "Modeling of non-stoichiometric silicon oxides obtained by plasma enhanced chemical vapour deposition process", *Thin Solid Films*, Vol. 515, No. 7-8, (2007), 3380-3386.

Process Optimization of Deposition Conditions for Low Temperature Thin Film Insulators used in TFT Displays

S. Rastani^a, H. Babai^b

^a Department of Electrical Engineering, School of Technology and Engineering, University of Qom, Qom, Iran

^b Graduate Student, Department of Science, University of Qom, Qom, Iran

P A P E R I N F O

چکیده

Paper history:

Received 12 July 2017

Received in revised form 16 November 2017

Accepted 14 January 2018

Keywords:

Plasma Deposition

Thin Film Transistor

Display

Process Optimization

Low Temperature Dielectric

دی الکتریک لازم برای گیت پلی سیلیکان ترانزیستور های لایه نازک نمایشگرها ی مسطح تهیه و فرآیند ساخت بهینه سازی گردیده است. از پلاسمای گازهای سیلان و اکسید نیتروژن برای ساخت اکسید سیلیسیوم در دمایی پایین تر از ۱۵۰ درجه سانتیگراد استفاده شده است. شرایط لایه نشانی و پارامتر های عملیاتی سیستم مانند فشار، دما، نسبت شار گازها، شار کل و توان پلاσμα مورد مطالعه و اثر هر کدام مورد بحث قرار گرفته است. همچنین خواص فیزیکی دی الکتریک بدست آمده نظیر قطر لایه و یکنواختی آن ارائه گردیده است.

doi: 10.5829/ije.2018.31.05b.05
