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A New Structure for 6 Bit Distributed MEMS Transmission Line Phase Shifter in Ku Band

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ABSTRACT

In this paper, using only 32 MEMS switches, a new design for 6 bit DMTL phase shifter is proposed. The reduction in number of switches in ordinary 6 bit phase shifter from 63 to 32 is due to combination of one 5.625 degree for least significant bit and 11.25 degree for the rest of the switches. In new proposed method, the die size and loss of the CPW line reduced by decreasing the number of the switches. Analytical and finite element simulation with HFSS and COMSOL software, is used for considering the performance of the proposed structure. The results showed that, maximum return loss of phase shifter and mean RMS phase error are -10.5 dB and1.4°, respectively. Although two different micro switches are used but the pull in voltages are identical. The final configuration size is $1.5 \times 18.5\ \mathrm{mm}^2$, and surface micromachining process is suggested for the phase shifter manufacturing.

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1. INTRODUCTION

Phase shifters are a serious component in several RF, military industry and microwave systems. Applications include controlling the relative phase of each element in a phase array antenna in a remote communication or steerable communications link and in cancelation loops used in high linearity amplifiers[1, 2]. Depending on the application, design approach of phase shifter is classified into two groups' viz., digital and analog [3]. According to phase shifter applications each of them has its own advantageous and disadvantageous. One of the most standard methods for implementing digital phase shifters is distributed MEMS transmission line (DMTL) [4]. The DMTL systems uses continuous number of shunt capacitive switches [5-9] and can be fabricated on micro strip [10, 11] or coplanar waveguide lines (CPW) [12-15]. Micro strip line requires via whole or radial stub which decreases quality factor and for DMTL phase shifter CPW structure is more efficient [3].

In digital approach, the DMTL phase shifters has a DC bias voltage which is applied to amount of required bits and the capacitance between line and switches variations hence the impedance of line alters, by varying the line impedance the phase of signal passing though the CPW line modifies[16]. Hayden and Rebeiz [13] 2-bit wide-band distributed coplanar-waveguide phase shifters has been offered by 21 capacitive shunt switches which 7 of distributed MEMS transmission line were devoted to first bit and rest of them to the second one. Each switch is capable of 12.857^{o} phase shift and 90 and 180 degree is shifted by turning the first and second bit's switches on, respectively. These results are very economical with switched transmission-line and reflection-based phase shifters.

Chen et al. [17] have developed a 4 bit phase shifter which was proposed for Ka-band operation. They have employed 15 shunt capacitive switches with 11.25 degree phase shift for each switch in this work and maximum phase shift is 168.75 degrees and bigger phase shifts are not possible. This low-loss distributed metal-air-metal MEMS phase shifter can be well functional to phased arrays.

As the number of bits of phase shifter increases, more number of switches configuration in on and off state should be studied. For example for 6 bit phase shifter, 63 conditions have to be studied but usually just few number of conditioned are studied such as 5.625^{o},

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11.25^o, 22.5^o,45^o, 90^o, 180^o and although probing the all condition are so critical in the total performance of the system, according to the best knowledge of the author of this article, there is no literature which covers all possible condition for 6 bit phase shifter.

In order to design of 6 bit phase shifter, present structure decreasing number of switches and leads to smaller size which is very prominent issue for designers. Afrang et al. [6] have presented a new structure for 6 bit phase shifter for Ka band which contains just 32 switches instead of 63 switches for ordinary 6 bit phase shifter. They have presented a MEMS capacitive switch together with two additional electrodes near the RF line under the bridge, which is capable of altering the phase of signal for two different values ($5.625^o and 11.25^o$). Electrostatic force for phase shifts 5.625° through two additional electrodes, and for phase shifts 11.25° through the RF line were applied to the bridge. So this switch requires two different actuation voltages for each condition. Also, two additional electrodes with a different height than the other parts of cause an increase in the number of the stages of the fabrication process.

The results showed for the DMTL phase shifters with more bits and consequently with small least significant bit, the size of the phase shifter will be large. In this paper, to decrease the size of the phase shifter, a new low-loss distributed design of MEMS switch is proposed. Two different switches have been used for 5.625 and 11.25 degree phase shift. Identical actuation voltage is used for all switches which will be discussed in details in the following sections.

2. THEORY OF THE PROPOSED STRUCTURE

In Figure 1 the proposed MEMS phase shifter is composed of CPW line and 32 shunt capacitive switches which are depicted. The total structure is composed of shunt capacitive switches with predefined spacing which is called unit cell. Each switch of Figure 1, is fixed-fixed beam that is illustrated in Figure 2, in up and down position. There are two static MAM capacitors connected to the ends of the bridge ($C_s/2$). The equivalent capacitor of $C_s/2$ and bridge capacitance in up and down position is called C_{up} and C_{down}, respectively. It is worthy to note that in down position the bridge capacitance increases to Pico Farad range and the equivalent becomes C_s. first switch is allocated for 5.625 degree phase shift and the rest of them are identical and 11.25 degree is shifted by each of 31 switches. First bit switch and one of the second bit's switch is shown in Figure 2, in on and off conditions.

Electrical model of the switches is shown in Figure 3. In this figure, L_t is the per unit inductance and $C_t$is the capacitance of the unloaded line with impedance Z_0.

The Switches in DMTL phase shifter in up and down conditions altered the impedance of the line which change the return loss of the CPW. Impedance mismatch in DMTL phase shifter leads to return loss. The governing equation for reflection coefficient is:

$$\Gamma in = 10^{\frac{R_{Lmax}}{20}} \quad (1)$$

where, R_{Lmax} is maximum return loss.

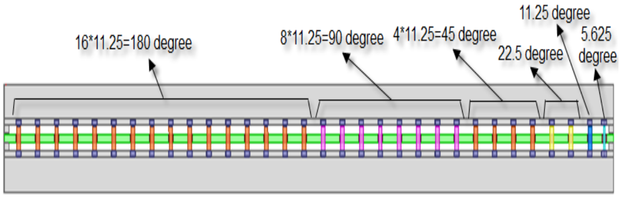
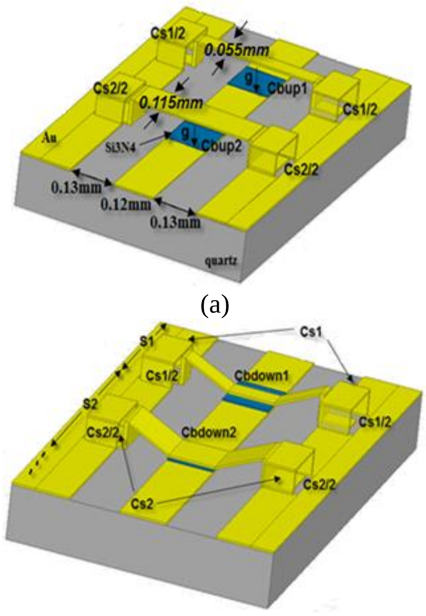


Figure 1. Total structure of proposed 6 bit phase shifter whit 32 switches



(a)

(b)

Figure 2. Structure of switches in up and down positions

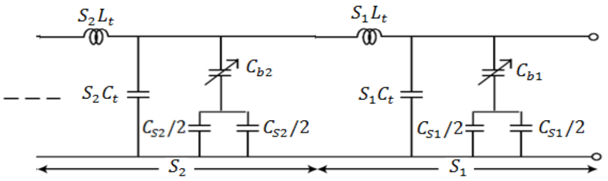


Figure 3. Electrical model of switches

According to literature [3], in ideal conditions the overall phase shifter return loss should be smaller than -10dB. To achieve this criteria, the return loss of each switch is considered to be -15dB. Therefore, the impedance of the switch in up and down condition can be calculated through the following equations:

$$R_{\mathrm{Lmax}} = -15 \text{ dB} \quad \rightarrow \Gamma\mathrm{in} = 10^{\frac{-15}{20}} = 0.178$$

$$Z_{Lup} = 50\sqrt{\frac{1+\Gamma_{\mathrm{in}}}{1-\Gamma_{\mathrm{in}}}} = 59.8 \tag{2}$$

$$Z_{Ldown} = 50\sqrt{\frac{1-\Gamma_{\mathrm{in}}}{1+\Gamma_{\mathrm{in}}}} = 41.8 \tag{3}$$

were Z_{Lup} and Z_{Ldown} are loaded-line impedance in the high capacitance state and highest capacitive loading on the line, respectively. Accordingly, the line impedance in up and down states must be less than 60 and 42 ohm, respectively. Also, the computations expressed that in the proposed DMTL phase shifter, the up and down impedance is considered to be 58 and 43 ohm, respectively.

The phase shift by each switch and distance between them is formulated in Equations (4) and (5)[18].

$$\Delta\emptyset = \mathrm{Z}_0 \frac{\mathrm{s}\omega\sqrt{\varepsilon_{\mathrm{r,eff}}}}{\mathrm{c}}\left(\frac{1}{\mathrm{Z_{Lup}}} - \frac{1}{\mathrm{Z_{Ldown}}}\right)\frac{\text{degree}}{\text{section}} \tag{4}$$

$$s = \frac{Z_{Ldown} \times C}{Z_0 \pi f_B \sqrt{\varepsilon_{r,eff}}}(\mathrm{m}) \tag{5}$$

where, $\mathrm{F_B}$ is brag frequency and $\varepsilon_{r,eff}$ is effective dielectric constantof the unloaded t-line that is defined as follows:

$$\varepsilon_{r,eff} \cong \frac{1+\varepsilon_r}{2} \tag{6}$$

Substituting $Z_{Lup} \times Z_{Ldown} = 2500$ into Equation (4), the phase shift obtained as:

$$\Delta\emptyset = \frac{360 f_0}{2500\pi f_B}({Z_{Ldown}}^2\text{-}2500)\frac{degree}{section} \tag{7}$$

For the each switches, the capacitance value can be determined as follows:

$$C_{Lup} = Z_{Ldown}\frac{({Z_0}^2 - {Z_{Lup}}^2)}{{Z_0}^2 {Z_{Lup}}^2 \pi f_B} Farads \tag{8}$$

$$C_r = \frac{({Z_0}^2 - {Z_{Ldown}}^2)}{({Z_0}^2 - {Z_{Lup}}^2)}\left(\frac{Z_{Lup}}{Z_{Ldown}}\right)^2 Farads \tag{9}$$

$$C_s = C_{ldown} = C_r \times C_{Lup} Farads \tag{10}$$

$$C_{Lup} = \frac{C_{bup} \times C_s}{C_{bup} + C_s} Farads \tag{11}$$

For linearity consideration $f_{\mathrm{B}} > 2f_0$, where $\mathrm{f_0}$ is operating frequency [3, 5]. Since, due to loading effect of the switches the impedance of CPW line decreases, so, the characteristic impedance has to be chosen higher than 50 ohm [3, 15]. Increasing the characteristic impedance of signal line would lead to increscent the phase shift which desirable and return loss that would degrade the performance of the phase shifter. Return loss is related exponentially to the characteristic impedance so there is a trade-off between the phase shift and return loss by adjusting the characteristic impedance. In DMTL phase shifters with quartz substrate ($\varepsilon_{\mathrm{r}} = 3.75$, $\varepsilon_{\mathrm{r,eff}} = 2.38$), characteristic impedance should be between 80 and 100 ohm to achieve maximum phase shift and minimum loss. Because of the impedance of the unit cell in upstate and downstate 58.14 and 43 ohm, respectively. Therefore, using Equation (4), the Z0 is obtained as 95.2 ohm. Consequently, the width of RF line and the spacing between RF line and ground are 120 and 130 micrometer, respectively. Specifications of two type of switches (5.625 and 11.25 degree) are listed in Table 1.

The proposed DMTL phase shifter can be fabricated through surface micromachining method. According to Table 1 the capacitance of bridge for 5.625° unit cell is half of the capacitance of 11.25° unit cell, so the ratio of the width of first bit to second bit is 0.5. The air gap (g) for all bridges is considered to be 1.6μm. So, no extra step is added to fabrication process and the size of the DMTL phase shifter is decreased noticeably. The spacing between 11.25°switches is $S_2 = 586$ μm and for 5.625° switch is $S_1 = 293$ μm so the total structure size becomes 18.5mm which is illustrated in Figure 4.

3. VERIFICATION

Simulation result could be classified into two categories. Electromagnetic simulation is carries out by ANSYS HFSS software and pull in voltage of switches is scrutinized by COMSOL software.

TABLE 1. Specification parameters for 5.625° unit cell and 11.25° unit cell

Parameter	Switch Type 1	Switch Type 2
$\Delta\emptyset$ (degree)	5.625	11.25
f_0(GHz)	18	18
$Z_0(\Omega)$	95.2	95.2
f_{B}(GHz)	95.4	47.7
S (μm)	293	586
$Z_{\mathrm{Ldown}}(\Omega)$	43	43
$Z_{\mathrm{Lup}}(\Omega)$	58.14	58.14
C_{r}	2.32	2.32
C_{Lup}(fF)	26.62	53.23
C_{s}(fF)	61.8	123.5
C_{bup}(fF)	46.76	93.5

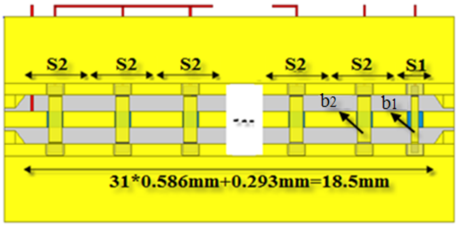
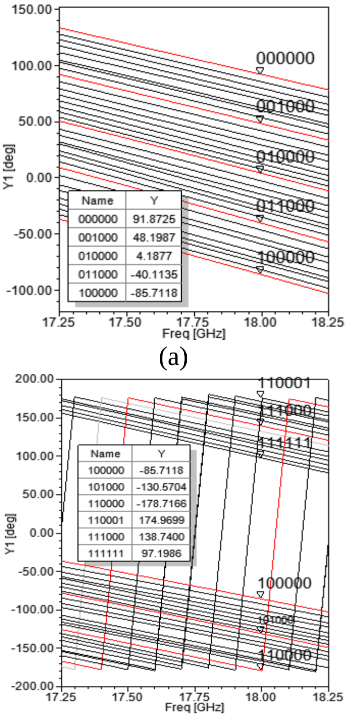


Figure 4. Top view of the proposed phase shifter

3. 1. Electromagnetic Simulation In the proposed new phase shifter, phase shift, insertion loss and return loss are simulated for all 64 conditions (0^o, 5.625^o, 11.25^o, $16.875^o, 22.5^o$, ..., 354.375^o) by HFSS software. Applying electrostatic force to the selected switches, their condition is altered from OFF to ON conditions and introduced phase change to the signal. For example for 253.125^o phase shift first, third, fourth and sixth bits have to be turned ON. The simulation results for all distinct situations are shown in Figures 5(a) and 5(b).

As it is shown in Figure 5(a) for $000000 \equiv 0^o$ the value of phase is 91.8725 degree and is considered to be the reference value and the rest of the phases are compared with this reference. Phase error and shifts for all possible conditions are represented in Tables 2 and 3.



(a)

(b)

Figure 5. Phase shift, **(a)** from $000000 \equiv 0^o$ to $100000 \equiv 180^o$, **(b)** from $100000 \equiv 180^o$to$111111 \equiv 354.375^o$

TABLE 2. The Phase shift and error for 0^o to 180^oconditions

Phase state	Phase shift	Phase error	Phase state	Phase shift	Phase error	Phase state	Phase shift	Phase error
0	0	0	61.875	62.6085	0.7335	123.75	121.0884	-2.6616
5.625	6.453	0.828	67.5	69.2765	1.7765	129.375	126.602	-2.773
11.25	12.2265	0.9765	73.125	74.542	1.417	135	131.986	-3.014
16.875	17.8983	1.0233	78.75	79.3409	0.5909	140.635	138.0975	-2.5775
22.5	22.2352	-0.2648	84.375	83.9413	-0.4337	146.25	145.6627	-0.5873
28.125	29.2352	1.1102	90	87.6848	-2.3152	151.875	150.455	-1.42
33.75	32.2336	-1.5164	95.625	94.4969	-1.1281	157.5	158.5954	1.0954
39.375	38.21	-1.165	101.25	100.9354	-0.3146	163.125	164.1215	0.9965
45	43.6738	-1.3262	106.875	106.2625	-0.6125	168.75	167.6052	-1.1448
50.635	49.9499	-0.6751	112.5	111.2605	-1.2395	174.375	173.2586	-1.1164
56.25	57.1382	0.8882	118.125	117.4572	-0.6678	180	177.5843	-2.4157

TABLE 3. The Phase shift and error for 180^o to 354.375^oconditions

Phase state	Phase shift	Phase error	Phase state	Phase shift	Phase error	Phase state	Phase shift	Phase error
180	177.5843	-2.4157	241.875	238.8325	-3.042	303.75	300.0746	-3.675
185.625	184.083	-1.542	247.5	249.8504	2.3504	309.375	306.296	-3.079
191.25	192.133	0.883	253.125	255.8985	2.7735	315	313.1325	-1.867
196.875	197.6585	0.7835	258.75	258.018	-0.732	320.635	320.2546	-0.370
202.5	204.2172	1.7172	264.375	262.046	-2.329	326.25	328.6013	2.3513
208.125	209.5537	1.4287	270	270.5891	0.5891	331.875	334.318	2.443
213.75	214.4947	0.7447	275.625	276.9026	1.2776	337.5	338.0624	0.5624
219.375	219.004	-0.1746	281.25	281.5634	0.3134	343.125	344.2584	1.1334
225	222.4429	-2.5571	286.875	286.9651	0.0901	348.75	350.3443	1.5943
230.635	228.1601	-2.4649	292.5	289.6509	-2.849	354.375	354.6739	0.2989
236.25	233.9068	-2.3432	298.125	297.2739	-0.851			

Figures 6 and 7 show the S_{11} and S_{12} that are extracted by HFSS.S_{11} and S_{12} are Return loss and Insertion loss, respectively. According to [3] the overall phase shifter return loss should be smaller than -10dB and the result of this paper as it shown in Figure 8 confirmed and S satisfied this issue. In 18GHz for all 64 conditions, return loss is less than -10dB and insertion loss is between -0.9dB and-1.8dB.

3.2. Mechanical Design and Simulation of Switch

As mentioned in the previous sections, the shunt capacitive switches are exploited in design of the proposed phase shifter. The only different between first switch and the rest of them is the width of the first switch is half of the rest.

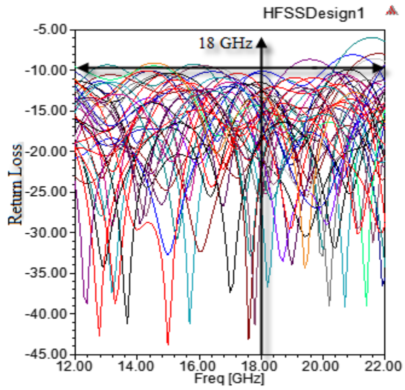


Figure 6. Return loss for all possible from 0 to 54.375 degree

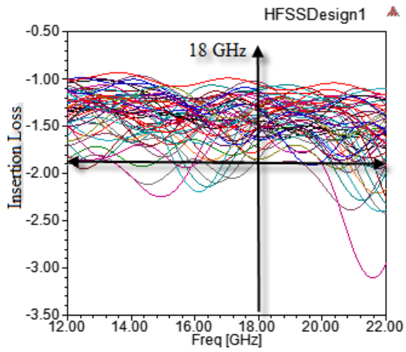


Figure 7. Insertion loss for all possible from 0 to 354.375 degree

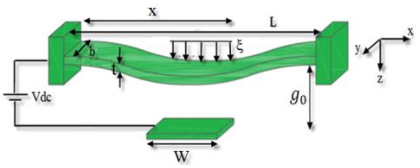


Figure 8. Applying electrostatic force between RF line and bridge

Electrostatic force is applied between the bridge and the RF line to turn the switch ON which is illustrated in Figure 8.

When the MEMS bridge is in the ON position, the corresponding voltage is usually named pull-in voltage can be obtained as follows [11, 19]:

$$V_{pI} = \sqrt{\frac{8\,K}{27\varepsilon_0 bW} g^3} \tag{12}$$

where, b is the membrane width, W is width of RF line, g is air gap between bridge and RF line, ε_0 is dielectric constant of air. The parameter K is spring constant of beam with clamped-clamped boundary conditions which is expressed as follows [3, 20]:

$$K = 32Eb\left(\frac{t}{l}\right)^3 \frac{1}{8\left(\frac{x}{l}\right)^3 - 20\left(\frac{x}{l}\right)^2 + 14\left(\frac{x}{l}\right) - 1} + 8\sigma(1 - \vartheta)b\left(\frac{t}{l}\right)\frac{1}{3 - 2\left(\frac{x}{l}\right)} \tag{13}$$

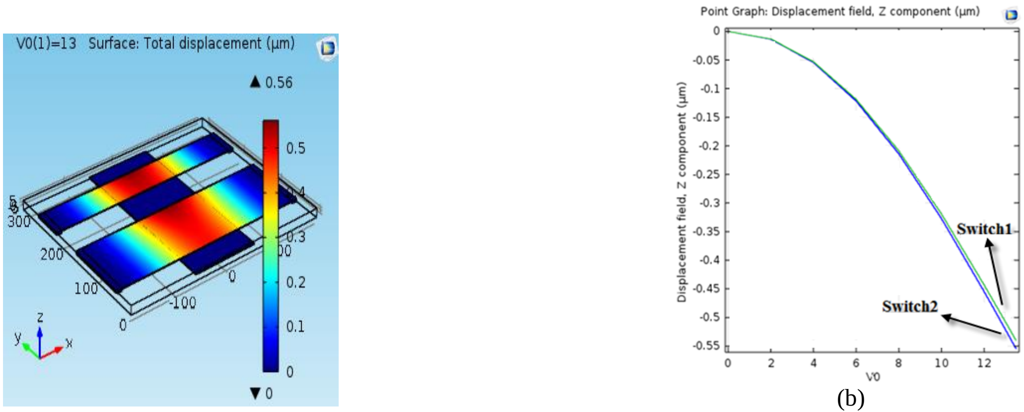
The pull-in voltage of clamped-clamped micro beam can be obtained by substituting Equation (13) into Equation (12) and resultant can be expressed as follows:

$$V_{pI} = \left(\frac{8\,bg^3}{27\varepsilon_0 bW}\right)^{1/2} \times \left(32E\left(\frac{t}{l}\right)^3 \frac{1}{8\left(\frac{x}{l}\right)^3 - 20\left(\frac{x}{l}\right)^2 + 14\left(\frac{x}{l}\right) - 1} + 8\sigma(1 - \vartheta)\left(\frac{t}{l}\right)\frac{1}{3 - 2\left(\frac{x}{l}\right)}\right)^{1/2} \tag{14}$$

where, E is Young's modulus, t is the thickness, L is the length, σ is the residual tensile stress, and v is Poison's ratio [8]. For an Au micro-switch electroplated with 1.2 μm thickness (E=79 GPa, v = 0.43), L = 350 μm, g = 1.6 μm, x=250 μm, and σ = 0 and 20 MPa, the pull-in voltage is obtained 5.2 V and 17.2 V, respectively.

While the width of the first switch is half of the switches, but according to Equation (14) pull-in voltage for all of them are identical. This issue is expected because Pull-in voltage is directly proportional to spring constant of the bridge and inversely related to the capacitance value between the bridge and bottom electrode that here is RF line. As the width of the bridge decreases (other parameters are constant) the capacitance decreases and higher pull-in voltage is expected but this issue is compensated by decreasing the spring constant of the bridge and as a result pull-in voltage remains constant. Simulation results confirm this issue that has been depicted in Figures 9(a) and 9(b).

As it is shown in Figure 9 pull-in voltage of both switches are identical and about 13 Volt. Table 4 listed the comparison results of this work and previous works. The results showed that obtained results has a good agreement with those of previous works.



(a)

(b)

Figure 9. Simulation result for Pull-in voltage of the first and the second bit switches

TABLE 4. Comparison of current state of the art DMTL phase shifters

Parameter	Liu et al. [14]	Topalli et al. [18]	Chen et al. [17]	Dey and Koul [21]	Afrang et al. [6]	This work
Frequency (GHz)	26	15	30	10	30	18
Bit number	3	3	4	5	6	6
Resolution	45^0	45^0	11.25^0	11.25^0	5.625^0	5.625^0
Cell number	14	28	15	62	32	32
Length (mm)	11	22.4	12	19	12.8	18.5
Min insertion loss [dB]	-2.6	-1.9	-1.37	-4.72	---	-1.8
Max return loss [dB]	-7	−10	-10	-12	-11	−10.5
RMS phase error	5^o	---	2.35^0	1.8^0	---	1.4^o
Actuation Voltage (v)	60	16	---	55	3.4 and 6.8	13

4. CONCLUSION

New design for 6-bit DMTL phase shifter with compact number of switches for 18GHz were proposed. Though, the two types of micro-switches with phase shift of 5.625 and 11.25 has been presented impedance matching criteria was considered convincingly. Also identical actuation voltage is used for all switches. Employing two types of different switches led to total size decrement to 18.5mm in comparison with ordinary 6-bit phase shifter with length of 35mm. In this study all 64 possible conditions were well deliberate and simulated with HFSS software. The results indicated that, the design resulted mean RMS phase error were obtained 1.4° and for all conditions return loss is smaller than -10dB which are acceptable values for phase shifters.

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A New Structure for 6 Bit Distributed MEMS Transmission LinePhase Shifter in Ku Band

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چکیده

در مقاله حاضر، ساختاری جدید برای شیفت دهنده فاز شش بیتی DMTLکه تنها ۳۲ سوئیچ MEMS در آن به کار رفته است، ارائه شده است. کاهش تعداد سوئیچ‌های شیفت دهنده فاز شش بیتی از ۶۳ به ۳۲، با توجه به ترکیبی از یک سوئیچ متفاوت در بیت اول جهت شیفت فاز ۵,۶۲۵ درجه و ۳۱ سوئیچ همسان دیگر با قابلیت شیفت فازهای۱۱,۲۵ درجه برای دیگر بیت ها، صورت می پذیرد. کاهش تعداد سوئیچ ها سبب کاهش اندازه شیفت دهنده فاز و در نتیجه کاهش تلفات خط CPW می شود. با استفاده از نرم افزارهای COMSOLو HFSS،مطالعه تحلیلی و شبیه‌سازی ساختار پیشنهادیصورت گرفته است. بر اساس نتایج،ماکزیمم تلفات بازگشتیشیفت دهنده فاز 10.5 dB- و میانگین خطای RMS،۱/۴ درجه است. با وجود داشتن دو نوع سوئیچ با ساختار متفاوت،ولتاژ عملگر برای تمامی سوئیچ ها یکسان است. اندازه کلی ساختار $1.5 \times 18.5\ mm^2$ **بوده و** پروسه میکروماشین کاری سطحی برای شیفت دهنده فاز ارائه شده پیشنهاد شده است.

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