IJE TRANSACTIONS A: Basics Vol. 28, No. 10, (October 2015) 1447-1454

International Journal of Engineering

Journal Homepage: www.ije.ir

TECHNICAL NOTE

Symmetrical, Low-Power, and High-Speed 1-Bit Full Adder Cells Using 32nm Carbon Nanotube Field-effect Transistors Technology

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PAPER INFO

Paper history:
Received 19 August 2015
Received in revised form 06 October 2015
Accepted 16 October 2015

Keywords:
Nanoelectronic
Carbon Nanotube Field-Effect Transistors
Full Adder
Capacitive Threshold Logic
Path Transistor Logic
Low-power
High-speed

ABSTRACT

Carbon nanotube field-effect transistors (CNFETs) are a promising candidate to replace conventional metal oxide field-effect transistors (MOSFETs) in the time to come. They have considerable characteristics such as low power consumption and high switching speed. Full adder cell is the main part of the most digital systems as it is building block of subtracter, multiplier, compressor, and other larger circuits. Therefore, it has a direct impact on the overall performance of the entire digital system. In this paper, we have presented two novel full adder cells using both capacitive threshold logic (CTL) and path transistor logic (PTL). The proposed cells have two symmetrical and identical modules to provide Sum and output carry (Cout). Intensive simulations using Synopsys HSPICE tool are run to evaluate the performance metrics of the proposed cells against some state-of-the-art full adders. Simulations are carried out in the presence of varying power supplies, temperatures, and output loads. Moreover, since process variations are a concern at the manufacturing stage of integrated circuits, we have performed Monte Carlo transient analysis to study the robustness of the proposed cells against diameter variations of carbon nanotubes (CNTs). Simulation results demonstrate that the proposed cells outperform their counterparts and exhibit reasonable results.

***doi**: 10.5829/idosi.ije.2015.28.10a.07*

1. INTRODUCTION

Among various digital cells, the 1-bit full adder cell is of interest of many circuit designers due to its extensive usage in the larger circuits. In fact, it is building block of other circuits such as subtracter, multiplier [1], compressor, and so on [2]. These circuits are also used in arithmetic logic unit (ALU) of different processors such as application specific instruction set processor (ASIP) [3], digital signal processor (DSP) [4-6], and general purpose processor (GPP). From above, it is clear that 1-bit full adder cell has a great influence on overall performance of a digital system.

Today power consumption has become a major concern in portable electronic systems such as personal digital assistants (PDAs), mobile communication devices, laptops and so many others. Since they have a battery with limiting life time, low power circuits will cause more operation by saving power. On the other hand, increasing in the complexity of algorithms implies to have circuits with higher speed. Therefore, it is of interest to design low-power and high-speed circuits. One way to reach this goal is that we shrink transistor sizes further. In 1965, G. Moore predicted that the number of transistors on an integrated circuit doubles about each 18 months. This prediction is known as Moore's law which has been continued until now [7]. Further shrinking of transistors into below than 65nm causes important issues for metal oxide filed-effect transistors (MOSFETs) [8]. At nanoscale regime MOSFETs encounter essential problems such as decreased gate control, increased leakage current, and large parametric variations which limits further scaling of them. Thereby, some new devices have been

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Please cite this article as: M. H.Shafiabadi, Y.SafaeiMehrabani, Symmetrical, Low-Power, and High-Speed 1-Bit Full Adder Cells Using 32nm Carbon Nanotube Field-effect Transistors Technology, International Journal of Engineering (IJE), TRANSACTIONS A: Basics Vol. 28, No. 10, (October 2015) 1447-1454

presented in recent years to replace conventional MOSFETs.

The carbon nanotube field-effect transistor (CNFET) is one of those new technologies. It has remarkable characteristics, i.e., high speed switching operation and low power consumption compared to silicon bulk transistors. They have similar current-voltage (I-V) characteristics to MOSFETs [9], and are promising candidate to replace them in the future. A CNFET transistor uses some carbon nanotubes (CNTs) in its structure to bridge source and drain contacts. It is worth to note that CNTs were discovered by S. Iijima [10]. By rolling up a graphite sheet, carbon tube is realized. According to arrangement angle of carbon atoms along the tube, CNT is either metallic or semiconducting. There is an integer pair (n1, n2) referred to as chirality vector and determines whether a CNT is metallic or semiconducting. Equation (1) shows how the diameter of a CNT can be achieved from chirality vector [11].

$$D_{CNT} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (1)$$

Using (1) we can obtain threshold voltage of a CNFET as follows.

$$V_{th} = \frac{0.43}{D_{CNT}(nm)} \quad (2)$$

It is worth to note that Equation (2) gives absolute value of threshold. Therefore, positive and negative values are used for n-type CNFETs (NCNFETs) and p-type CNFETs (PCNFETs), respectively. Figure 1 shows the structure of a CNFET transistor [12]. Similar to MOSFETs it contains four terminals called gate, source, drain, and substrate.

The reminder of this paper is structured as follows. In section 2 some state-of-the-art full adder cells from literature are reviewed. In section 3 the proposed full adders are presented in detail. Section 4 provides simulation results and discussions. In this section comprehensive simulations are performed to closely study figure of merit of each full adder cell. Finally, section 5 concludes the paper.

2. REVIEW OF PREVIOUS FULL ADDERS

In this section, we briefly review pros and cons of different full adder designs. Since the proposed cells are based on capacitive threshold logic (CTL) we have chosen some designs which employ CTL.

Figure 2 illustrates the design of Design 2 full adder [13]. The main advantage of the Design 2 cell is that it uses the small number of transistors, i.e., only eight transistors. Moreover, it contains seven capacitors. Capacitors form a network to realize voltage division based on superposition theorem for each combination of inputs. Then, using inverter gates, Majority-not function is realized. This method reduces the number of transistors remarkably. Now, to realize output carry (Cout) it is needed only a conventional inverter. On the other hand, to produce complement of Sum signal two times of values of Majority-not output plus voltage division of inputs is utilized. Finally, using an inverter gate the Sum signal is produced. However, the Design 2 consists of small number of transistors, but it is susceptible to noise because of utilizing capacitor at the internal node.

Figure 3 illustrates the design of 3C2C full adder [14]. The same as the Design 2 it uses eight transistors but the number of capacitors has been reduced to five capacitors. The 3C2C utilizes the same scenario to produce Sum and Cout outputs and only the number of capacitors is less than the Design 2. In fact, it is the enhanced version of the Design 2 full adder.

Figure 4 illustrates the design of Minority function bridge style full adder (MBFA) [15]. It compromises 16 CNFETS and a 3-input capacitor network. The maximum critical path consists of five transistors which makes a long propagation delay. The presence of inverters in the last stage of the circuit enhances the driving capability.

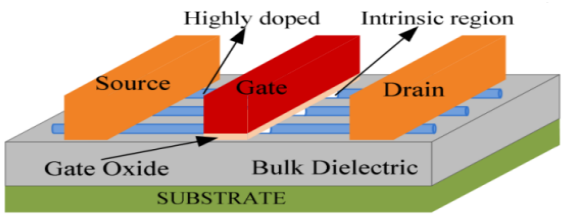

Figure 1. The structure of a CNFET transistor [12]

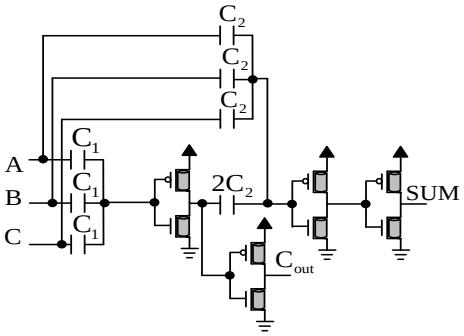

Figure 2. The design of Design 2 full adder

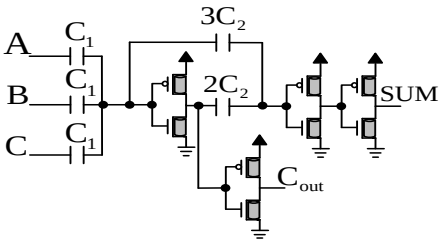

Figure 3. The design of 3C2C full adder

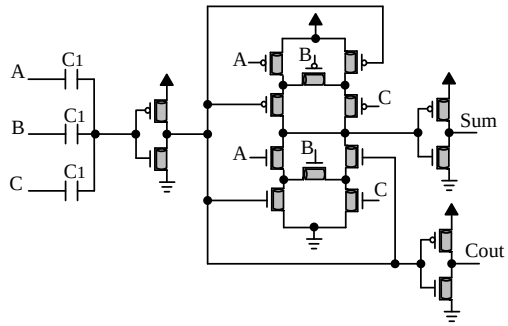

Figure 4. The design of MBFA full adder

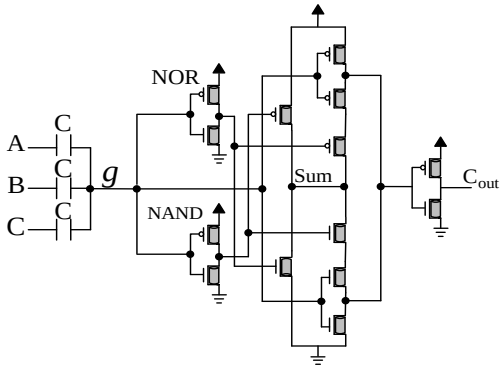

Figure 5. The design of FA1 full adder

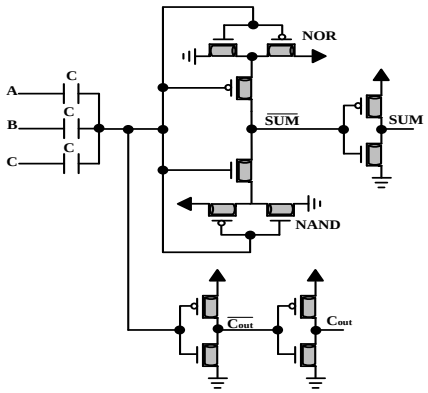

Figure 6. The design of FA2 full adder

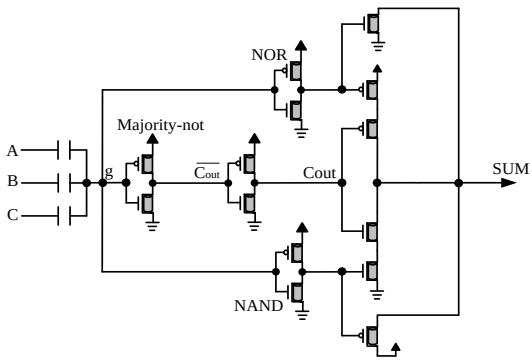

Figure 7. The design of SyMuT full adder

Figure 5 illustrates the design of FA1 full adder [16]. The FA1 contains 14 transistors and a 3-input capacitor network. Employing two inverters, the NAND and NOR functions are produced. Then using them and voltage of capacitor network Sum output is realized. The main concern for the FA1 is that it has static power consumption. In fact when the summation of inputs are 1 or 2 (Σin= 1, 2) then transistors that produce Sum signal are not completely off and cause current flow from power supply to the ground. The other drawback is that Sum output has not enough driving power in the presence of large fanouts. Figure 6 illustrates the design of FA2 full adder [17]. In FA2 all transistors are controlled by means of voltage of capacitor network. This improves the speed of adder. The FA2 comprises 12 transistors which three of them are placed along the critical path. Existing of inverters at the output nodes increases the driving power capability.

Figure 7 illustrates the design of SyMuT full adder [18]. It has fully symmetric structure which makes the layout design easier. In this design first Cout signal is produced. Then, using it, Sum is produced. The SyMuT contains 14 transistors and has rail-to-rail outputs. It has critical path with three transistors.

3. THE PROPOSED FULL ADDER

Two novel designs are presented for 1-bit full adder cell in this section. These designs are based on both capacitive threshold logic (CTL) and pass transistor logic (PTL) and have fully symmetric structures for Sum and Cout signals. The first design has not driving power whereas the second one advantages it at the expense of more transistors. The first design is called fully symmetric full adder (FSFA1) and the second one is called FSFA2.

3. 1. The First Design (FSFA1) The FSFA1 uses 2-input NAND and NOR functions to multiplex different paths to provide the desired outputs. Equations (3) and (4) show the Boolean functions for the proposed cell.

$$Sum = (\bar{B}.\bar{C} + B.C).A + (\bar{B}.C + B.\bar{C}).\bar{A} \quad (3)$$

$$Cout = B.C + (\bar{B}.C + B.\bar{C}).A \quad (4)$$

Table 1 shows how the output signals are produced using input signals.

In order to produce NAND and NOR functions we use CTL. This technique reduces the number of transistors. Figure 8 shows the corresponding circuit. For instance, in order to have a NAND function it is enough to set the absolute value of threshold voltage of PCNFET such that to be less than the threshold voltage of NCNFET. As mentioned in (1) and (2), it can be done by altering the chirality values of CNTs. In this

case, PCNFET will be on even if the summation of input signals B and C are logic 0, 1. Then, output will reach to power supply. Only in the case that both inputs are logic 1, then PCNFET will become off and vice versa NCNFET switches on. Therefore, output will be pulled down to ground.

TABLE 1. Truth table of full adder

B	C	NAND	NOR	Sum	Cout
0	0	1	1	A	0
0	1	1	0	$\overline{A}$	A
1	0	1	0	$\overline{A}$	A
1	1	0	0	A	1

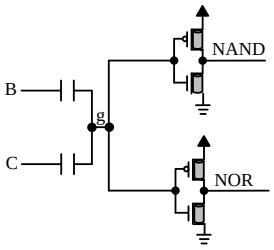

Figure 8. NAND/NOR functions

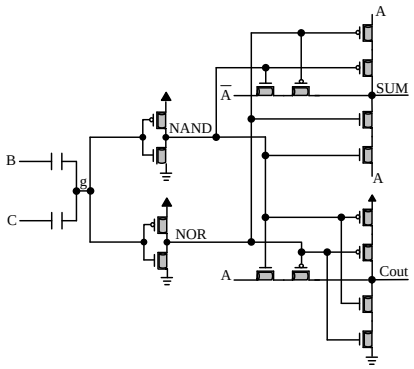

Figure 9. The structure of FSFA1

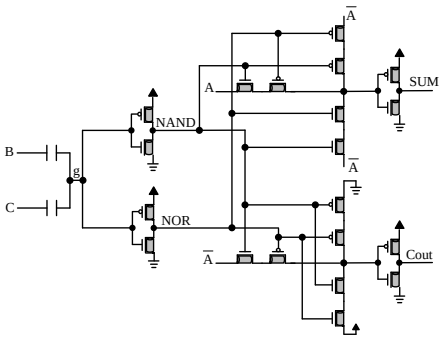

Figure 10. The structure of FSFA2

After producing NAND and NOR functions they are utilized to control pass transistors to produce the desired outputs. The structure of FSFA1 is shown in Figure 9. It consists of 18 transistors and a 2-input capacitor network. The maximum critical path of FSFA1 consists of three CNFETs. Considering Figure 9, it is clear that there are two identical modules for Sum and Cout outputs. Pass transistors cause threshold loss problem. To mitigate this problem we have set the diameters of CNTs such that a small threshold voltage is realized for them. This is one advantage of CNFET technology in which we can alter the threshold voltage of transistors easily.

3. 2. The Second Design (FSFA2) One drawback for FSFA1 is that it has not driving power. Moreover, because of threshold loss problem the final outputs are not full swing. Therefore, to resolve these issues another design called FSFA2 is presented in this subsection. The main idea behind the FSFA2 is the same as one existence in FSFA1. By subtly changing of input signals and add two more inverters at the output nodes we obtain the second design. The FSFA2 not only has rail-to-rail outputs but also has driving power. Therefore, it can be used in large circuits. Figure 10 illustrates the structure of FSFA2. The FSFA2 contains 22 transistors and its maximum critical path has three transistors.

4. SIMULATION RESULTS AND DISCUSSIONS

In this section, we report simulation results and provide discussions. First, the simulation environment is proposed in a separate subsection. Then, simulation results are reported in another subsection.

4. 1. Simulation Setup The Synopsys HSPICE tool is used to run simulations. The 32nm technology node model is used to simulate circuits [19, 20]. This model was developed for MOSFET-like CNFETs which can have one or more CNTs in their channel. It includes nonidealities such as source/drain resistance and capacitance, Schottky barrier effects, CNT charge screening effects, and so on.

The 56 transitions from an input combination to another one are fed to the cells. The combinations that do not change outputs are not considered. For each combination, the delay is measured from the moment that the input signal reaches 50% of its value to the moment that the output signal reaches the same level. Then, the maximum delay is considered as the delay of the circuit. The power consumption is measured during a long time. It is average power consumption that is reported by HSPICE. Since power and delay are two contrary metrics, we take account a quantitative metric called power delay product (PDP). The PDP compromises between power and delay. The algorithm

proposed in [21] is employed to obtain the minimum PDP for each full adder cell. We use standard fanout of four inverters (FO_4) to measure figure of merit for each full adder. Moreover, input buffers are used to simulate realistic inputs. Buffers are constructed by cascading two inverter gates.

4. 2. Simulation Results In the first simulation, we have studied robustness of circuits against power supply scaling. Performances of circuits are considered in a vast range of power supplies ranged from 0.85V to 1V. The operating frequency and temperature are set to be 100MHz and 27°C, respectively. The simulation results are tabulated in Table 2. Bold-faced numbers show the best results. This table depicts that the performance metrics of FSFA2 is better than FSFA1. For instance, in 0.9V supply, its delay, power consumption and PDP is better than FSFA1 by about 21, 35, and 49%, respectively. This reduction in power consumption is due to rail-to-rail outputs for FSFA2. Therefore, fanout inverters will switch fast and short circuit current will be decreased. Moreover, since there is full swing outputs, transistors existing in the fanout inverters will be quite off or on. Therefore, static power consumption is removed. Table 2 demonstrates that the proposed cells scale well with power supply variations and outperform the other cells in terms of delay, power consumption and PDP metrics. It is worth to note that 3C2C and Design 2 cells have the worst PDP values.

In the second simulation, temperature noise is taken into account. In this simulation, we study the susceptibility of different full adders against ambient temperatures. All circuits are simulated at 0.9V supply, 100MHz operating frequency and fanout of FO_4. Temperatures are changed from 0 to 70°C. Simulation results are shown in Figure 11. Figure 11 demonstrates that the FSFA2 and the FSFA1 have the lowest energy consumption, respectively, compared to other cells. Among different cells, 3C2C, FA1, and Design 2 have the highest PDP, respectively.

Full adder cell often is used in larger circuits with larger fanouts. In this experiment, we study the driving power of different cells against varying output loads. Simulations are performed at 0.9V power supply, 100MHz frequency, 27°C and output loads from 2fF to 10fF. Results are shown in Figure 12. It is clear from Figure 12, when the output load increases the PDP of FSFA2 and MBFA cells are gradually increased while the PDP of 3C2C, Design 2, FA1, and FA2 are sharply increased. Therefore, the proposed cell (FSFA2) can be effectively used in larger structures.

Process variation is one of the concerns of CNFET technology. Inaccurate manufacturing process produces CNTs with different diameters. Therefore, the threshold voltage of each CNFET will be different from the other ones, and might negatively affect the performance of the circuit or cause a malfunction.

TABLE 2. Performance metrics of full adders against varying power supplies

Vdd (V)		0.85	0.9	1
Delay (pS)	Design 2	66.162	68.699	70.744
	3C2C	116.98	122.27	475.46
	FA1	89.471	80.539	75.489
	FA2	54.150	49.523	44.053
	SyMuT	33.120	44.796	41.391
	MBFA	42.729	40.400	37.492
	FSFA1	30.835	29.484	27.024
	FSFA2	**25.480**	**23.066**	**19.675**
Power (µW)	Design 2	0.82320	1.22690	2.66980
	3C2C	1.11620	1.55630	3.41320
	FA1	1.02820	1.14550	1.49470
	FA2	0.57609	0.81418	1.68550
	SyMuT	0.45429	0.66322	1.24140
	MBFA	0.34140	0.40375	0.59918
	FSFA1	0.34950	0.42040	0.72254
	FSFA2	**0.22770**	**0.26953**	**0.43058**
PDP (fJ)	Design 2	0.05446	0.08428	0.18887
	3C2C	0.13057	0.19028	1.62290
	FA1	0.09199	0.09225	0.11283
	FA2	0.03119	0.04032	0.07425
	SyMuT	0.01504	0.02970	0.05138
	MBFA	0.01458	0.01631	0.02246
	FSFA1	0.01077	0.01239	0.01952
	FSFA2	**0.00580**	**0.00621**	**0.00847**

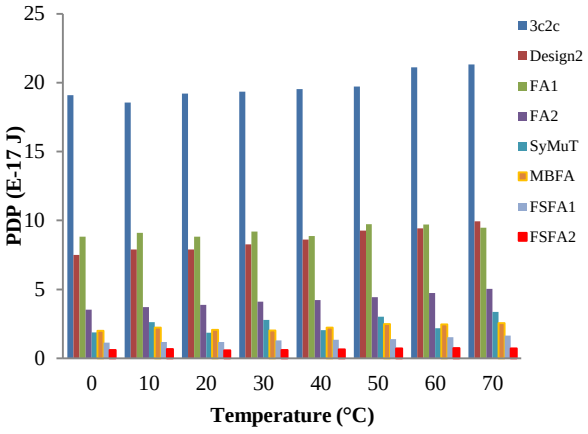

Figure 11. PDP against varying temperatures

In this simulation, we study the robustness of the proposed cells against process variation. A Monte Carlo transient analysis is performed. A credible number of 30 iterations are performed for each diameter deviation. Diameter deviations from the mean value are in the range of 0.08nm to 0.2nm [22]. The distribution of the diameters of CNTs is supposed to be Gaussian with 6-sigma distribution [23]. Table 3 tabulates the maximum power, delay, and PDP variations for FSFA1 and FSFA2 cells. Table 3 depicts that both FSFA1 and FSFA2 function well in presence of diameter variations of CNTs. It is worth to note that FSFA2 is more robust than FSFA1.

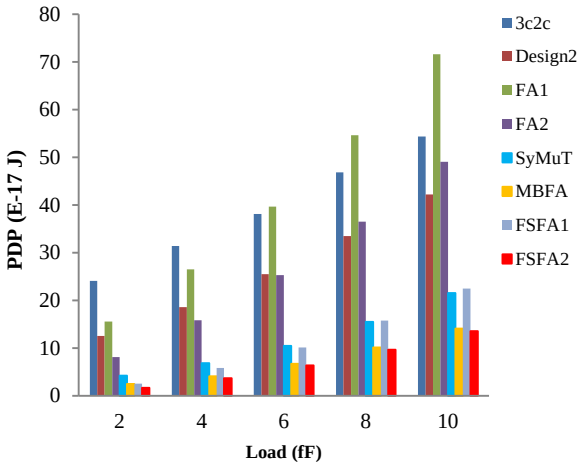

Figure 12. PDP against output load

TABLE 3. Performance variations against diameter variations

Design	Diameter Deviation (nm)	0.08	0.12	0.16	0.2
FSFA1	Delay variation (E-11 S)	9.550	0.307	0.445	0.584
	Power variation (E-7 W)	0.467	0.773	1.194	1.747
	PDP variation (E-18 J)	16.33	3.58	5.490	7.874
FSFA2	Delay variation (E-11 S)	0.378	0.671	4.210	4.099
	Power variation (E-7 W)	0.274	0.439	1.855	2.150
	PDP variation (E-18 J)	0.724	1.228	5.886	6.915

TABLE 4. Performance results of 4-bit ripple carry adder

V_{DD}	0.65		
	Power (*E-6 W)	**Delay (*E-12 S)**	**PDP (*E-17 J)**
3C2C	Fail	Fail	Fail
Design 2	1.5865	431.89	68.520
FA1	0.6558	2264.3	148.50
FA2	0.6963	429.53	29.909
SyMuT	0.59161	211.20	12.495
MBFA	0.40681	1198.7	48.765
FSFA1	0.18891	257.63	4.8669
FSFA2	0.15517	132.35	2.0536

To study the performance of full adders in a real test bed, we use a 4-bit ripple carry adder (RCA). The delay is calculated from the moment that inputs are fed to the first stage full adder until the moment that desired signals are loaded from the forth stage full adder cell. To have realistic input signals we use two casceded inverter gates (buffers) and we also apply buffers at the output nodes. Simulation results are tabulated in Table 4. Simulation results confirm that both the proposed designs are more efficient than other cells. For instance, the FSFA2 consumes less PDP about 97, 98, 93, 83, 95, and 57% compared to Design 2, FA1, FA2, SyMuT, MBFA, and FSFA1, respectively. Note that the 3C2C fails to function in an RCA, since it is so sensitive to voltage levels at internal nodes. The FSFA2 has the least power consumption due to using pass transistor logic. In conclusion, the proposed cell is very suitable to be employed in large arithmetic structures.

5. CONCLUSION

Two novel full adder cells using both capacitive threshold logic (CTL) and pass transistor logic (PTL) were presented in this paper. They use two symmetrical modules in their structure to produce Sum and Cout signals. The first design had 18 transistors and a 2-input capacitor network. Capacitor network was responsible for realizing 2-input NAND and NOR functions. Then, they were applied to control transistors to generate the desired outputs for Sum and Cout. One drawback of the first design was that it had not rail-to-rail output signals. Therefore, by changing the inputs of transistors and adding two inverter gates the second design was presented. It had 22 transistors and its outputs were full swing.

Synopsys HSPICE tool was used to simulate the circuits. All designs simulated in 32nm CNFET technology. Intensive simulations in presence of power supply scaling, temperature noise, and output load were

performed. Simulation results confirmed that both of proposed designs had better performance compared to other ones. We observed that both of proposed full adders were low-power, high-speed, and low-energy. Finally, a Monte Carlo transient analysis was run to evaluate the susceptibility of the proposed cells against the diameter variations of carbon nanotubes. Simulation results demonstrated that the proposed cells can function well against process variation.

6. ACKNOWLEDGEMENT

The authors gratefully acknowledge the financial and other support of this research namely “Design of Full Adder Cell with Low Energy Consumption in Carbon Nanotube Technology,” provided by the Islamic Azad University, Islamshahr Branch, Islamshahr, Iran.

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Symmetrical, Low-Power, and High-Speed 1-Bit Full Adder Cells Using 32nm Carbon Nanotube Field-effect Transistors Technology

TECHNICAL NOTE

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P A P E R I N F O

Paper history:
Received 19 August 2015
Received in revised form 06 October 2015
Accepted 16 October 2015

Keywords:
Nanoelectronic
Carbon Nanotube Field-Effect Transistors
Full Adder
Capacitive Threshold Logic
Path Transistor Logic
Low-power
High-speed

چکیده

ترانزیستورهای اثر میدان نانو لوله کربنی (CNFETs) احتمال زیادی دارند تا در آینده جایگزین ترانزیستورهای کلاسیک اثر میدان فلز اکسید (MOSFETs) شوند. آنها دارای مشخصات قابل توجهی همچون مصرف توان پایین و سرعت سوئیچینگ بالا می باشند. سلول تمام جمع کننده از آنجایی که هسته تفریق کننده، ضرب کننده، فشرده کننده و سایر مدارهای بزرگتر می باشد مهمترین بخش اغلب سیستم های دیجیتال می باشد. بنابراین تاثیر مستقیم بر روی کارایی کل سیستم دیجیتال دارد. در این مقاله، با استفاده از منطق آستانه خازنی (CTL) و منطق ترانزیستور عبور (PTL) دو عدد سلول تمام جمع کننده نوین ارائه شده است. سلول های ارائه شده دارای دو عدد ماژول یکسان و متقارن برای تولید سیگنال مجموع و رقم نقلی (Cout) می باشند. با استفاده از ابزار Synopsys HSPICE شبیه سازی های جامعی به منظور ارزیابی پارامترهای سلول های ارائه شده در برابر برخی از روش های نوین انجام شده است. شبیه سازی ها در حضور منبع تغذیه متغیر، دما، و بار خروجی انجام شده اند. علاوه بر این، از آنجایی که تغییرات فرآیند ساخت در مرحله تولید جزو نگرانی های اصلی می باشد، به منظور بررسی مقاومت سلول های ارائه شده در برابر تغییرات قطر نانو لوله های کربنی (CNTs) از تحلیل مونتو کارلو استفاده شده است. نتایج شبیه سازی تصدیق می نمایند که سلول های ارائه شده نسبت به رقیبان خود پیشی گرفته و نتایج منطقی را نشان می دهند.

***doi**: 10.5829/idosi.ije.2015.28.10a.07*