International Journal of Engineering

Journal Homepage: www.ije.ir

Digital Controller Design based on Time Domain for DC-DC Buck Converter

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PAPER INFO

Paper history:
Received 27 February 2014
Received in revised form 09 March 2015
Accepted 04 April 2015

Keywords:
DC-DC Buck Converter
Digital PID Controller
Integral Square Error (ISE)
Patterning
State-space Averaged (SSA)
Voltage Mode Control

ABSTRACT

In this paper, the digital controller design for compensating the dc-dc buck converter output voltage has been analyzed in the digital domain. The main idea of this paper is patterning the samples of high order ideal controller and using integral square error in determining digital PID coefficients. This approach provides higher precision of digital controller design and eliminates the need for manipulating the coefficients, which in turn will lead to stringent design parameters in response to the system output. The proposed scheme has been simulated in MATLAB software and the results have been presented. The digital controller has been designed based on the proposed method for the buck converter and has been implemented on a TMS320LF2812 DSP core.

doi: *10.5829/idosi.ije.2015.28.05b.07*

1. INTRODUCTION

In recent years, DC–DC converters with step-up/step-down characteristics have been widely used in applications such as portable devices [1-4], communication power supply [5, 6], power factor correction [7-11], hybrid electrical vehicles or fuel-cell vehicles [12, 13].

The design of DC–DC converter controllers has experienced considerable changes during the recent decades. Considering many advantages offered by digital control over the analog control, abundant attention has been devoted to the digital control [14]. These advantages include stable functioning, flexibility and capability in implementation of complex control algorithms. There exist numerous methods for controller design in digital control, e.g. designing the controller in frequency domain and thereafter transferring it to the digital domain [15, 16].

PID controllers are one of the most widely used controllers in the industry [17], to the extent that they are used in more than 90% of modern industrial processes. The reason for this popularity lies in the simplicity, versatility, speed, reliability and flexibility which this controller offers. A variety of methods and formulae have been introduced so far for adjustment of the PID controller, the most important of which to mention include the Ziegler and Nichols [18] and Cohen and Coon [19] methods. In 1991 new settings were introduced for the Ziegler and Nichols method [20]. The method was based on particle swarm optimization (PSO) algorithm [21]. The Internal Model Control designing method and Integral of Time Absolute Value minimization method [22] have also been introduced for regulating the controller. In most of the introduced methods for maximum yield, the optimized value is reached after designing the controller coefficients and mathematical manipulation [23].

The main idea of this paper is patterning the samples of high order ideal controller and using integral square error in determining digital PID coefficients. Accurate designing of digital controller and no requirement for mathematical manipulation are from the privileges of the proposed method, resulting in careful fulfillment of the design parameters in system output response.

In this paper, initially a sample buck converter has been considered and the small signal transfer function in

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Please cite this article as:M. A. Javadi Rad, A. Taheri, Digital Controller Design based on Time Domain for DC-DC Buck Converter, International Journal of Engineering (IJE), TRANSACTIONS B: Applications Vol. 28, No. 5, (May 2015) 693-700

the frequency domain has been obtained using the State-Space Averaged model. In the next stage, the open-loop response of the converter in the digital domain has been determined with the aid of one of the S-Z domain transformations. Afterwards, considering the design parameters and using Truxal rules [24] and one of the S-Z domain transformations, the ideal closed-loop response was specified in the digital domain. Considering the open and closed-loop response of the system, the high order ideal digital controller was designed. Then by patterning the ideal controller behavior and minimization of integral square error, the digital PID controller parameters are designed. Finally the buck converter was simulated in MATLAB software considering the load changes and compensated for the purpose of regulating the output voltage. The simulation and implementation output results confirmed the efficiency of the proposed method.

The paper structure is as follows: use of the State-Space Averaged model, determination of small signal transfer function of the converter and the proposed method for digital controller design have been presented in the section 2; in section 3, a digital controller will be designed for a DC-DC buck converter based on the introduced method. The performance comparison of the controllers designed for DC-DC converter are made in section 4. Section 5 includes the implementation results. Finally, the conclusion will be given in section 6.

2. DIGITAL CONTROLLER DESIGN SCHEME

2. 1. State-space Averaged Model for DC-DC Buck Converter Figure 1 illustrates the circuit structure of a buck converter.

The small signal transfer function of the buck converter is obtained through different methods [25, 26]. To achieve this goal, the State-Space Averaged technique has been used:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)}=\frac{V_g(1+sR_CC)}{1+s\left(R_CC+\left[R\|R_L\right]C+\frac{L}{R+R_L}\right)+s^2LC\left(\frac{R+R_C}{R+R_L}\right)} \quad (1)$$

In this equation, $\hat{v}_o$ and $\hat{d}$ are the small variations of the output voltage and duty cycle, respectively.

2. 2. Proposed Method for Digital Controller Design The proposed method in this paper is based on patterning of the samples of high order ideal controller and using integral square error in determining digital PID coefficients. This approach provides increased accuracy in designing of digital controller and no requirement for manipulation of coefficients leading to careful fulfillment of the design parameters in system output response. At first, considering the design parameters including the maximum overshoot and settling time values, the denominator coefficients of ideal closed-loop response in frequency domain are obtained. In a general sense, the standard form of a second-order system can be described using the relationship (2):

$$F_s=\frac{{\omega_n}^2}{s^2+2\zeta\omega_n+{\omega_n}^2} \quad (2)$$

It is important to note that the F_s numerator is not necessarily equal to ${\omega_n}^2$. In this relationship, ω_n is the angular frequency and ζ is the damping ratio. Considering the design values t_s (settling time) and M_P (maximum overshoot) and their relationship with ζ and ω_n, the denominator F_s can be determined.The relationships between t_s and M_P with ζ and ω_n have been presented below:

$$M_P=e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}} \quad (3)$$

$$t_s=\frac{4}{\zeta\omega_n} \quad (4)$$

Using these two relationships and the known amounts t_s and M_P the ζ and ω_n values are obtained. After determining the denominator of the relationship (2), the equation is transferred to the digital domain with the help of one of the S-Z transformations (e.g. zero order hold) and the denominator of closed-loop response is determined in the digital domain. Then it is normalized using the greatest exponent coefficient [27]:

$$den_F=d_0z^2+d_1z+d_2 \quad (5)$$

$$DEN_F=z^2+D_1z+D_2 \quad (6)$$

$$D_1=\frac{d_1}{d_0}\ D_2=\frac{d_2}{d_0} \quad (7)$$

The closed-loop form of the transfer function in the digital domain is as follows. It should be noted that the numerator order should not be greater than the denominator order.

$$A_{CL}(z)=\frac{N_0z^2+N_1z+N_2}{z^2+D_1z+D_2} \quad (8)$$

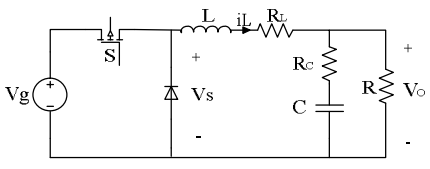

Figure 1. DC-DC buck converter

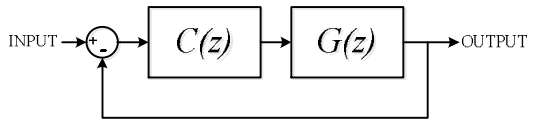

Figure 2. Basic block diagram of a feedback system.

The N_0 , N_1 and N_2 coefficients are obtained considering the Truxal rule set. The mentioned rule set is as follows:

$$A_{CL}(z)|_{z=\infty} = 0 \tag{9}$$

$$A_{CL}(z)|_{z=1} = 1 \tag{10}$$

$$\frac{dA_{CL}(z)}{dz}|_{z=1} = \frac{1}{K_V} \tag{11}$$

In the next step, the open-loop response of the system shown in section 2.1 is transferred from the S domain to the digital domain. Using one of the S to Z transformations, the open-loop response of the system in the digital domain is also determined. Considering the block diagram of a feedback system (Figure 2) the output-input relationships are defined as follows:

$$A_{CL}(z) = \frac{G(z)C(z)}{1+G(z)C(z)} \tag{12}$$

The $C(z)$ block is the controller of the system which is determined using Equation (13) as follows.

$$C_{ideal}(z) = \frac{A_{CL}(z)}{(1-A_{CL}(z))G(z)} \tag{13}$$

Using this relationship, the ideal digital controller for the digital domain is designed. The high number of zeros and the pole $C_{ideal}(z)$ could cause the implementation of the controller costly and time consuming.To remove this problem, a controller with lower order compared with $C_{ideal}(z)$ and a behavior similar to $C_{ideal}(z)$ should be designed. The PID analog format in general state is expressed using the formula (14):

$$s_c(t) = K_P s_e(t) + K_I \int s_e(t)dt + \frac{K_D ds_e(t)}{dt} \tag{14}$$

There have been various kinds of methods to nail to discrete PID model like backward difference, forward difference, bilinear transformation, impulse-invariance, step invariance and matched pole-zero. The discrete form of PID through backward difference method is:

$$C_{design}(z) = \frac{S_c(z)}{S_e(z)} = K_P + \frac{K_I T_S z}{z-1} + \frac{K_D(z-1)}{T_S z} \tag{15}$$

After transferring of Equation (15) to the digital domain and generalization, the following relationships are resulted:

$$S_c[n+1] = S_c[n] + \left(K_P + K_I T_S + \frac{K_D}{T_S}\right) S_e[n] + \left(-K_P - \frac{2K_D}{T_S}\right) S_e[n-1] + \frac{K_D}{T_S} S_e[n-2] \tag{16}$$

$$b_1 = \left(K_P + K_I T_S + \frac{K_D}{T_S}\right) \; b_2 = \left(-K_P - \frac{2K_D}{T_S}\right) \; b_3 = \left(\frac{K_D}{T_S}\right) \tag{17}$$

S_c is considered as the ideal controller step response and S_e is regarded as the step input. By entering different values into the equation for different times, the unknown coefficients b_1 , b_2 , b_3 can be obtained. If b_1 , b_2 , b_3 coefficients are determined considering the ideal controller behavior, a good approximation of the ideal controller will be achieved. For gaining the b_1 and b_2 values, the first two ideal controller step response are used. The complementary idea of this method is that in order to determine b_3 there is a sample in the ideal controller response that causes the controller coefficients to be designed fully optimized. To identify this sample, the minimum integral error value (18) has been used. The error between the output ideal step response and the controlled output step response is considered as the signal error.

$$error[n] = S_{ACL}[n] - S_{ACL_d}[n]$$
$$error(t) = error[nT_S] \; ISE = \int_0^\infty e^2(t)dt \tag{18}$$

For identifying the desired sample, a search space of the ideal controller step has been considered. To limit the search space, only the *m* of the first sample is used. Numerous experiments proved that *m* is the sample for which the ideal closed-loop response has maximum overshoot. Considering the samples after *m* can cause intensive fluctuation of the closed-loop response.

$$n = 0 \;\; S_c[1] = b_1 \tag{19}$$

$$n = 1 \;\; S_c[2] = S_c[1] + b_1 + b_2 \tag{20}$$

$$2 \le n \le m \;\; S_c[n+1] = S_c[n] + b_1 + b_2 + b_3 \tag{21}$$

3. DESIGNING OF A SAMPLE CONTROLLER IN DIGITAL DOMAIN

The DC-DC buck converter parameters' values have been given in Table 1.

TABLE 1. System parameter values

Parameter	Value	Unit
Capacitor, C	376	μF
Inductor, L	4.1	μH
Load resistor, R	1	Ω
ESR of capacitor, R_C	5	mΩ
ESR of inductor, R_L	80	mΩ
DC input voltage	12	volt
Switching frequencies, f_S	150	kHz
Settling time,t_s	500	μsec
Maximum overshoot,M_P	20	%
Rise time,t_R	50	μsec

Using the State-Space Averaged model, the open-loop response of the buck converter small signal is shown in the Relationship (22).

$$G(s)=\frac{20\left(0.3\times10^{-4}s+1\right)}{1.503\times10^{-7}s^2+5.4975\times10^{-5}s+1} \quad (22)$$

Now, with the help of one of the S-Z transformations, the open-loop response of the system's small signal is mapped into the digital domain. For this purpose, the ZOH transformation has been used:

$$G(z)=\frac{0.01702\ z-0.01489}{z^2-1.998\ z+0.9985} \quad (23)$$

The value of t_s and M_P have been considered according to Table 1. The closed-loop response is obtained as given below:

$$A_{CL}(z)=\frac{0.5067z-0.4148}{z^2-1.401z+0.4933} \quad (24)$$

Albeit, it should be noted that all the S-Z domain transformations contain errors. Using the system open-loop response and the closed-loop response in Z-domain, the $C_{ideal}(z)$ can be determined with the aid of Relationship (13).

$$C_{ideal}(z)=\frac{0.5067\ z^3-2.133\ z^2+3.572\ z-2.975}{0.1061\ z^3-0.4039\ z^2+0.6076\ z-0.4508} \quad (25)$$

Considering the ideal controller step response (Figure 3) and the Relationships (19) and (20), the PID parameters have been calculated.

Given Section 2. 2 calculation results, the search space for specifying the b_3 value is constructed considering 32 samples (m=32). The maximum overshoot of ideal closed-loop step response has occurred in the sample no. 32. Figure 4 illustrates the integral square errors. The graph holding the lowest area with the time axis is the result of the optimized controller. Here the sample no. 17 has been selected for making the b_3 coefficient.

$$b_1=0.7055\ b_2=-1.3210\ b_3=0.6294 \quad (26)$$

The designed digital controller is therefore resulted as follows:

$$C_{design}(z)=\frac{0.7055-1.3210z^{-1}+0.6294z^{-2}}{1-z^{-1}} \quad (27)$$

Considering Figure 5, it can be observed that response of $C_{ideal}(z)$ and $C_{design}(z)$ steps have values very close to each other. Response of the controlled closed-loop step by the controllers that are different in b_3 value has been presented in the Figure 6.

Figure 7 shows the controlled closed-loop step response by $C_{ideal}(z)$ and $C_{design}(z)$. The design parameters' values in $A_{CL_d}(z)$ are confirmed. As can be seen from above, the closed-loop response obtained from the designed controller is similar to the ideal closed-loop response with good approximation.

4. PERFORMANCE COMPARISON OF VARIOUS METHODES

The performance comparison of the controllers designed for DC-DC converter are made in over shoot, rise time and settling time.

a: Ideal response with ideal controller
b: Internal Mode Control method (IMC)
c: Ziegler and Nicholes method (ZN)
d: Proposed method

In methods b and c, the controller is designed in the frequency domain and then by Bilinear transform is converted to the digital domain. Since all methods of s to z transmission have some error, the error will influence on parameters of designed controller (b and c). In the proposed method, the controller is designed from the outset in the digital domain, so this error is minimized. As can be seen in Figure 8, closest to the ideal closed-loop response is achieved by the proposed method.

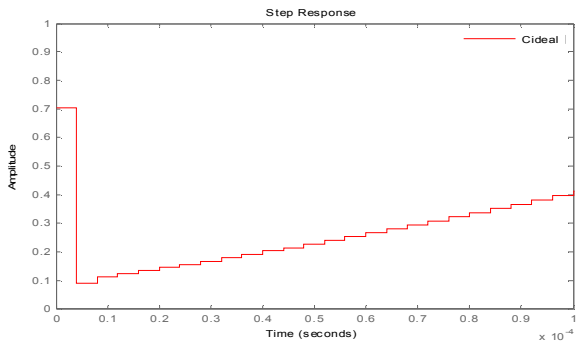

Figure 3. Step response of the buck converter ideal controller.

Table 2 gives the details about the close loop step response of buck converter with different PIDs designed based on b, c and d methods. As seen in Table 2, the design parameters value of the proposed method is much more accurate than the other two methods.

TABLE 2. Closed-loop step responses detail

Method	M_p (%)	t_s (μsec)	t_r (μsec)
Ideal controller	20	500	50
IMC	22	870	67
ZN	5	535	85
Proposed method	20	545	54

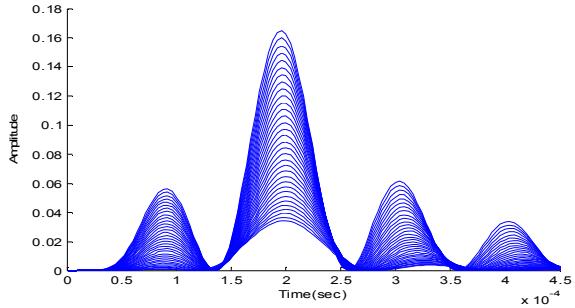

Figure 4. ISE curves between step response of $A_{CL}(z)$ and $A_{CL_d}(z)$.

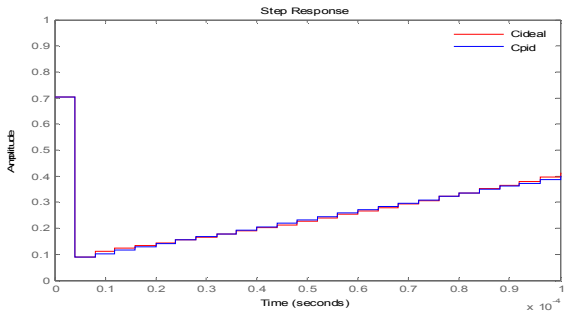

Figure 5. Step response of $C_{ideal}(z)$ and $C_{design}(z)$

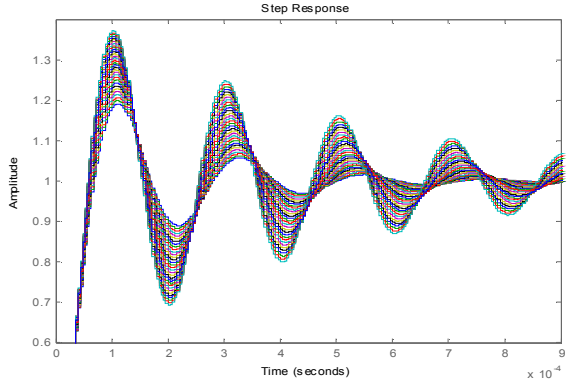

Figure 6. Comparison among step responses of controlled systems for any designed controller.

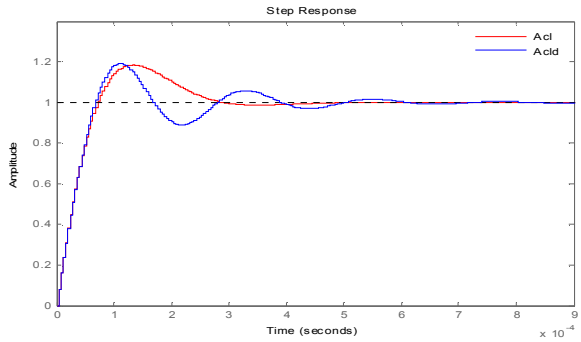

Figure 7. Closed-loop step responses of a system controlled by $C_{ideal}(z)$ and $C_{design}(z)$.

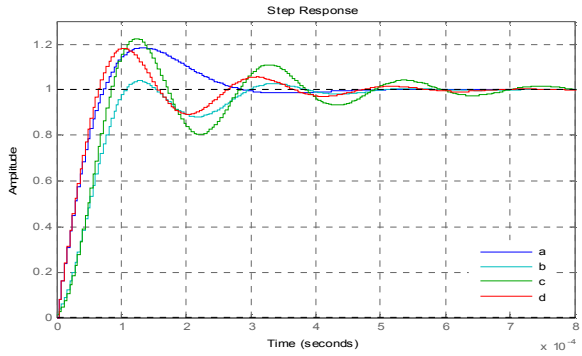

Figure 8. Comparison of closed-loop step response of various methods

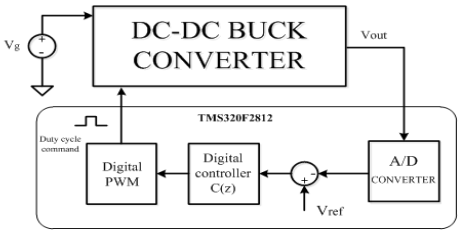

Figure 9. Voltage-mode pulse width modulation control structure.

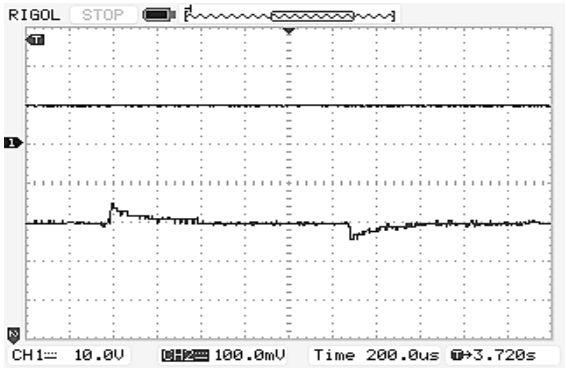

Figure 10. Channel 1: Input voltage (Vg=10volt), Channel 2: output voltage response when the load increased 100% then decreased 50%.

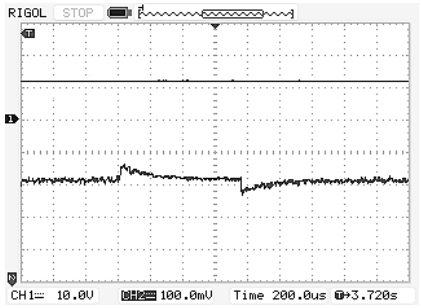

Figure 11. Channel 1: Input voltage (Vg=12volt), Channel 2: output voltage response when the load increased 100% then decreased 50%.

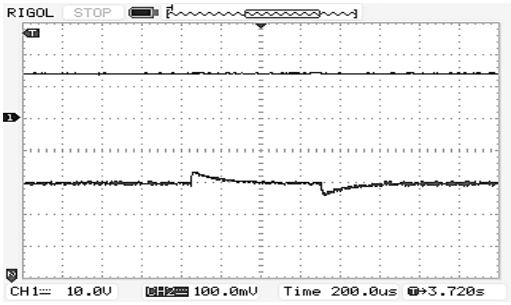

Figure 12. Channel 1: Input voltage (Vg=14volt), Channel 2: output voltage response when the load increased 100% then decreased 50%.

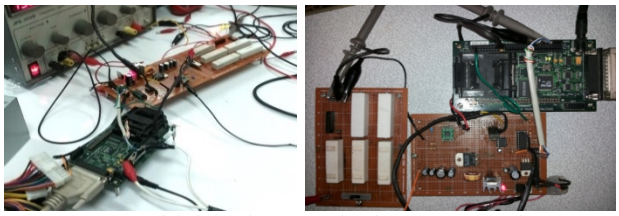

Figure 13. A fabricated DC-DC buck converter and TI C2000 ezdsp F2812.

5. EXPERIMENTAL RESULTS

In this paper, the digital control for DC-DC buck converter in voltage mode has been implemented based on the TMS320F2812 digital signal processor chip while its structure is given in Figure 9.

Procedurally, output voltage of DC-DC buck converter is compared with a reference voltage, and then error signal is produced. Indeed, there is a little time which is wasted between error signal sampling and command signal (DC) updating.The PID controllers have been implemented and evaluated using a Texas Instruments (TI) eZdsp F2812.The eZdsp F2812 is a stand- alone evaluation module with a TMS320F2812 DSP, which is a 32-bit fixed point DSP controller with on-board flash memory.The CPU operates at 150 MHz. The TMS320F2812 supports peripherals used for embedded control applications, such as event manager modules and a dual 12-bit, 16 channels ADC. The conversion period of the A/D is 80 ns.

The buck converter input voltage in Figure 10, 11 and 12 is 10, 12 and 13 volts, respectively (Channel 1). Channel 2 shows the implemented buck converter output voltage in load changes. The load is initially increased by 100% and then is decreased by 50%. The maximum ripple amplitude is equal to 60 mV. Figure 13 represents the implemented buck converter together with the TI ezdsp F2812 chip.

6. CONCLUSION

In this paper, a new method has been introduced for designing of a digital controller for buck DC-DC converter in digital domain. The proposed method determines the digital controller coefficients with high accuracy. The controller coefficients are determined using primary samples of ideal controller step response. It is important to note that in case the primary samples of ideal controller step response entails negative and non-linear slop, i.e. the ideal controller step response includes initially an undershoot, a step will be added to the proposed method. In this step, considering the behavior of the samples having positive slope, the primary samples are approximated with the same positive slope and then the introduced method is used for determining the digital controller coefficients. Because using the samples with negative slope for determining the digital controller coefficients results in instability of the closed-loop response of the system.

7. ACKNOWLEDGEMENTS

I would like to thank Dr. Asghar Taheri for his most support and encouragement. This research was supported by University of Zanjan.

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Digital Controller Design based on Time Domain for DC-DC Buck Converter

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P A P E R I N F O

Paper history:
Received 27 February 2014
Received in revised form 09 March 2015
Accepted 04 April 2015

Keywords:
DC-DC Buck Converter
Digital PID Controller
Integral Square Error (ISE)
Patterning
State-space Averaged (SSA)
Voltage Mode Control

چکیده

در این مقاله طراحی کنترلر دیجیتال به منظور جبران سازی ولتاژ خروجی مبدل باک در حوزه Z آنالیز گردیده است. ایده اصلی در این مقاله، الگو برداری از نمونه های کنترلر ایده آل مرتبه بالا و استفاده از انتگرال مربع خطا در تعیین ضرایب PID دیجیتال است. این رویکرد، افزایش دقت در طراحی کنترلر دیجیتال و عدم نیاز به دستکاری ضرایب را ارائه می کند که منجر به بر آورده شدن دقیق پارامترهای طراحی در پاسخ خروجی سیستم می شود. طرح پیشنهادی در متلب شبیه سازی شده و نتایج ارائه گردیده است. کنترلر دیجتال بر اساس روش ارائه شده برای مبدل BUCK طراحی گردیده و روی هسته TMS320LF2812 DSP پیاده سازی شده است .

***doi**: 10.5829/idosi.ije.2015.28.05b.07*