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Analysis of Integral Nonlinearity in Radix-4 Pipelined Analog-to-Digital Converters

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ABSTRACT

In this paper, an analytic approach to estimate the nonlinearity of radix-4 pipelined analog-to-digital converters due to the circuit non-idealities is presented. Output voltage of each stage is modeled as sum of the ideal output voltage and non-ideal output voltage (error voltage), in which non-ideal output voltage is created by capacitor mismatch, comparator offset, input offset, and finite gain of amplifier. The integral nonlinearity (INL) can be obtained as the expected value of total input error due to the errors in all stages of radix-4 pipelined ADC.

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1. INTRODUCTION

Depending on architecture of pipelined analog-to-digital, in each stage of ADC, three main error mechanisms can be distinguished: quantization error, noise error, and static and dynamic errors [1-20]. The integral nonlinearity (INL) and differential nonlinearity (DNL) are used as static performance measures. The linearity of the ADC refers to the deviation of its transfer function from the ideal straight-line transfer function. INL and DNL are the error factors that are used to quantify this deviation. Several error sources in the each stage of ADC cause these errors, such as: capacitor mismatch, finite gain of amplifier and offset error. By estimation total input, error can be estimated by INL [1-3]. Several methods have been proposed for calculating INL. Limitations of pipelined ADCs depending on errors in each stage was presented and INL estimated based on expected value of total errors. A general method for system level prediction of INL in pipelined ADC based on random error with Gaussian distribution was presented in literatures [3, 4]. A novel method for stochastic nonlinearity analysis of a pipelined ADC was presented [2] and the INL predicted include linear error. In this paper, we present the method for estimation INL of a N- stage radix-4 pipelined [5-7], ADC architecture. In section II, the INL is defined as the expected value of total error in ADC with Gaussian distribution In section III, a relationship is presented based on output voltage of radix-4 pipeline stage, due to capacitor mismatch, finite gain of amplifier and offset errors. In this model, the output voltage of each stage is sum of the ideal and non-ideal voltages. In section IV, it is shown how different types of errors (capacitor mismatch and finite gain of op-amp) in a stage of radix-4 pipelined ADC affect the static performance of converter.

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2. INL CALCULATION

The Integral Nonlinearity can be obtained as the expected value of $|e_{tot}|$ with Gaussian distribution, where $|e_{tot}|$ is total equivalent input error due to effects of circuit non-idealities in all stages of ADC. Therefore the INL is given by [2, 3]:

$$INL = E\left[|e_{tot}|\right] = \int_{-\infty}^{+\infty} |e_{tot}| . \frac{1}{\sqrt{2\pi\sigma_{tot}^2}} exp\left(\frac{-e_{tot}^2}{2\sigma_{tot}^2}\right) de_{tot} = \sqrt{\frac{2}{\pi}}\sigma_{tot} \quad (1)$$

where, σ_{tot} is standard deviation of e_{tot}.

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3. ERROR MODEL FOR A RADIX-4 PIPELINE STAGE

The main source of nonlinearity errors in pipelined ADCs are capacitor mismatch, comparator offset, op-amp offset, and finite gain of amplifier. There are several design for pipelined ADC. Pipelined ADCs with switched-capacitor implementation, which consist of a cascade of several radix-4 stages have been reported in literatures [5, 6]. In these pipelined ADCs, the input signal is captured by sample and hold. This signal quantized by the sub-ADC, which produces a digital output. Redundant digit set in each stage is of {-3, -2, -1, 0, 1, 2, 3}(6 comparator in each stage) and the digital signal goes to the sub-DAC, which converts it to an analog signal. This analog signal is subtracted from the input signal that is amplified. The multiplying digital-to-analog conversion (MDAC) is performed with gain of 4. A pipelined ADC with a minimum redundant digit set of {-2, -1, 0, 1, 2} is another possible architecture [5]. Figure 1 shows the switched-capacitor of a radix-4 pipeline stage. Although a fully differential switched-capacitor circuit is used, a single-ended circuit is dealt here to simplify the error analysis. The circuit has two clock phases, for normal operation. In the sampling phase, the input is sampled at the bottom plates of all capacitors C_1, C_2, and C_3. The total charge on the bottom plates of the capacitors is:

$$Q_s = (0 - V_{in}) \times (C_1 + C_2 + C_3) \tag{2}$$

where, V_{in} is input voltage of stage. In the next clock phase, (amplification and subtraction) C_1 is connected to the op-amp feedback path, C_2 and C_3 are connected to 0 or $\pm V_{ref}$, depending on the output from sub-ADC. The total charge on the bottom plates of capacitors in this clock phase is:

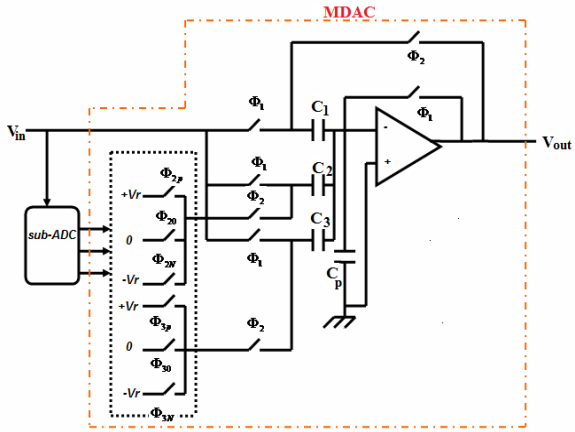

Figure 1. Switched-capacitor of radix-4 pipelined ADC stage

$$\begin{aligned} Q_a = {} & (V^- - V_{out})C_1 + V^- C_p \\ & + (V^- - (D^{(1)} + D^{(3)})V_{ref})C_2 \\ & + (V^- - (D^{(2)} + D^{(3)})V_{ref})C_3 \end{aligned} \tag{3}$$

where, V_{out} is output voltage, C_p is parasitic capacitance, $V^- = -\frac{V_{out}}{A}$ is negative terminal of op-amp and A is amplifier gain. $D^{(1)}$, $D^{(2)}$, and $D^{(3)}$ are:

$$D^{(1)} = \begin{cases} 1, & (1/8)V_{ref} < V_{in} \le (3/8)V_{ref} \\ 0. & otherwise \\ -1, & (-3/8)V_{ref} \le V_{in} < (-1/8)V_{ref} \end{cases}$$

$$D^{(2)} = \begin{cases} 1, & (3/8)V_{ref} \le V_{in} < (5/8)V_{ref} \\ 0. & otherwise \\ -1, & (-5/8)V_{ref} \le V_{in} < (-3/8)V_{ref} \end{cases}$$

$$D^{(3)} = \begin{cases} 1, & (5/8)V_{ref} < V_{in} \le V_{ref} \\ 0. & otherwise \\ -1, & -V_{ref} \le V_{in} < (-5/8)V_{ref} \end{cases}$$

The total charge is conserved and the output signal V_{out} of radix-4 pipeline stage with effect of op-amp offset and parasitic capacitance is given by:

$$\begin{aligned} V_{out} = {} & \frac{1}{C_1 + \frac{C_1 + C_2 + C_3 + C_p}{A}} \\ & \{V_{in}(C_1 + C_2 + C_3) - \{D^{(1)}C_2 + D^{(2)}C_3 \\ & + D^{(3)}(C_2 + C_3)\}V_{ref} + V_{os}(C_1 + C_2 + C_3 + C_p)\} \end{aligned} \tag{4}$$

where, V_{os} is op-amp offset. In the ideal case of $C_p = 0$, $2C_1 = 2C_2 = C_3$, $V_{os} = 0$, and $A \to \infty$, the output voltage is:

$$V_{out} = 4V_{in} - V_{DAC} = 4V_{in} - \underbrace{(D^{(1)} + 2D^{(2)} + 3D^{(3)})}_{D} V_{ref} \tag{5}$$

Therefore, the digital code in radix-4 pipeline stage in the ideal case is $D = D^{(1)} + 2D^{(2)} + 3D^{(3)}$. The ideal output voltage of ith stage is shown in figure. Errors due to the capacitor mismatch are defined as: $\alpha_1 = \frac{C_2}{C_1} - 1, \alpha_2 = \frac{C_3}{C_1} - 2, \alpha_p = \frac{C_p}{C_1}$.

Therefore, the output voltage of ith stage V_{outi} is expressed as:

$$\begin{aligned} V_{outi} = {} & \frac{1}{\left(1 + \frac{4 + \alpha_{1i} + \alpha_{2i} + \alpha_{pi}}{A_i}\right)} \{V_{ini}(4 + \alpha_{1i} + \alpha_{2i}) - \{D_i^{(1)}(1 + \alpha_{1i}) \\ & + D_i^{(2)}(2 + \alpha_{2i}) + D_i^{(3)}(3 + \alpha_{1i} + \alpha_{2i})\}V_{ref} + V_{osi}(4 + \alpha_{1i} + \alpha_{2i} + \alpha_{pi})\} \end{aligned} \tag{6}$$

Note that the effects of capacitor mismatch errors on the output voltage are amplification gain error and DAC

gain error. Therefore, there are two gain errors depending on capacitor mismatch and finite gain of amplifier. Equation (6) can be rewritten as:

$$V_{outi} = \left(4+e_{G_i}\right)V_{ini} - \left\{D_i^{(1)} + 2D_i^{(2)} + 3D_i^{(3)}\right\}V_{ref} - \left\{D_i^{(1)}p_{1i} + D_i^{(2)}p_{2i} + D_i^{(3)}\left(p_{1i}+p_{2i}\right)\right\}V_{ref} + V_{osi}\lambda_i \quad (7)$$

where

$$e_{G_i} = \frac{\left(\alpha_{1i}+\alpha_{2i}\right)\left(A_i-4\right)-4\alpha_{pi}-16}{A_i+\alpha_{1i}+\alpha_{2i}+\alpha_{pi}+4}$$

$$p_{1i} = \frac{\alpha_{1i}\left(A_i-1\right)-\alpha_{2i}-\alpha_{pi}-4}{A_i+\alpha_{1i}+\alpha_{2i}+\alpha_{pi}+4}$$

$$p_{2i} = \frac{\alpha_{2i}\left(A_i-2\right)-2\alpha_{1i}-2\alpha_{pi}-8}{A_i+\alpha_{1i}+\alpha_{2i}+\alpha_{pi}+4}$$

$$\lambda_i = \left(\frac{4+\alpha_{1i}+\alpha_{2i}+\alpha_{pi}}{1+\frac{4+\alpha_{1i}+\alpha_{2i}+\alpha_{pi}}{A_i}}\right)$$

and equivalently can be written as:

$$V_{outi} = V_{oi,ideal} + e_i = 4V_{ini} - \left\{D_i^{(1)} + 2D_i^{(2)} + 3D_i^{(3)}\right\}V_{ref} + e_i \quad (8)$$

where, $V_{oi,ideal}$ is ideal output voltage and e_i is total error in ith stage, that is expressed as:

$$e_i = e_{G_i}V_{ini} - \left\{D_i^{(1)}p_{1i} + D_i^{(2)}p_{2i} + D_i^{(3)}p_{3i}\right\}V_{ref} + V_{osi}\lambda_i \quad (9)$$

The output voltage of ith stage is sum of the ideal voltage and total error of this stage that includes of gain errors due to capacitor mismatch and amplifier finite gain, and offset error of op-amp. The input-output relationship of first stage is given by:

$$V_{o1} = V_{o1,ideal} + e_1 = 4V_{in} - V_{DAC1} + e_1$$
$$V_{in} = \frac{V_{o1} + V_{DAC1} - e_1}{4} \quad (10)$$

and for second stage it can be written:

$$V_{o2} = 4V_{in2} - V_{DAC2} + e_2$$
$$V_{in2} = \frac{V_{o2} + V_{DAC2} - e_2}{4} \quad (11)$$
$$V_{in2} = V_{o1}$$

With repeat the above equations for all stages, it can be written as:

$$V_{in} = \frac{V_{DAC1}}{4} + \frac{V_{DAC2}}{4^2} + \frac{V_{DAC3}}{4^3} + \ldots + \frac{V_{DACN-1}}{4^{N-1}} - \left(\frac{e_1}{4} + \frac{e_2}{4^2} + \frac{e_3}{4^3} + \ldots + \frac{e_{N-1}}{4^{N-1}}\right) + \frac{\varepsilon_{qN} + D_N}{4^{N-1}} \quad (12)$$

where, ε_{qN} is quantization error of Nth stage, and D_N is ideal output of last stage. Therefore, the input-referred error, where is equivalent to the contributions of all the individual error is:

$$e_{in,tot} = \frac{e_1}{4} + \frac{e_2}{4^2} + \frac{e_3}{4^3} + \ldots + \frac{e_{N-1}}{4^{N-1}} = \sum_{i=1}^{N-1}\frac{e_i}{4^i} \quad (13)$$

where, e_i is total error in ith stage. To keep the errors smaller than LSB/2 (monotonic and no missing codes), it can be written as [1]:

$$e_i \le \frac{1}{2} \times \frac{FS}{2^{r_{i+1}}} \quad (14)$$

where, FS is the full-scale conversion range, and r_{i+1} is resolution of remaining in the stages after ith stage. Therefore, the MSB stages must have a more accurate gain compared to the LSB stages and first stages the most critical. The accuracy of first stage for M-bit resolution is given by:

$$e_1 \le \frac{1}{2} \times \frac{FS}{2^M} \quad (15)$$

3. 1. Capacitor Mismatch Gain Error The relationship between input and output of ith stage with capacitor mismatch error is given by:

$$V_{oi} = V_{ini}\left(4+\alpha_{1i}+\alpha_{2i}\right) - V_{ref}\left\{D_i^{(1)}(1+\alpha_{1i}) + D_i^{(2)}(2+\alpha_{2i}) + D_i^{(3)}\left(3+\alpha_{1i}+\alpha_{2i}\right)\right\} \quad (16)$$

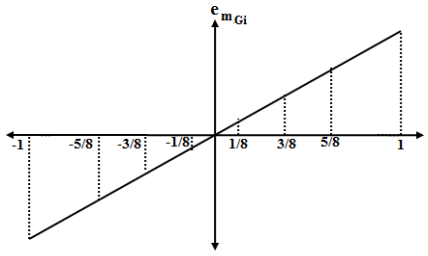

Figure 2. Amplifier gain error due to capacitor mismatch

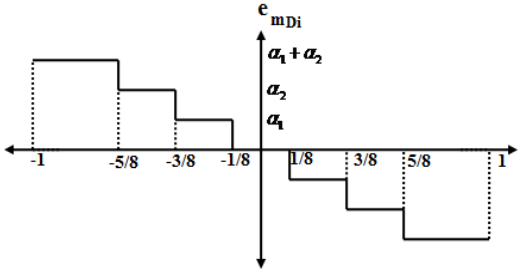

Figure 3. DAC gain error due to capacitor mismatch

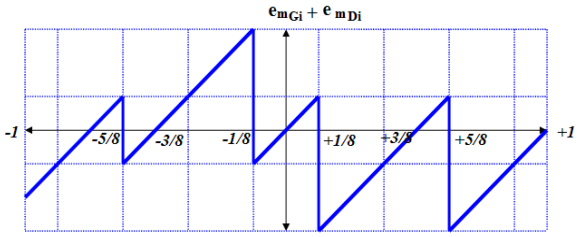

Figure 4. Sum of the amplifier gain and DAC gain errors due to capacitor mismatch

The error due to capacitor mismatch is:

$$e_{mi} = (\alpha_{1i} + \alpha_{2i})V_{ini} - \{D_i^{(1)}\alpha_{1i} + D_i^{(2)}\alpha_{2i} + D_i^{(3)}(\alpha_{1i} + \alpha_{2i})\}V_{ref} \quad (17)$$

Due to capacitor mismatch error, the slope of error voltage can be positive or negative. This error is sum of the amplifier gain error $e_{m_{Gi}}$ and DAC gain error $e_{m_{Di}}$:

$$e_{mi} = e_{m_{Gi}} + e_{m_{Di}} \quad (18)$$

where

$$e_{m_{Gi}} = (\alpha_{1i} + \alpha_{2i})V_{ini} \quad (19)$$

Depending on the ratio capacitors, capacitor mismatch can be positive or negative. Figure 2 shows the amplifier gain error with positive mismatch that has been assumed FS ranges is -1 and +1. DAC gain error is:

$$e_{m_{Di}} = -\{D_i^{(1)}\alpha_{1i} + D_i^{(2)}\alpha_{2i} + D_i^{(3)}(\alpha_{1i} + \alpha_{2i})\}V_{ref} \quad (20)$$

Figure 3 shows this error. Sum of the amplifier gain and DAC gain error is non-ideal error in ith stage depending on capacitor mismatch Figure 4. Assuming that α_{1i} and α_{2i} are the same random variables with Gaussian distribution, zero mean and standard deviation of the error at $V_{ini} = -\frac{1}{8}$ has maximum, therefore:

$$e_{mi,\max} = e_{mi}\left(V_{ini} = -\frac{1}{8}\right) = \frac{6}{8}\sigma_{Ci} \quad (21)$$

The total input referred nonlinearity error due to capacitor mismatch of radix-4 pipeline ADC is given by:

$$\varepsilon_{mi,\max} = \frac{e_{m1,\max}}{4} + \frac{e_{m2,\max}}{4^2} + \ldots + \frac{e_{mN-1,\max}}{4^{N-1}} = \sum_{i=1}^{N-1}\frac{6}{8}\times\frac{\sigma_{Ci}}{4^i} \quad (22)$$

If all stages are the same, $\varepsilon_{mi,\max}$ will have a zero mean and a standard deviation. Therefore [4]:

$$INL_{avg} = \frac{1}{LSB}E\{\varepsilon_{mi,\max}\} = \frac{2^M}{\sqrt{2\pi}}\sigma_{\varepsilon_{mi}} \quad (23)$$

where, INL_{avg} is the average of absolute of $\varepsilon_{mi,\max}$, $E\{.\}$ Denotes the statistical expected value and $\sigma_{\varepsilon_{mi}}$ is the standard deviation of $\varepsilon_{mi,\max}$. Therefore INL_{avg} due to capacitor mismatch error is:

$$INL_{avg} = \frac{2^M}{\sqrt{2\pi}}\frac{6}{8}\sigma_C\sqrt{\sum_{i=1}^{N-1}\left(4^{-i}\right)^2} \cong 0.08\times 2^M\times\sigma_C \quad (24)$$

To keep linearity of ADC (no missing codes), it can be written as:

$$\frac{6}{8}\sigma_{C1} \le \frac{FS}{2^{M+1}}; \qquad \sigma_{C1} \le \frac{1}{3\times 2^{M-2}} \quad (25)$$

3. 2. Amplifier Gain Error Due to finite gain of the operational amplifier, the amplification of input signal in each stage is usually smaller or bigger than ideal value and an error is generated in this stage. The relationship between input and output of ith stage due to finite gain of amplifier is given by:

$$V_{oi} = \frac{1}{1+\frac{4}{A_i}}\left(4V_{in_i} - \{D_i^{(1)} + 2D_i^{(2)} + 3D_i^{(3)}\}V_{ref}\right) \quad (26)$$

Equivalently, it can be expressed as:

$$V_{oi} \cong \left(1 - \frac{4}{A_i}\right)\left(4V_{in_i} - \{D_i^{(1)} + 2D_i^{(2)} + 3D_i^{(3)}\}V_{ref}\right) \quad (27)$$

So, the amplification and DAC gain errors are:

$$e_{A_{Gi}} = \frac{-16}{A_i}V_{in_i} \quad (28)$$

$$e_{A_{Di}} = +\frac{4}{A_i}\{D_i^{(1)} + 2D_i^{(2)} + D_i^{(3)}\}V_{ref\ i} \quad (29)$$

The effects of these errors are explained in Figures 5 and 6. Therefore, the output voltage error is:

$$e_i = -\frac{16}{A_i}V_{ini} + \left\{D_i^{(1)}\frac{4}{A_i} + D_i^{(2)}\frac{8}{A_i} + D_i^{(3)}\frac{12}{A_i}\right\}V_{ref\ i} \quad (30)$$

The error due to the finite gain is, sum of the amplifier gain error and DAC gain error. Figure 7 shows this error. Assuming that $\frac{1}{A_i}$ is random variable with Gaussian distribution, zero mean and standard deviation of σ_{Ai}, the error at $V_{ini} = -1$ has maximum, therefore:

$$e_{Ai,ma} = e_{Ai}(V_{ini} = -1) = 4\sigma_{A_i} \quad (31)$$

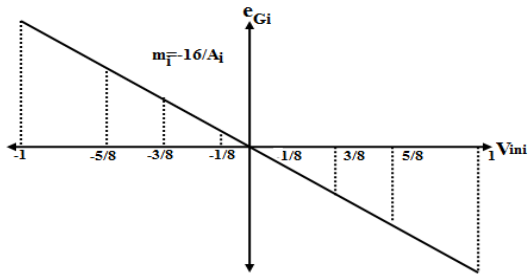

Figure 5. Amplification gain error due to finite gain of amplifier

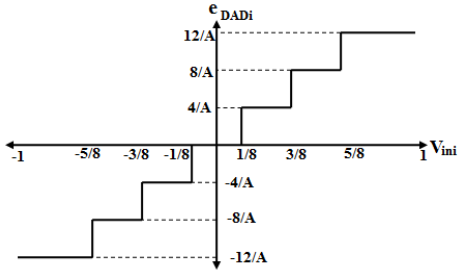

Figure 6. DAC gain error due to finite gain of amplifier

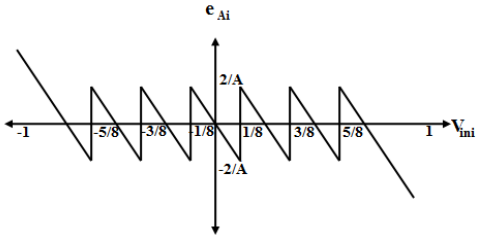

Figure 7. Sum of the amplifier gain and DAC gain errors due to finite gain of amplifier

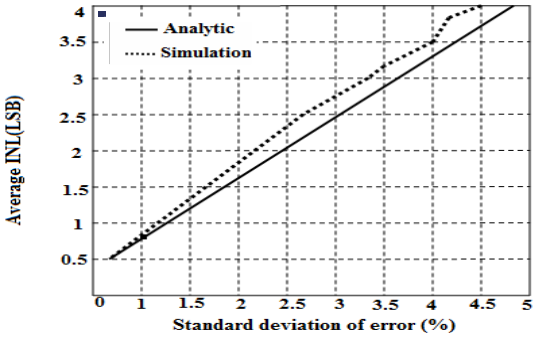

Figure 8. INL vs. standard deviation of capacitor mismatch error for a 10-bit radix-4 pipelined ADC

The average of INL is given by:

$$INL_{avg} = \frac{2^M}{\sqrt{2\pi}} 4\sigma_{A_i} \sqrt{\sum_{i=1}^{N-1} \left(4^{-i}\right)^2} \cong 0.42 \times 2^M \times \sigma_{A_i} \qquad (32)$$

To keep linearity of ADC (no missing codes), it can be written as:

$$4\sigma_{A_i} \le \frac{1}{2^M} \quad \equiv \quad \sigma_{A_i} \le \frac{1}{2^{M+2}} \qquad (33)$$

4. SIMULATION RESULTS

Figure 8 shows the INL diagram of a 10-bit radix-4 pipelined ADC where all stages are identical and only capacitor mismatch error was considered. In this figure, the INL is obtained via simulation and analytic method. For errors smaller than 0.6%, the analytical INL is very close to the simulated INL. For the same conditions (with capacitor mismatch), the INL of an 8-bit radix-4 pipelined ADC is shown in Figure 9. In this figure for errors smaller 2.5 %, the analytical INL is very close to the simulated INL. Therefore, this method is very accurate for INL less than one LSB. Figure 10 shows the INL diagram of a 10-bit radix-4 pipelined ADC due to finite gain of amplifier. It can be seen that, in these conditions the size of errors is smaller. Maximum difference of INL between analytical and simulation results is presented in Table 1.

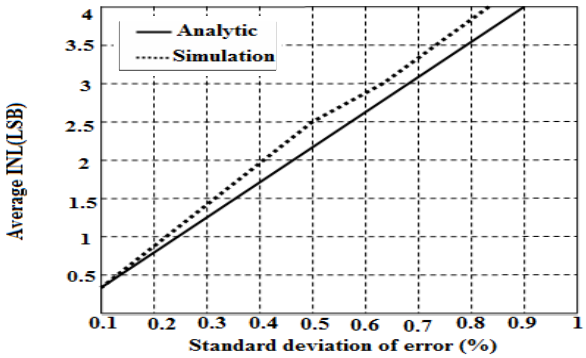

Figure 9. INL vs. standard deviation of capacitor mismatch error for a 8-bit radix-4 pipelined ADC

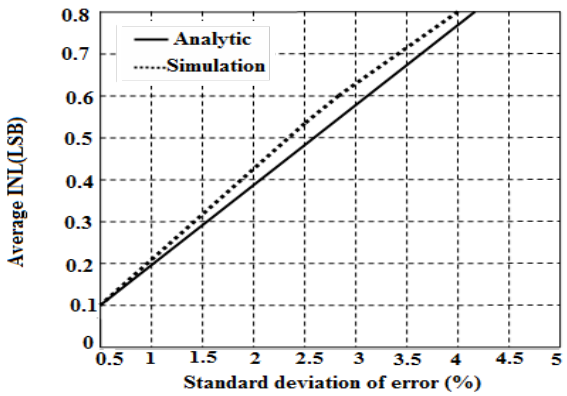

Figure 10. INL vs. standard deviation due to finite gain of amplifier for a 10-bit radix-4 pipelined ADC

TABLE 1. Max. difference of INL between analytical and simulation results

Maximum INL	Gain error @2.5 % dev.	Mismatch Cap. Error @2.5% dev.
Analytical	2LSB	0.48 LSB
Simulation	2.4 LSB	0.53 LSB

5. CONCLUSION

In this paper, a new modeling of all errors in radix-4 pipelined ADC was presented and based on this modeling, the INL vs. standard deviation of capacitor mismatch and finite gain of amplifier was estimated. This method can be extended to other architecture of pipelined ADC.

6. REFERENCES

1. S.H. Lewis, "Optimizing the stage resolution for pipelined multistage analog-to-digital converters for video rate applications," ***IEEE Trans circuits and system II,Exp. Briefs,*** Vol. 39, No. 8, (1992), 516-523.
2. D. Goren, E. Shamsaev, I.A. Wagner, " A Novel Method for Stochastic Nonlinearity Analysis of a CMOS Pipeline ADC," ***Proc. of IEEE Design Automation Conference (DAC)***, (2001)**,**127-132.
3. P.J. Quinn, A.H.M. van Roermund, " Accuracy Limitations of Pipelined ADCs," ***Proc. of IEEE Int. symp. circuits and systems,*** (2005).
4. G. Nikandish, B. Sedighi, M. Sharif Bakhtiar, " INL Prediction Method in Pipeline ADCs," ***APCCAS***, (2006)**,** 13-16.
5. M. Furuta, S. Kawahito, D. Miyazaki, " A Digital-Calibration Tehnique for Redundant Radix-4 Pipelined Analog-to-Digital Converters," ***IEEE Trans***, Vol. 56, (2007), 2031-2310.
6. D. W. Cline and P. R. Gray, " A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 µm CMOS**,"** ***IEEE J. Solid- State Circuit***s, Vol. 31, (1996), 294-303.
7. A. Avizienis,"Signed-digit number representations for fast parallel arithMetic," ***IRE Trans. Electron***. Computer, Vol. EC-10, (1961), 389-400.
8. I. Ahmed, J. Mulder, and D. A. Johns, "A low-power capacitive charge pump based pipelined ADC," ***IEEE Journal of Solid-State Circuits,*** Vol. 45, No. 5, (2010), 1016-1027.
9. K. Deguchi, N. Suwa, M. Ito, T. Kumamoto, and T. Miki, "A 6-bit 3.5-GS/s 0.9-V 98-mW flash ADC in 90-nm CMOS," ***IEEE Journal of Solid-State Circuits,*** Vol. 43, No. 10, (2008), 2303-2310.
10. F. Maloberti, Data converters, Springer, (2007).
11. A. Panigada, I. Galton, "Digital Background Correction of Harmonic Distortion in Pipelined ADCs, ***IEEE Trans. Circuits and Systems I: Regular Papers,*** Vol.53, No.9, (2007), 1885–1895.
12. S. Yang, J. Cheng, P. Wang, "Variable-amplitude dither-based digital background calibration algorithm for linear and high-order nonlinear error in pipelined ADCs," ***Elsevier Microelectronics Journal,*** Vol.41, (2010), 403-410.
13. C. Tsang, .Chiu, J. Vanderhaegen, S. Hoyos, C. Chen, R. Brodersen, B. Nikolic, "Background ADC calibration in digital domain," in ***Proc. IEEE Custom Integrated Circuits Conf.*** , (2008), 301–304.
14. A. Meruva, B. Jalali, "Digital Background Calibration of Higher Order Nonlinearities in Pipelined ADCs," in ***proc. IEEE International Symposium on Circuits and Systems***, , (2007), 1233–1236.
15. S.J. Azhari and L. Safari, "Fully Differential Current Buffers Based on a Novel Common Mode Separation Technique," ***International Journal of Engineering (IJE) Transactions B: Applications***, Vol. 24 , No. 3, (2011), 237 – 249.
16. E. Farshidi and A. Keramatzadeh, "A New Approach for Low Voltage CMOS based on Current-controlled Conveyors," ***International Journal of Engineering (IJE) Transactions B: Applications***, Vol. 27 , No. 5, (2014), 723 – 730.
17. M. Sasikumar and S. Chenthur Pandian "Modified Bi-directional AC/DC Power Converter with Power Factor Correction," ***International Journal of Engineering (IJE) Transactions B: Applications,*** Vol. 25 , No. 3, (2012), 175–180.
18. M. Fallah and H. MiarNaimi, "A Novel Low Voltage, Low Power and High Gain Operational Amplifier Using Negative Resistance and Self Cascode Transistors," ***International Journal of Engineering (IJE) Transactions C: Aspects***, Vol. 26 , No. 3, (2013), 303 – 308.
19. M. D Nair and R. Sankaran, "Simulation and Experimental Verification of Closed Loop Operation of Buck / Boost DC-DC Converter with Soft Switching," ***International Journal of Engineering (IJE) Transactions C: Aspects***, Vol. 25 , No. 4, (2012), 267 – 274.
20. Y. Kebbati, "Modular approach for an ASIC integration of electrical drive controls," ***International Journal of Engineering (IJE) Transactions B: Applications,*** Vol. 27 , No. 2, (2011), 107– 118.

Analysis of Integral Nonlinearity in Radix-4 Pipelined Analog-to-Digital Converters

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چکیده

در این مقاله یک روش تحلیلی برای تقریب میزان غیرخطی بودن مبدلهای آنالوگ به دیجیتال ناشی از اثرات غیر ایدال مداری ارائه شده است. ولتاژ خروجی هر طبقه بصورت جمع ولتاژ ایدال و ولتاژ غیرایدال(ولتاژ خطا) مدل شده است که در آن ولتاژ غیرایدال بدلیل ناهمسانی خازنها، افست مقایسه گر، افست ورودی و بهره محدود تقویت کننده ها ایجاد شده است. معیار تجمیع غیرخطی(INL) به عنوان معیار تقریب تاثیر همه خطاها از همه طبقات مبدلهای آنالوگ به دیجیتال پایه-٤ بدست می آید.

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