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New Hybrid Cascaded Multilevel Inverter

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ABSTRACT

This paper proposes a single-phase five-level inverter with a modified pulse width-modulated (PWM) control scheme. The modified pulse width-modulation technique is developed to reduce switching losses. Also, the proposed multilevel inverter can reduce the requirement of power switches compared to a conventional cascaded multilevel inverter. The modes of operation, control signals, and operating principle of the proposed inverter are analyzed. The inverter is capable of producing five levels of output-voltage (V_s, $V_s/2$, 0, $-V_s$, $-V_s/2$) from the dc supply voltage. In particular, aspects of total harmonic distortion (THD) for the proposed multilevel converters are discussed. The hybrid cascaded H-Bridge inverter with very low switching losses is ideal for such operations. The behaviour of the inverter has been analyzed with the simulation and experimental results. In this paper a new five level inverter with reduced number of switches is proposed and MATLAB/SIMULINK results are presented.

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1. INTRODUCTION

The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonic applications [1]. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs that can be batteries, fuel cells, capacitors, etc. [2]. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multi level inverter is higher output quality, lower harmonic component, better electromagnetic compatibility, and lower switching losses. The most common topologies are the cascaded H-bridge inverter and its derivatives, the Diode-clamped multilevel inverter, and Flying Capacitor multilevel inverter [3]. The main advantage of common topologies is that the rating of the switching devices is highly reduced to the rating of each cell [4]. However, they have the drawback of the required large number of switching devices which equals 2(k-1) where k is the number of levels [5]. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency. Multilevel voltage source inverters have unique structure which allows them to extent high voltages and to reduce individual device switching frequency without the use of transformers [6]. For high-power applications, multilevel inverter structures have the particular advantages of operation at high dc bus voltages, achieved using series connections of switching devices and a reduction in output voltage harmonics, achieved between multiple voltage levels [7]. Moreover, multilevel converters present several other advantages: Generate better output waveforms with a lower dv/dt than the standard converters (power quality) [8].

This paper proposes a new converter topology, presented as a block diagram in Figure 1. This topology includes an H-bridge stage with a bidirectional switch, drastically reducing the power circuit complexity [9]. The new converter topology shown in block diagram offers an important improvement in terms of lower component count and reduced layout complexity when compared with the five-level converters presented in the diode clamped and flying capacitor multilevel inverter [10]. Hybrid converters are converters that present semiconductor switching at different frequencies. Symmetrical converters are converters with symmetric

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dc sources [11]. The new topology achieves almost a 40% reduction in the number of main power switches required and uses no more diodes or capacitors.

2. CIRCUIT CONFIGURATION

The proposed cascaded multilevel inverter as shown in Figure 2 consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four diodes and one IGBT. The inverter produces output voltage in five levels: zero, $0.5V_s$, V_s, $-0.5V_s$ and $-V_s$. In this circuit configuration the two capacitors in the capacitive voltage divider are connected directly across the dc bus, the dynamic voltage balance between the two capacitors is automatically restored.

2.1. Modes of Operation Figure 2 shows the complete power circuit used in the five-level inverter. The H-bridge is formed by the four main power devices, namely Disp1 to Disp4, capacitor voltage divider provides a half of the supply voltage, at node A, formed by C1 and C2. The bidirectional switch formed by the controlled switch Disp5 and the four diodes, D5 to D8, which connects to node A. A resistive load and the same output waveform were considered in all the cases. The required five voltage output levels 0, $V_S/2$, V_S,$-V_S/2$,$-V_S$ are generated as follows:

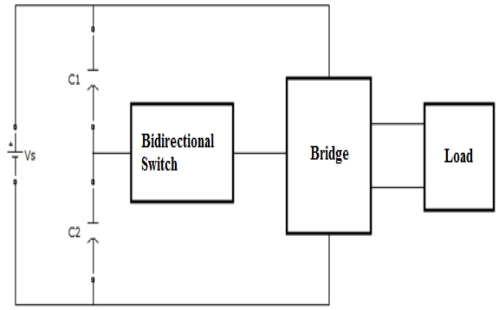

Figure 1. Block diagram of New Topology

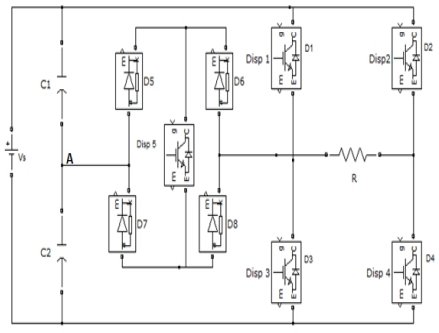

Figure 2. Proposed five level H-bridge Inverter

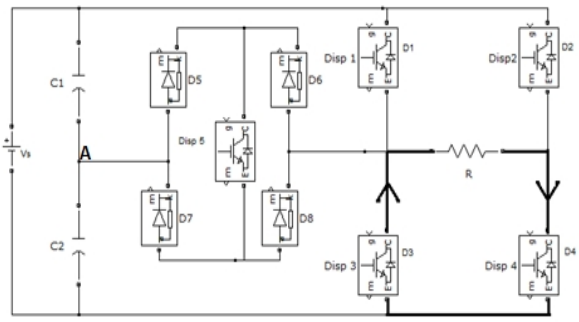

Figure 3. Switching combination required to generate output voltage level Zero

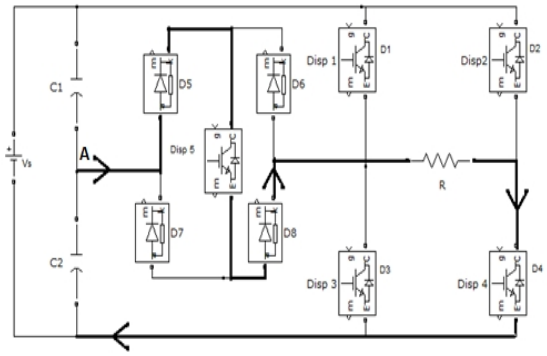

Figure 4. Switching combination required to generate output voltage level $V_s/2$

MODE 1. When the two main switches Disp3 and Disp4 are ON, it short-circuits the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Figure 5 shows the current paths that are active at this stage.

$$V_{out} = 0 \quad ; 0 < t < \pi/6 \;;\; {}^{5\pi}/_{6} < t < 7\pi/6 \;;\; {}^{11\pi}/_{6} < t < 2\pi$$

MODE 2. When the auxiliary switch, Disp5 is ON, it connects the positive terminal of load to node A, through diodes D5 and D8, and when the main switch Disp4 is ON, it connects the negative terminal of load to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_s/2$. Figure 4 shows the current paths that are active at this stage.

$$V_{out} = {}^{V_s}/_{2} \quad ; {}^{\pi}/_{6} < t < \pi/3 \;;\; {}^{2\pi}/_{3} < t < 5\pi/6$$

MODE 3. When the main switch Disp1 is ON, it connects the positive terminal of load to V_S, and when Disp4 is ON, it connects the negative terminal of load to

ground. All other controlled switches are OFF; then the voltage applied to the load terminals is V_S. Figure 3 shows the current paths that are active at this stage.

$V_{out} = V_s$; $\pi/3 < t < 2\pi/3$

MODE 4: When the auxiliary switch, Disp5 is ON, it connects the positive terminal of load to node A, through diodes D6 and D7, and when the main switch Disp2 is ON, it connects the negative terminal of load to $V_S/2$. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_s/2$. Figure 6 shows the current paths that are active at this stage.

; $7\pi/6 < t < 8\pi/6$

$V_{out} = -V_s/2$; $5\pi/3 < t < 11\pi/6$

MODE 5. When the main switch Disp2 is ON, it connects the negative terminal of load to V_s, and when Disp3 is ON, it connects positive terminal of load to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_s$. Figure 7 shows the current paths that are active at this stage.

$V_{out} = -V_s$; $8\pi/6 < t < 5\pi/3$

TABLE 1. Switching table

Disp 1	Disp 2	Disp 3	Disp 4	Disp 5	V_{out}
On	Off	Off	On	Off	V_s
Off	Off	Off	On	On	$V_s/2$
Off	Off	On	On	Off	0
Off	On	Off	Off	On	$-V_s/2$
On	Off	Off	On	Off	$-V_s$

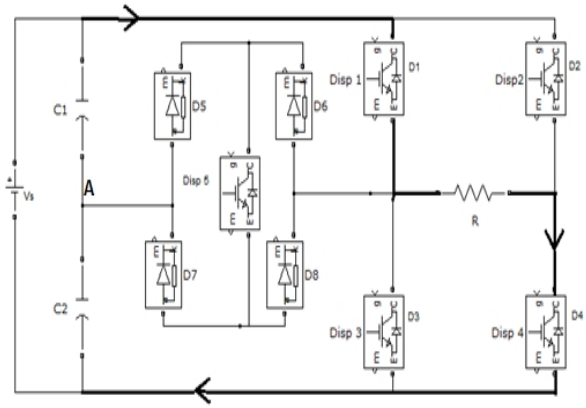

Figure 5. Switching combination required to generate output voltage level V_s

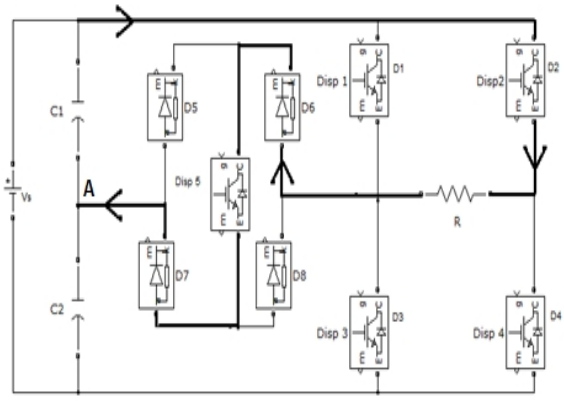

Figure 6. Switching combination required to generate output voltage level $-V_s/2$

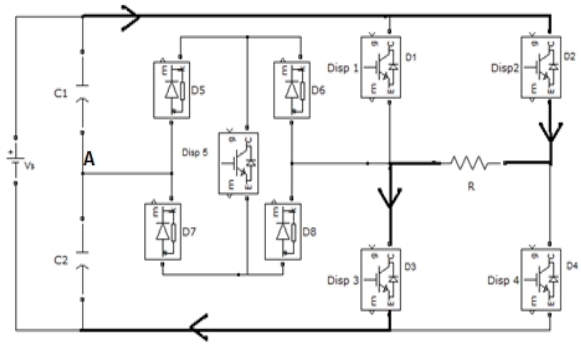

Figure 7. Switching combination required to generate output voltage level $-V_s$

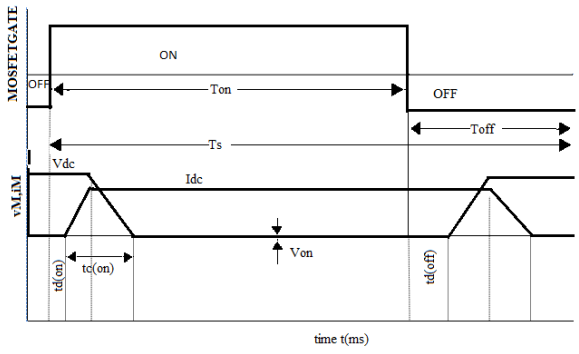

Figure 8. Linear characteristics of IGBT

3. SWITCHING LOSS CALCULATIONS

Consider a MOSFET switch connected across a dc voltage of value V_{dc}. During on time, the current through switch is I_{dc}. The figure shows the waveforms of the voltage and current through switch when it is operated at a switching frequency of $F_s=1/T_s$, where T_s is the switching period. In the figure, v_M, i_M are the

voltage across and the current through the MOSFET [12].

Switching losses can be calculated from the turn on and turn off characteristics of the switch. Instantaneous voltage and current during on time $t_{c(on)}$ are:

$$v(t) = V_{dc} - (V_{dc} - V_{on}) * (t/t_{c(on)} \quad (1)$$

$$i(t) = I_{dc} * (t/t_{c(on)} \quad (2)$$

where,

v(t), i(t)	instantaneous voltage and current
V_{dc}	voltage across switch when turned off
V_{on}	voltage across switch when turned on
t	time in sec
$t_{c(on)}$	turn-on cross over interval
I_{dc}	current through switch when turned on
T_s	sampling time in sec

Instantaneous power during the interval $t_{c(on)}$ is:

$$p(t) = v(t) * i(t) = \left\{V_{dc} * I_{dc} * \left(\frac{t}{t_{c(on)}}\right)\right\} - (V_{dc} - V_{on}) * \left(\frac{t^2}{t_{c(on)}^2}\right) \quad (3)$$

Energy dissipated during this interval is $t_{c(on)}$

$$E_{c,on} = \int_0^{t_{c(on)}} \left\{V_{dc} * I_{dc} * \left(\frac{t}{t_{c(on)}}\right)\right\} - (V_{dc} - V_{on}) * \left(\frac{t^2}{t_{c(on)}^2}\right) = (V_{dc} * I_{dc} * t_{c(on)})/6 - (V_{on} * I_{dc} * t_{c(on)})/3 \quad (4)$$

During turn off transition, of $t_{c(off)}$, the current falls from I_{dc} to zero and the V_{on} increases linearly to V_{dc}. The instantaneous voltage and current during this period are:

$$v(t) = V_{on} + (V_{dc} - V_{on})/t_{c(off)} \quad (5)$$

$$i(t) = I_{dc} - I_{dc}/t_{c(off)} \quad (6)$$

where,

$t_{c(off)}$	turn off cross over interval
T	The instantaneous power dissipated during the interval is $t_{c(off)}$

$$p(t) = v(t) * i(t) = V_{on} * I_{dc} + (V_{dc} - V_{on}) * I_{dc} * \left(\frac{t}{t_{c(off)}}\right) - V_{on} * I_{dc} * \left(\frac{t}{t_{c(off)}}\right) - (V_{dc} - V_{on}) * I_{dc} * \left(\frac{t^2}{t_{c(off)}^2}\right) \quad (7)$$

The average switching loss P_{sw} in the switch is:

$$P_{sw} = \left(\frac{1}{6}\right) * V_{dc} * I_{dc} * \frac{t_{c(on)} + t_{c(off)}}{T_s} + \left(\frac{1}{3}\right) * V_{on} * I_{dc} * \{t_{c(on)} + t_{c(off)}\}/T_s \quad (8)$$

4. PROPOSED PWM TECHNIQUE

Figure 9 shows the relationship between the sinusoidal reference signal and the triangular carrier signal which is used to create the PWM signal. The output of the PWM signal is either 1, when $V_{ctrl} > V_{tri}$ or 0, when $V_{ctrl,} < V_{tri}$, and the PWM signal width can be written as Equation (9)

$$T_{Pwm} = A_{ctrl}.T_{tri} \quad ;0 \le A_{ctrl} \le 1 \quad (9)$$

where,

T_{PWM}	Width of the PWM signal
A_{ctrl}	Height of the control signal
T_{tri}	Period of the triangular signal
V_{ctrl}	Output voltage of the control signal
V_{tri}	Output voltage of the triangular signal

Modulated signal is created as per Equations (11) and (12), and amplitude modulation index m_a can be found in the Equation (13).

$$f(t) = m_a \sin(\omega t) \quad (10)$$

$$A_1 = 1; f(t) \ge 0 \quad 0; f(t) < 0 \quad (11)$$

$$A_2 = 1; |f(t)| \ge 1/2 \quad 0; |f(t) < 1/2 \quad (12)$$

$$m_a = V_{ctrl} / V_{tri} \quad (13)$$

The hybrid multilevel inverter consists of one full H-bridge and bidirectional switch. The one leg of full H-bridge operates at square wave mode and remaining switches operate at PWM mode. The modulated signals PWM, A2, and A1 as shown in Figure 13 are the parameters used in digital process to generate the control signals as shown in Table 2.

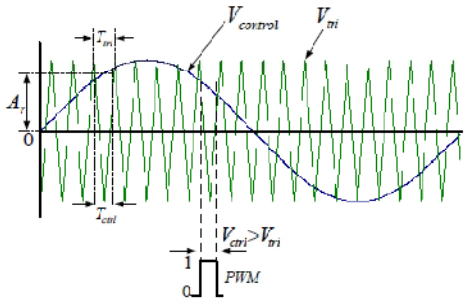

Figure 9. The relationship between the reference signal and the carrier signal

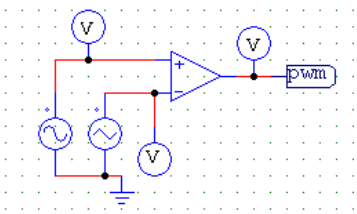

Figure 10. Modulated signal generation of PWM

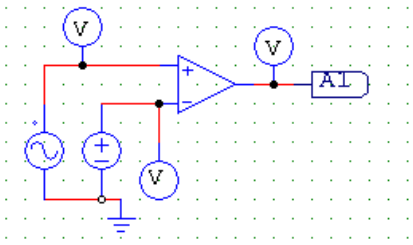

Figure 11. Modulated Signal generation of A1

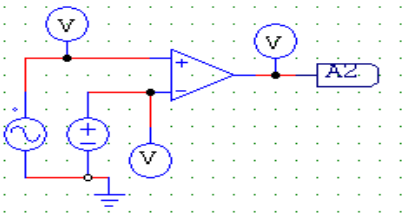

Figure 12. Modulated signal generation of A2

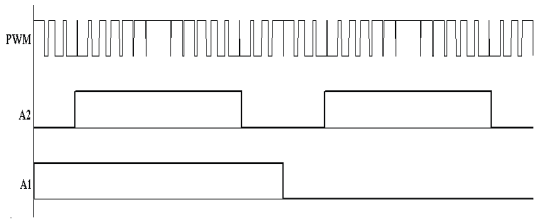

Figure 13. Modulated Signals

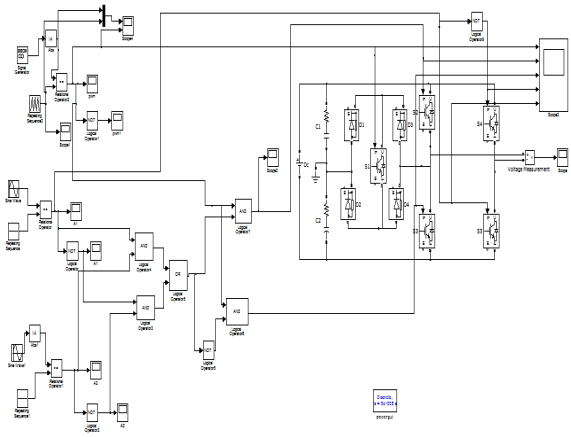

Figure 14. Simulink model of proposed multilevel inverter

TABLE 2. Digital process of the control signals

Electronic Switch Devices	Digital Process
S1	PWM•((A2•A1)+($\overline{A2}$•$\overline{A1}$))
S2	$\overline{A1}$
S3	PWM•$\overline{((A2•A1)+(A2•A1))}$
S4	A1
S5	PWM

5. SIMULATION RESULTS

The control signals are generated and the output voltage evaluated by using the MATLAB/SIMULINK platform. Output voltage can be controlled using the modulation index and output frequency controlled by adjusting the frequency. The simulation results of the proposed hybrid multilevel inverter are illustrated in Figure 17. The simulation results based on switching losses analysis are also performed for the proposed hybrid multilevel inverter as shown in Figure 14.

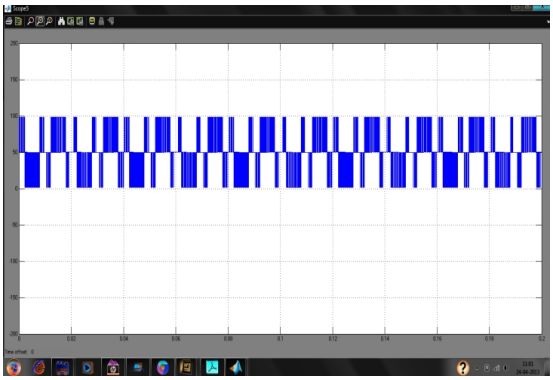

Figure 15. Balancing Capacitor Voltage of C1

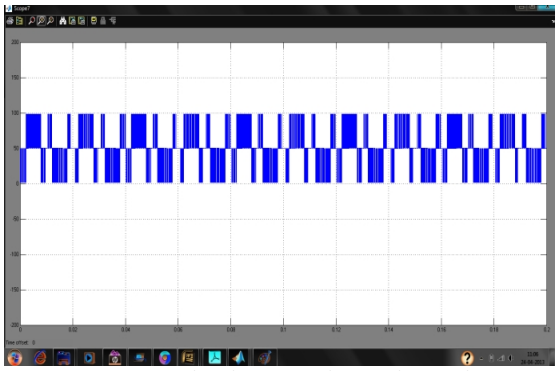

Figure 16. Balancing Capacitor Voltage of C2

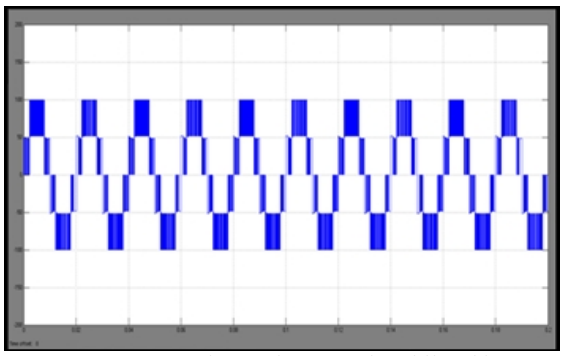

Figure 17. Output voltage of proposed multilevel inverter

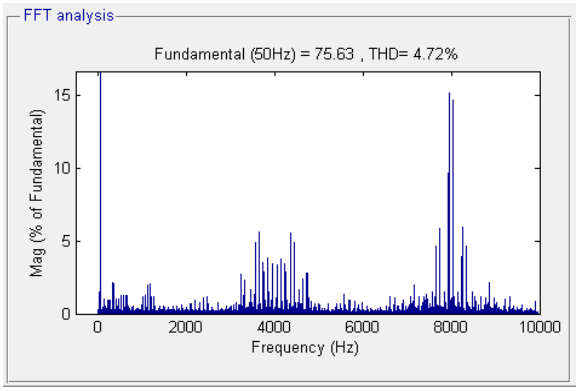

Figure 18. THD Analysis of Proposed multilevel inverter

TABLE 3. Simulation parameters for new hybrid cascaded multilevel inverter

Input voltage	100V
Frequency of the carrier	12,000Hz
Dc bus utilisation voltage	93.01V
Modulation index	0.75

TABLE 4. Comparison between different topologies

	Diode clamped	Flying capacitor	Cascaded H-bridge	New hybrid cascaded
No. of switches	8	8	8	5
No. dc supply	1	1	2	1
Main diodes	8	8	8	5
Clamping diodes	12	0	0	0
Dc bus capacitors	4	4	2	2
Balancing capacitors	0	0	6	0

Table 4 shows the comparison between different topologies for a five level multilevel inverter based on requirement of main switches, dc supply, main diodes, clamping diodes, balancing capacitors, and DC bus capacitors.

6. EXPERIMENTAL RESULTS

The block diagram shown in Figure 19 explains the hardware which consists of power supply, DC source, Microcontroller, Driver circuit and the power switches. To experimentally validate the new hybrid cascaded MLI using the proposed modulation technique, a prototype of five-level inverter has been built using IRF460 MOSFET for the full bridge inverter and power diode for the auxiliary switch as shown in Figure 20. The gating signals are generated using PIC16F877A microcontroller which is shown in Figures 21- 24. The output voltage for the five level is shown in Figure 25.

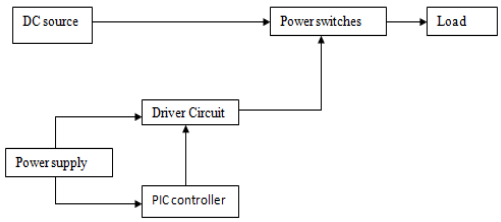

Figure 19. Block Diagram Representation

Figure 20. Hardware Implementation

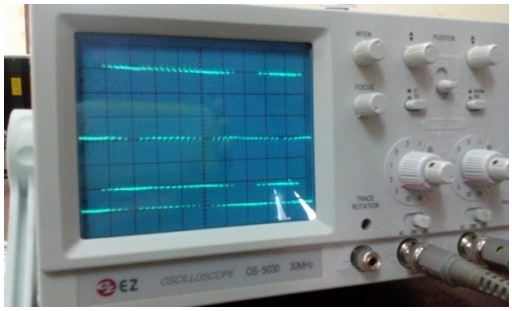

Figure 21. Gate pulse for the switch 1

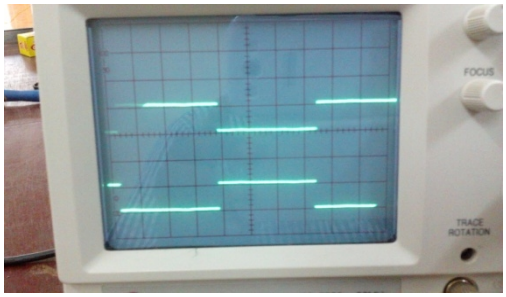

Figure 22. Gate pulse for the switch 2 and switch 4

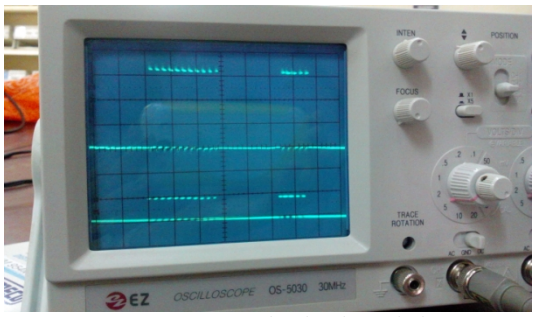

Figure 23. Gate pulse for the switch 3

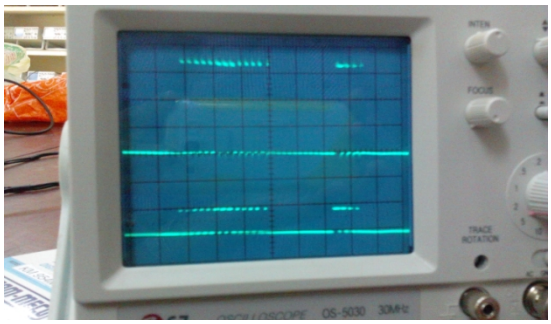

Figure 24. Gate pulse for the switch 5

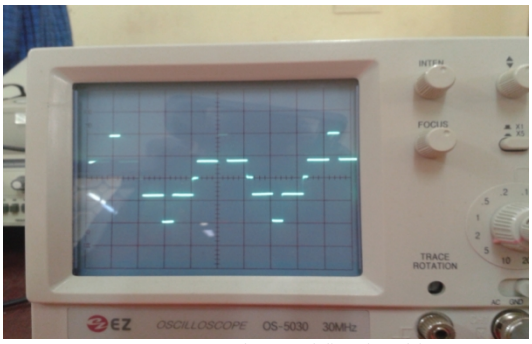

Figure 25. Output voltage of five level inverter

7. CONCLUSION

In conclusion, a single-phase five-level inverter with a modified pulse width-modulated (PWM) control scheme has been developed. The proposed multilevel inverter can reduce the requirement of power switches compared to a conventional cascaded multilevel inverter. The modes of operation, control signals, and operating principle of the proposed inverter were analyzed. The inverter is capable of producing five levels of output-voltage (V_s, $V_s/2$, 0, $-V_s$, $-V_s/2$) from the dc supply voltage. Aspects of total harmonic distortion (THD) for the proposed multilevel converters have been discussed. The behaviour of the inverter has been analyzed with the simulation results and experimental results.

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New Hybrid Cascaded Multilevel Inverter

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چکیده

در این مقاله یک اینورتر پنج سطحی تک فاز با طرح کنترل مدوله شده‌ی پهنای پالس اصلاح شده (PWM) پیشنهاد شده است. روش مدولاسیون پهنای پالس اصلاح داده شده برای کاهش تلفات سوئیچینگ است. همچنین، اینورتر چند سطحی ارائه شده می‌تواند نیاز به سوئیچ های قدرت در مقایسه با اینورتر چند سطحی آبشاری متعارف را کاهش دهد. حالت‌های کار، سیگنال‌های کنترل، و مبنای عمل اینورتر پیشنهادی تحلیل شده است. اینورتر قادر به تولید پنج سطح ولتاژ های خروجی $(V_s, V_s/2, 0, -V_s, -V_s/2)$ از منبع تغذیه‌ی ولتاژ مستقیم است. جنبه‌های واپیچش هارمونیکی کل (THD) برای مبدل‌های چند سطحی پیشنهادی به طور خاص مورد بحث قرار گرفته است. اینورتر ترکیبی آبشاری و H- پل با تلفات سوئیچینگ بسیار کم برای چنین عملیاتی ایده‌آل است. رفتار اینورتر با شبیه سازی و نتایج تجربی تحلیل شده است. در این مقاله اینورتر پنج سطحی جدید با تعداد سوئیچ‌های کاهش‌یافته به همراه نتایج MATLAB / SIMULINK ارائه شده است.

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