NEURAL NETWORK IMPLEMENTATION OF A THREE PHASE REGULATED PWM AC TO DC CONVERTER WITH INPUT UNBALANCE CORRECTION

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Abstract Under unbalanced supply condition low order harmonics will appear at the input and output terminals of the PWM AC to DC converter. Based on the positive and negative sequence components, an unbalanced transfer matrix in terms of the input phase voltages is derived. An on-line method using a neural network (NN) is used to implement this transfer matrix. It is shown that by using an additional load feedback loop the unbalance correction property is not affected.

Key Words PWM AC to DC Converter, Unbalanced Input, NN Implementation

چکیده تخت شرایط ورودی نامتعادل هارمونیک های مرتبه های پایین در ترمینالهای ورودی و خروجی مبدل PWM AC-DC ظاهر می شوند و بنابراین خواص عالی تکنیک PWM از دست خواهد رفت. بر پایهٔ محاسبهٔ مؤلفه های مثبت و منفی ولتاژ ورودی، یک ماتریس تبدیل نامتعادل برای مبدل بدست خواهیم آورد که بر حسب ولتاژ فازهای ورودی قابل بیان می باشد. برای اعمال این روش از یک مدار آنالوگ برای تولید المانهای ماتریس تبدیل استفاده می کنیم و در نهایت با استفاده از یک شبکهٔ عصبی سیگنالهای گیت یوئیچها را، بمنظور اعمال تصحیح فوق، تولید خواهیم نمود. همچنین نشان خواهیم داد که با استفاده از یک حلقهٔ تنظیم ولتاژ خروجی عملکرد تصحیح عدم تعادل صدمه ای نخواهد دید و ولتاژ خروجی قابل تنظیم خواهد بود.

INTRODUCTION

Recent evolution of fully controlled power semiconductor devices with high frequency switching capability has made it possible to use PWM technique to improve the quality of input and output waveforms of the AC to DC converters. This approach offers advanced properties such as sinusoidal input currents at unity power factor and high quality output DC voltage.

However, under real operating conditions the input supply is unbalanced and under this condition the standard PWM tecnique will be impaired and the low-order abnormal harmonics will appear in the output and input terminals of the converter.

The unbalanced supply occurs frequenctly in a weak AC system due to several conditions such as single phase loads which are not uniformaly distributed among the three phases, nonsymmetrical transformer winding or transmission impedance, etc. Particularly the PWM converters which are used frequently in industrial power systems have a unbalanced inputs.

There are, in general, three ways to reduce or eliminate undesired effects caused by unbalanced input supply of a PWM AC to DC converter, i.e, using a large output low-pass filter, a fast feedback loop, or a feedforward control loop. A large output low-pass filter, however, increases the size of the converter and the time constant of the system which in turn will decrease the speed of the response. Using a fast output feedback control loop would require a relatively high switching frequency thus limiting the converter power handling abilities. Several feedforward approaches

for eliminating the effects of unbalanced input have been proposed [1-3]. In [1] the control implementation requires many components which reduce the accuracy and the reliability of the converter and speed of the response. In the last feedforward approach [3], since the main objective is to regulated the output voltage, the second harmonic is only eliminated when the unbalance is less than 8%.

In this paper an NN implementation of a simple feedforward method to improve the performance of a PWM AC to DC converter under unbalanced condition, is presented. Based on positive and negative sequence components calculation, a transfer matrix which eliminates generated abnormal harmonics at the output and input terminals of the converter under unbalanced condition is derived. By using a three layer perceptron, we generate, on-line, the associated PWM gating signals for six switches.

INPUT UNBALANCE CORRECTION METHOD

Figure 1 shows a general three phase PWM AC to DC converter. When the input supply is unbalanced the three input phase voltages by a generalized form as:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_a \sin(\omega t + \phi_a) \\ V_b \sin(\omega t + \phi_b) \\ V_c \sin(\omega t + \phi_c) \end{bmatrix} \quad (1)$$

where V_a, V_b, V_c represent amplitudes and ϕ_a, ϕ_b, ϕ_c represnt the three phase voltages. Three unbalanced phasors of a three phase system can be resolved into

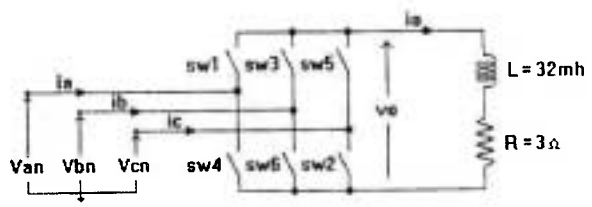

Figure1. General 3-phase AC to DC converter.

three balanced systems of phasors [4]: positive sequence, negative sequenee and zero sequenee. Assuming there is no neutral path in the system, the zero sequence component must be zero. If we assume $[V_p]$ and $[V_n]$ as the positive and negative sequenee's phasors, from [4] we have:

$$[V_p] = \begin{bmatrix} V_{ap} \\ a V_{ap} \\ a^2 V_{ap} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} V_a + \alpha V_b + \alpha^2 V_c \\ V_a + \alpha^2 V_b + V_c \\ \alpha^2 V_a + V_b + \alpha V_c \end{bmatrix} \quad (2)$$

$$[V_n] = \begin{bmatrix} V_{an} \\ \alpha^2 V_{an} \\ \alpha V_{an} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} V_a + \alpha^2 V_b + \alpha V_c \\ \alpha^2 V_a + \alpha V_b + V_c \\ \alpha V_a + V_b + \alpha^2 V_c \end{bmatrix} \quad (3)$$

Where α is an operator and its value is $1 < 120°$, and V_a, V_b, V_c are the phasors of input phase voltages. Let us consider the transfer matrix of converter [T], then the output DC voltage of the converter is equal to:

$$v_o = [T]\,[v_i] \quad (4)$$

where [T] is a 1×3 matrix. When the input supply in unhalanced it was shown in [1] that if the transfer matrix [T] is symmetrical, the abnormal harmonics will appear in the output DC voltage and inp ut current (2nd order harmonic in the output DC voltage and third order harmonic in the input current). The simulation results for this case are shown in Figure 6.

By using an unsymmetrical transfer matrix which consists of two symmetrical component matrixes we can compensate the input unbalance and eliminate the abnormal harmonics in the output and input terminals of PWM AC to DC converter:

$$[T] = [T_p] + [T_n] \quad (5)$$

By substituting Equation 5 into Equation 4 it could be

shown:

$$v_o = [T][v_t] = ([T_p] + [T_n])([v_p] + [v_n])$$
$$= [T_p][v_p] + [T_n][v_n] + [T_p][v_n] + [T_n][v_p] \quad (6)$$

It was shown in [1] that the first two terms in Equation 6 produce DC component of v_o and the second two terms in Equation 6 produce the 2nd order harmonic of DC voltage and this in turn produces the third order harmonic of input current. This abnormal harmonics eliminated by choosing the second two terms of Equation 6 as:

$$[T_p] = kr\,[v_p]^T \quad (7)$$

$$[T_n] = -\,kr\,[v_n]^T \quad (8)$$

where kr is an arbitrary scaling Factor. Since:

$$[T_p][v_n] + [T_n][v_p] = kr\,[v_p]^T[v_n] - kr\,[v_n]^T[v_p] = 0 \quad (9)$$

Thus the output voltage v_o becomes:

$$v_o = kr\,[v_p]^T[v_p] - kr\,[v_n]^T[v_n] \quad (10)$$

$$= \frac{3kr}{2}(V_{mp} - V_{mn}) \quad (11)$$

Where V_{mp} and V_{mn} are the amplitudes of $[v_p]$ and $[v_n]$. By substituting Equations 7 and 8 into Equation 5 the transfer matrix becemes:

$$[T] = kr\,([v_p]^T + [v_n]^T) \quad (12)$$

Finally by substituting time relation Equations of 2 and 3 into Equation 12 the transfer matrix becomes:

$$[T] = \frac{kr}{\sqrt{3}}\begin{bmatrix} v_b \sin(\omega t + \phi_b + 90) + v_c \sin(\omega t + \phi_c + 90) \\ v_c \sin(\omega t + \phi_c + 90) + v_a \sin(\omega t + \phi_a + 90) \\ v_a \sin(\omega t + \phi_a + 90) + v_b \sin(\omega t + \phi_b + 90) \end{bmatrix} \quad (13)$$

From Equation 13 we find out that we can directly calculate the transfer matrix from phase voltages by 90 phase shift lead or lag. And so the calculation of positive and negative sequences is not needed. The factor kr is limited by the maximum gain of PWM technique used. Thus:

$$kr\,V_{mp} = G \quad (14)$$

where G is the maximum PWM gain and for SPWM which is used in this paper it is equal to $\sqrt{3}/2$. Therefore, considering (14) we have:

$$kr = \frac{G}{V_{mp}} = \frac{\sqrt{3}}{2\,V_{mp}} \quad (15)$$

From Equations 11 and 15 the output DC voltage is equal to:

$$V_{o,DC} = \frac{3\sqrt{3}}{4} V_{mp}(1 - U_b^2) \quad (16)$$

where $U_b = V_{mn}V_{mp}$ is defined as unbalance factor. Equation 16 shows that when U_b increases, the output DC voltage decreases, and when it is equal to %100, the output DC voltage is equal to zero.

IMPLEMENTATION OF THE TRANSFER MATRIX

For implementation of the transfer matrix we use the circuit shown in Figure 2 and the NN gating signal

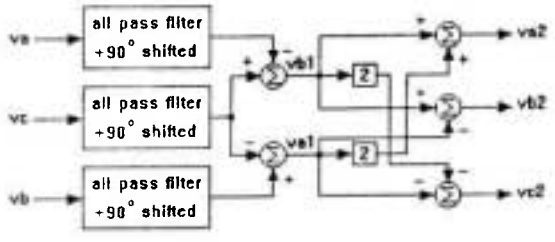

Figure 2. Unbalance correction circuit.

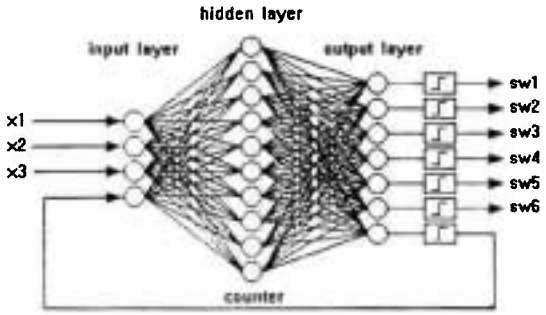

Figure 3. NN gating signal generator.

generator shown in Figure 3. The circuit shown in Figure 2 consists of two parts. One part calculates the elements of transfer matrix and the other compensates the phase and magnitude error due to using dynamic trilogic PWM.

Dynamic Trilogic PWM [5]

For on-line application of the SPWM technique to the AC to DC converter we compare the triangular carrier with the three modulating waves and generate the bilogic PWM signals X_1, X_2 and X_3 which have two possible values of +1, and -1 (+1 when modulating wave is greater than carrier and -1 otherwise). Now we must translate the bilogic PWM signals to trilogic PWM signals Y_a, Y_b and Y_c which have three possible values +1,0 and -1 (+1 when upper switch conducts, -1 when lower switch conducts and 0 when the two switches are off). The formula for translating the bilogic PWM variables to the trilogic PWM variables is based on the linear mapping:

$$\begin{bmatrix} Y_a \\ Y_b \\ Y_c \end{bmatrix} = \frac{1}{2}[C] \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} \tag{17}$$

Where:

$$[C] = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \tag{18}$$

The important property of the trilogic PWM is that only one of the upper switches and one of the lower switches can conduct simultaneously:

Calculation of Transfer Matrix Elements

This part consists of two summer and three all pass filters with 90° phase shifts. The inputs are the three instantaneous input phase voltages which are scaled down. This part calculates two elements of the transfer matrix [T] based on Equation 13. It should be noted that the third element of transfer matrix v_{cl}, which can be obtained by inverting the $v_{al} + v_{bl}$ is omitted since it is not required in the next part.

Magnitude and Phase Error Compensation

From Equation 17 we found that Y_a is proportional to the difference between X_1 and X_2. Thus if we produce X_1, X_2 and X_3 by comparing the elements of the transfer matrix [T] with the triangular carrier, then there will be a magnitude and phase error between the gating signals and the elemenets of transfer matrix [T], and this will result in no correction for the abnormal harmonics, created under unbalanced condition. Under a symmetrical condition the phase error will be 30° (which is the difference between the line and phase voltages in a symmetrical system). To overcome this problem, a line to phase transformation is required. By taking v_{al} and v_{bl} as the line variables and v_{a2}, v_{b2} and v_{c2} as the phase variables we have:

$$\begin{bmatrix} v_{al} \\ v_{bl} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_{a2} \\ v_{b2} \\ v_{c2} \end{bmatrix} \tag{19}$$

The third equation is based on the assumption that there is no zero sequence component and thus the sum of three voltages is equal to zero. From the above equation we have:

$$\begin{bmatrix} v_{a2} \\ v_{b2} \\ v_{c2} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & 1 & 0 \\ -1 & 1 & 1 \\ -1 & -2 & 1 \end{bmatrix}\begin{bmatrix} v_{a1} \\ v_{b1} \\ 0 \end{bmatrix} \quad (20)$$

The 1/3 gain appears in all of the equations which is ignored in the circuit of Figure 2.

Gating Signal Generation

By using a three layer NN, we generate the PWM gating singals for switches, on-line.

First the bilogic PWM signals X_1, X_2 and X_3 are produced by comparing the modulating waves v_{a2}, v_{b2} and v_{c2}, produced by unbalance correction circuit of Figure 2, with the triangular carrier. Then this bilogic signal is fed into the NN gating signal genarator of Figure 3 through coeficient scaling factor k.

As discussed before, this type of PWM ensures that at each time only one switch from upper switches and one switch from the lower switches conduct. When all switches are off, the NN generates the free-wheeling pulses and sends them to one of the three converter legs to provide free-wheeling of load current. By using one of the outputs of the NN, which feeds back to input and works as a counter which counts 0, 1, 2 and then resets, the pulses are evently distributed to all the counter legs.

The NN Structure

Recently parallel distribution processing such as the NN have received wide attention in order to process complex data in a short time. Because of parallel processing mechanism of the network, it is expected that the NN can execute the non-linear data mapping in a very short time. At this time, however, the computation speed with simulator is not so fast because the operation of the NN is simulated in a series sequential computer at present. But the processing speed of an NN chip with parallel processing mechanism is very fast.

The NN structure which is used in this paper is shown in Figure 3. It consists of three distinct layers. The input layer, which receives the input data, a hidden layer which begins the learning process, and an output layer, which continues the learning process and provides outputs.

Inputs of the network are three bilogic signals and the output of the counter which are feedback to inputs and outputs of the network are gating signals for switches and output of the counter.

Since the node activation function is given sigmoid, the NN outputs are not always exactly 0 or 1, and it must be digitized to obtain the necessary gating signals for the switches. The digitized pattern is the output of the NN passing through the hard limiter given by:

$$\text{if } sw_i > 0.5 \quad sw_i = 1$$
$$\text{else} \quad sw_i = 0 \quad i = 1, \ldots, 6 \quad (21)$$

We have tested many types of NN and decided to use one hidden layer with 10 neurons bacause the number of neurons was the least and the learning process took a relatively short time.

The NN Learning

By using Equation 17 we can produce the learning patterns for the NN. First we produce the 8 combinations of the three bilogic PWM variables and their corresponding trilogic PWM variables and switching patterns. Then by adding one dimention to this data, for counter operation, we produce the learning patterns which consist of 24 stimula patterns. The learning patterns are given in appendix.

The error backpropagation algorithm is used to optimize the weights and bios values such that the output of the NN will approach the desired output.

THE DC VOLTAGE REGULATION LOOP

A standard DC voltage loop with a PI regulator is

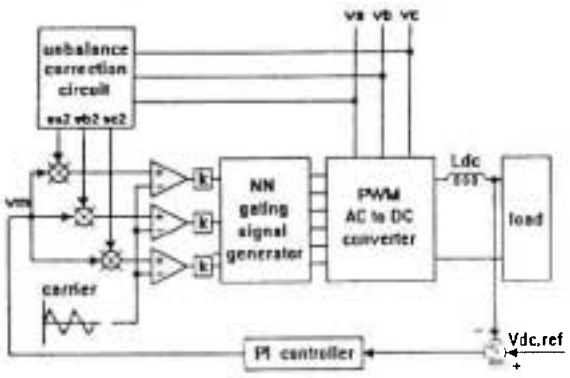

Figure 4. DC voltage regulation loop.

used to vary the output voltage according to the load demands Figure 4. The ratio of A_r, to A_c is the control variable and is defined as modulation index where A_r is the amplitude of the modulating wave and A_r is the amplitude of the carrier. By keeping the A_c constant, we can control the output DC voltage by controlling the A_r. The modulating waves produced by the unbalance correction circuit of Figure 2, are multiplied by the output of the PI controller and thus the output DC voltage can be controlled. The controller parameter decided by simulation is equal to $K_p=0.2$ and $T_i=0.01$s.

SIMULATION RESULTS

Steady State Results

Let us assume the unbalanced input phase voltages are;

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 100\sin(\omega t) \\ 60.3\sin(\omega t - 2\pi/3) \\ 87.2\sin(\omega t + 2.5) \end{bmatrix} \quad (22)$$

(Note that the sum of $v_a+v_b+v_c=0$ and the unbalance factor is equal to %20). The supply frequency is equal to 60Hz and the switching frequency is equal to 1260Hz (21 per unit). Under these conditions, the simulation results of the

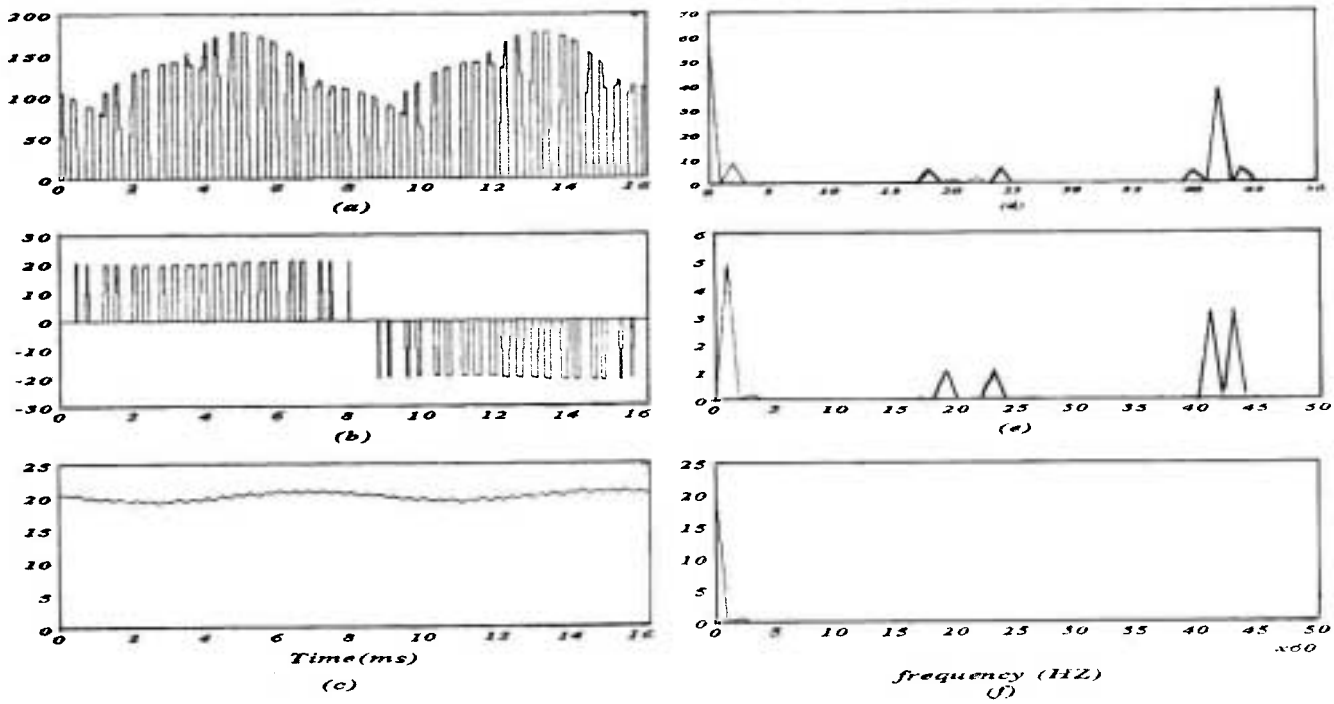

Figure 5. Input/output waveforms of the converter without unbalance correction. (**a**) output voltage. (**d**) output voltage spectrum. (**b**) input current. (**e**) input current spectrum. (**c**) output current. (**f**) output current spectrum.

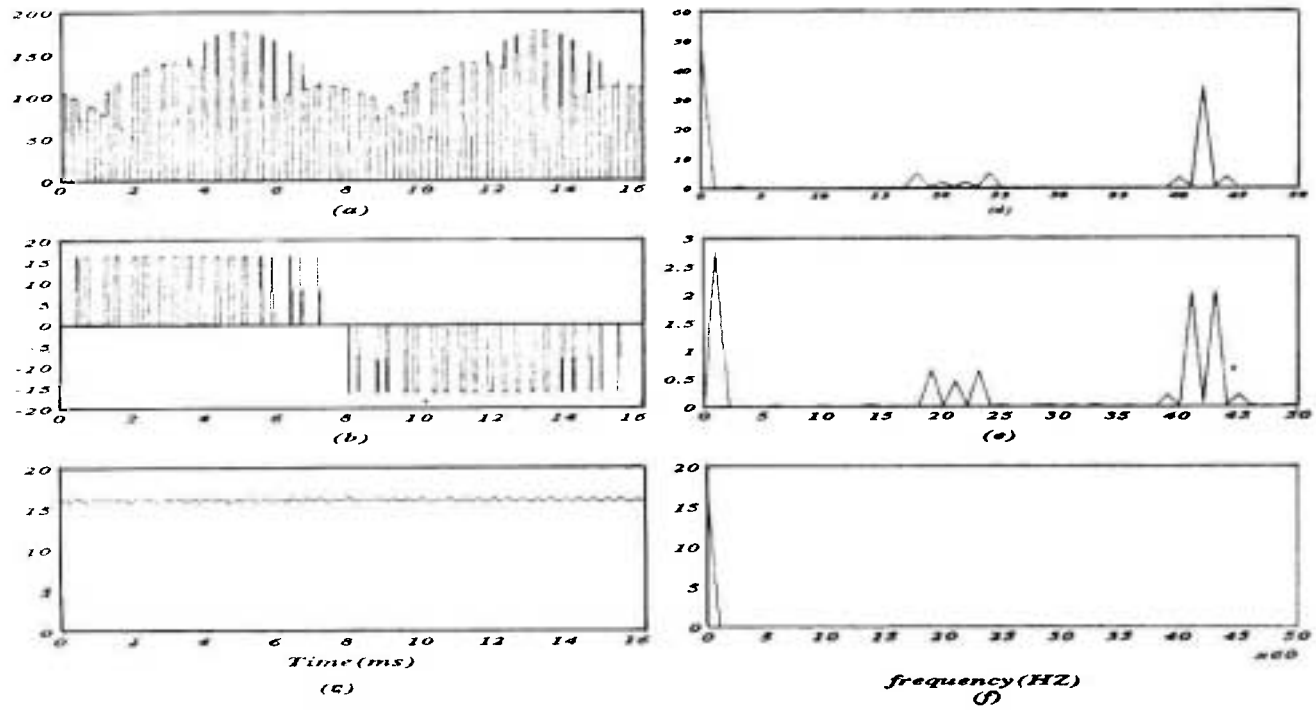

Figure 6. Input/output waveforms of the converter with proposed unbalance correction method. **(a)** output voltage. **(d)** output voltage spectrum. **(b)** input current. **(e)** input current spectrum. **(c)** output current. **(f)** output current spectrum.

input/output waveforms and their spectrums, without unbalance correction and with the proposed unbalance correction technique are shown in Figures 5 and 6, respectively. The presence of a 2nd order abnormal harmonic in the output voltage and current spectrums and a third order abnormal harmonic in the input line current spectrum without unbalance correction are clearly evident. Also as is seen from the spectrums of the input/output waveforms of the converter with proposed unbalance correction method, there is no low order harmonics below the switching frequency.

Dynamic Results

To examine the performance of the proposed unbalance correction scheme under dynamic operation, an input line disturbance was applied to the system in Figure 4 at 16.6ms resulting in a 20% unbalance after the disturbance. The simulation result of the load voltage (Figure 7) shows that the

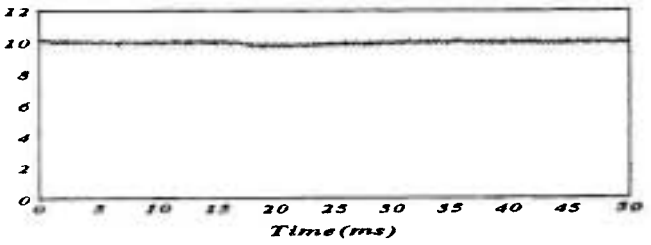

Figure 7. Load voltage for %20 input disturbance at 16.6 ms.

disturbance to the load has been kept to the minimum, also 2nd order harmonic has been suppressed and the load voltage is regulated.

To investigate the performance of the unbalance correction method under reference change we consider %60 reference step down and then %60 reference step up. The simulation results for these two cases with the %20 unbalance in the supply voltage, are shown in Figure 8. Again we notice that there is no low order harmonic before and after the reference change. These results show that with using an additional load feedback loop for

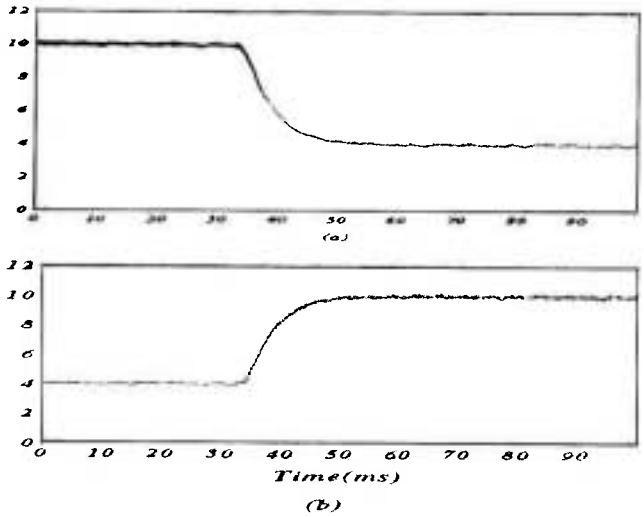

Figure 8. Dynamical results of load voltage. (**a**) %60 step down. (**b**) %60 step up.

load-regulation, the performance of unbalance correction is not affected.

CONCLUSION

In this paper an NN implementation of a simple feedforward method to improve the performance of a PWM AC to DC converter under unbalanced operating condition is presented. It has been shown that in this approach there is no need for positive/negative sequence component calculation and the transfer matrix is expressed directly in terms of the instantaneous three input phase voltages. By using an NN for gating signal generation, the accuracy and the reliability of the converter and the speed of the response are increased.

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