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Design and Analysis of Symmetrical Dual Gate Tunnel Field Effect Transistor with Gate Dielectric Materials in 10nm Technology

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ABSTRACT

In this work, a Symmetrical Dual Gate Tunnel Field Effect Transistor (SDGTFET) is proposed with gate dielectric materials in 10nm technology. The electrical performance parameters of this proposed device are investigated using technology computer aided design (TCAD) simulator. The new SDGTFET employing with high-k dielectric material such as hafnium oxide (HfO_2) and interfacial layer (IL). The 2nm HfO_2 with 30 dielectric constant is used between the interfacial layer and the metal gate on both sides of the device. The variation of the drain current with the varying of gate length, effective gate materials and effective oxide layer thickness of the device is evaluated in this work. By optimizing the proposed device with gate dielectric material the on current gets ~4.2 times enhanced and the averaged subthreshold swing (SSavg) becomes reduced from 90.2 mV/dec to 53.8 mV/dec. Therefore, the SDGTFET structure has better performance than single material and double material TFET and shows a lower ambipolar current and a better on current to off current ratio.

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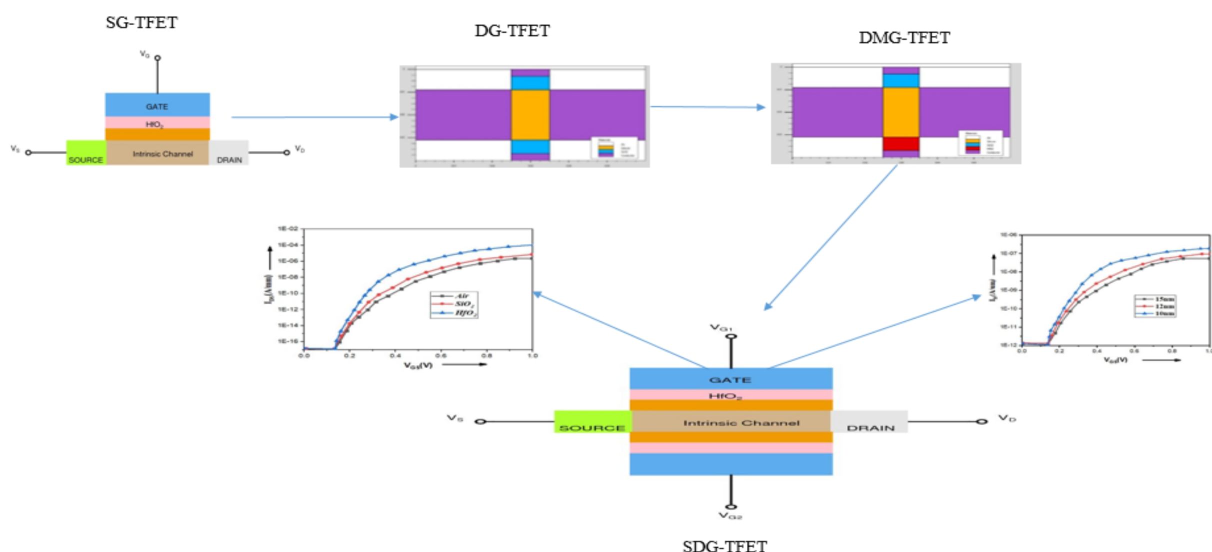
Graphical Abstract



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1. INTRODUCTION

An advanced Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) represents a pivotal innovation in the realm of semiconductor technology, revolutionizing the design and functionality of electronic devices (1). MOSFETs are fundamental building blocks of modern integrated circuits, and advancements in their structure and materials have been crucial for achieving higher performance, increased energy efficiency, and enhanced miniaturization in electronic systems. The traditional MOSFET consists of a metal gate, an insulating silicon dioxide layer, and a semiconductor material, such as silicon. The advanced MOSFET has innovations beyond the conventional design, such as the integration of high-k dielectric material being hafnium oxide (HfO_2), Titanium dioxide (TiO_2) and low-k dielectric material being silicon dioxide (SiO) and novel materials to overcome challenges associated with scaling down transistor dimensions (2). This shift is driven by the need to reduce the thickness of the gate oxide layer, a critical component in MOSFETs, to maintain control over the flow of electrical current while avoiding leakage current in the device. High-k dielectrics enable the creation of physically thinner gate oxides, allowing for better electrostatic control and improved transistor performance in semiconsuctors (3). The pursuit of smaller transistor sizes has led to the development of Fin Field-Effect Transistor (FinFET) and nanowire advanced transistor architectures. These three-dimensional structures provide better control over the flow of electrons, mitigating short-channel effects and allowing for continued transistor scaling. Advanced MOSFET technology is integral to the progress of semiconductor manufacturing processes, enabling the creation of more powerful and energy-efficient electronic devices. As semiconductor research and development continue to evolve, the exploration of new materials, advanced transistor architectures, its performance and innovative manufacturing techniques will further shape the landscape of advanced MOSFETs, influencing the capabilities and efficiency of future electronic systems (4).

The Advanced Tunnel Field-Effect Transistor (TFET) represents a cutting-edge development in semiconductor technology, pushing the boundaries of traditional transistor design to overcome challenges related to power consumption and performance scaling (5). As an innovative electronic device, the TFET devices leverages quantum mechanical tunneling phenomena to facilitate low-power operation, making it a promising device for applications demanding high energy efficiency and improved transistor scaling (6). In contrast to MOSFETs, TFETs exploit the quantum tunneling effect, allowing electrons to pass through a thin barrier without the need for high thermal energy (7). This unique an improved characteristic enables TFETs to operate at lower voltage levels, resulting in reduced power consumption and improved overall energy efficiency. The adoption of TFETs is particularly significant in the context of power-constrained devices, such as those used in portable electronics and low-power Internet of Things (IoT) applications (8). The TFET design often incorporates materials with a narrow bandgap, enabling efficient quantum tunneling. The concept is especially relevant for addressing challenges associated with conventional MOSFETs as they approach the physical limits of scaling down in size (9). TFETs provide an alternative path to continue the advancement of transistor technology by mitigating issues like subthreshold swing, which affects the energy efficiency in small-scale nano transistors. As semiconductor research and development progress, the exploration of advanced TFET architectures, materials, and fabrication techniques continues. Engineers and researchers are working to optimize TFET designs for mainstream integration, considering factors such as manufacturability, reliability, and compatibility with existing semiconductor processes and analysis (10). The continuous evolution of TFET technology holds the promise of revolutionizing the landscape of low-power electronics, enabling the development of energy-efficient devices that are crucial for the future of computing and communication systems (11).

The dielectric constant SiO_2 depends on various factors, including the crystalline structure, temperature, and frequency of the applied electric field. This material is commonly used as a dielectric material in the semiconductor industry, the dielectric constant is typically around 3.9 (12). The dielectric constant of SiO_2 is relatively low compared to other dielectric materials. The lower dielectric constant helps in minimizing the capacitive coupling between adjacent conductive structures in integrated circuits (13). However, as semiconductor devices have scaled down in size, there are challenges associated with increasing capacitance and reducing leakage currents. This has led to the exploration of alternative high-k dielectric materials, such as hafnium dioxide (HfO_2), to address these challenges in advanced semiconductor technologies (14).

The HfO_2 is a metal oxide that is used as a dielectric material in the nano scale devices and manufacturing of advanced semiconductor devices, particularly in the fabrication of modern integrated circuits (15). The dielectric constant is a measure of a materials ability to store electrical energy in an electric field. The dielectric constant of HfO_2 is typically in the range of 20 to 30, depending on factors such as the specific crystalline phase, the method of deposition, and the conditions of the fabrication process. This value is higher than the dielectric constants of conventional SiO_2, which has historically been used as a high-k dielectric material in semiconductor devices. The use of HfO_2 as a high-k

dielectric is motivated by the need to reduce the physical thickness of the dielectric layer while maintaining a high capacitance to improve the overall performance of transistors in integrated circuits (16). High-k dielectrics are employed to overcome the limitations of traditional silicon dioxide in terms of thickness scaling and leakage current in advanced semiconductor technologies.

The Titanium dioxide (TiO_2) is another material that is often used as a dielectric in various applications. The dielectric constant or relative permittivity of TiO_2 can vary depending on factors such as the crystalline phase, temperature, and frequency of the applied electric field. The crystalline form of TiO_2, which is rutile, the dielectric constant is typically around 85. Anatase and brookite are two other crystalline phases of TiO_2, and they may have different dielectric constants. It's important to note that the dielectric constant can vary with the frequency of the electric field (17).

One of the common challenges in TFET emerging technology is the limited experimental validation. Many researchers might rely on simulations and theoretical models, and experimental verification might be lacking. Filling this gap requires more efforts in fabricating and characterizing SDGFET devices to validate the theoretical predictions and understand real-world performance for low power applications. The selection of materials is crucial in semiconductor device design. The literature may not fully explore the variety of materials that could enhance the performance of advanced TFET devices. Researchers could explore new material combinations such as high-k dielectric materials such as HfO_2 and TiO_2 to improve its overall device performance and reduce leakage current. The literature extensively cover the challenges associated with the fabrication processes for TFETs. Addressing this gap involves optimizing fabrication techniques and advanced to ensure reproducibility, scalability, and manufacturability in nanometer technology not behind 22nm. The SDGTFET is designed for low-power applications, the literature comprehensively explore the trade-offs between power consumption and performance metrics such as speed. Addressing this gap requires a balanced approach to optimizing device parameters for specific applications in nanometer technology.

The SDGTFET has gained attention in the realm of semiconductor devices is characterized by its unique dual-gate structure. It consists of two gates, each influencing the flow of charge carriers in the transistor and the symmetrical design allows for enhanced control over the transistor's behavior. The traditional TFET, the SDGTFET relies on quantum tunneling for carrier transport and tunneling occurs through a thin barrier, enabling low-power operation. The primary advantage of SDGTFET is their potential for extremely low-power operation due to the reliance on tunneling. The symmetrical dual-gate design provides improved control and flexibility in tuning the transistor's characteristics. Optimizing fabrication processes and ensuring the process of compatibility with nano structures to existing advanced semiconductor manufacturing techniques are critical for TFET practical applications. Therefore, SDGTFET device is a unique approach to low-power semiconductor devices, leveraging a unique dual-gate structure and quantum tunneling principles.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Two dimensional structure of SDGTFET with high-k gate dielectric material and interfacial layer as shown in Figure 1. The 10nm scale, conventional TFET design face challenges such as increased leakage currents and quantum effects (18). The SDG TFET, with its enhanced symmetrical dual gate architecture, offers a potential solution by providing better control over the electrostatic field. The high-k gate dielectric materials such as HfO_2 is employed for achieving optimal performance at 10nm scale. High-k dielectrics are particularly important in reducing leakage currents and enhancing gate control. The integration of advanced dielectric materials ensures that the SDG TFET can operate efficiently while maintaining a low power footprint (19). The proposed device plays a pivotal role in improving device characteristics. The design allows for a more uniform electric field distribution and tunneling barrier thickness and distance. This architecture is beneficial in achieving better ON/OFF current ratios, which are crucial for low power applications. The 10nm scale SDG TFET leverages tunneling as its fundamental mechanism of operation (20). The symmetrical gates help in optimizing tunneling processes, ensuring reliable and efficient charge through the channel and this 10nm SDG TFET is to enhance power efficiency. The combination of the symmetrical dual gate (SDG) architecture and advanced gate dielectric materials contributes to lower leakage

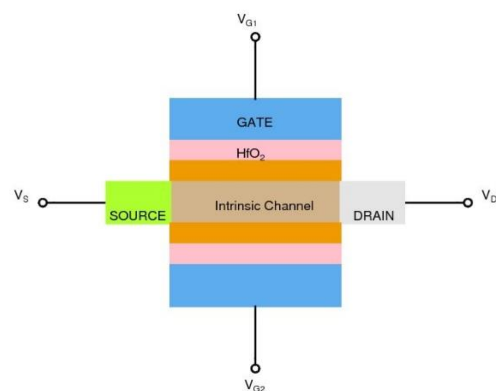

Figure 1. Proposed SDGTFET in 10nm regime

currents, reduced power consumption, and improved overall energy efficiency (21).

Designing a SDG TFET with advanced gate dielectric materials using Technology Computer-Aided Design (TCAD) involves a comprehensive process that encompasses simulation, analysis, and optimization. TCAD tools provide engineers with a virtual environment to model and simulate semiconductor devices (3).

The SDGTFET under consideration makes use of simulation parameters as shown in Table 1. Various models and methods are applied for the simulation, employing the TCAD tool, as outlined in Tables 2 and 3.

TABLE 1. Utilized Parameter for the simulation of SDGTFET

Utilized Parameters	Values
Thickness of HfO_2	2nm
Metal Gate-1 Work Function(W_F)	4.8eV
Metal Gate-2 Work Function(W_F)	4.8eV
Device Length(W_L)	60 nm
Gate Length(L_G)	10 nm
Source Length(L_S)	25nm
Drain Length(L_D)	25nm

TABLE 2. Models used for the device

Model	Description
conmob	Specifies the mobility concentration and dependency
fldmob	Calculation of all the device field dependency
evsatmod=1	implements the carrier concentration and temperature mobility
hcte.el	to enable electric field energy balance for electrons for relaxation time
taurel.el	specifies the relaxation time in the energy balance
taumob.el	specifies the relaxation time for electrons in the temperature dependency

TABLE 3. Methods used for the device

Method	Description
newton	specifies the solution method
maxtrap	used as trap procedure
autonr	used to increase the speed of newton solution method
dvlimit	used as maximum magnitude
nblockit	used as the block iterations

The different design parameters to optimize the performance of SDGTFET. This could include varying the dimensions of the device in nanometer dimensions, doping concentrations, and material properties. Investigate the impact of different semiconductor materials on the device performance. Compare and analyze the characteristics of SDGTFET based on various materials, such as silicon, III-V compounds. The noise analysis to understand the impact of noise sources on the device performance. This can involve studying the thermal noise, flicker noise, and other sources that affect the signal integrity. The power consumption characteristics of the Symmetrical Dual Gate TFET under different operating conditions. Analyze the device performs in terms of energy efficiency and power dissipation. The temperature dependence of the Symmetrical Dual Gate TFET. To understand the device behaves at different temperature ranges and explore potential strategies for temperature compensation.

3. RESULTS AND DISCUSSION

The analysis of Id (drain current) versus Vgs (gate-source voltage) for a SDGTFET with different gate dielectric materials involved for the proposed device characteristics under varying gate voltages. SDGTFET are promising device for low-power applications due to their ability to achieve sub-threshold swing values below the limit of conventional TFET (22, 23). One of the critical parameters to analyze is the sub-threshold swing, which is a measure of the SDGTFET ability to turn on and off efficiently. A lower SS value indicates better improved performance in in the device. The threshold voltage changes with different gate dielectric materials. Vth is the gate voltage at which the device starts conducting. It's essential for determining the operating region of the TFET (24). To analyze the drain current (Id) varies with different gate-source voltages. This shows the on-state behavior of the TFET as shown in Figure 2. A high Ion/Ioff ratio indicates better switching behavior and power efficiency of the proposed device (25, 26). The proposed tunneling device, the tunneling current should be a dominant factor. Analyze the impact of gate dielectric materials such as high-k HfO_2 on tunneling mechanisms and their influence on device performance.

The drain current (Id) versus gate-source voltage (Vgs) characteristics for a SDGTFET with variation of different technology regimes as shown in Figure 3 and investigate the proposed device characteristics scale with 10nm, 12nm and 15nm nodes (27). The 10nm node are scalable to smaller technology nodes for the limitations associated with scaling factor. The dynamic power consumption of SDGTFET during switching events and

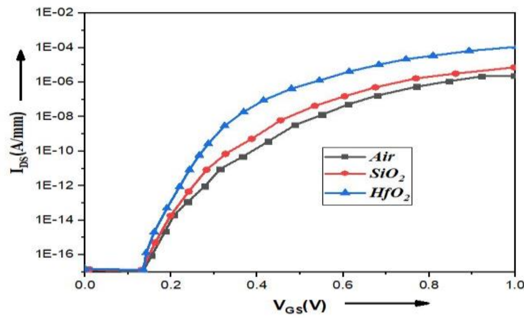

Figure 2. Characteristics of drain current and Gate voltage with dielectric materials

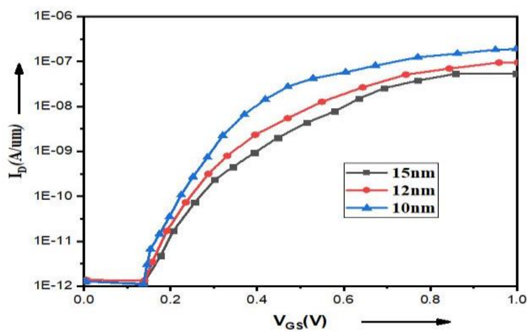

Figure 3. Characteristics of drain current and Gate voltage with different technolgy node

static power consumption in the off-state are reliable in 10nm regime. The performance of the SDGTFET with gate dielectric materials and technology nodes has improved compared to conventional TFET and double gate TFET (28).

The drain conductance (Gd) of SDGTFET is the derivative of the drain current (Id) with respect to the drain-source voltage (Vgs). In the characteristics of a SDGTFET with gate dielectric materials, the analysis of drain conductance involves the conductance varies with different parameters, such as improved gate voltages, gate dielectric materials, and bias conditions (29). The high-k gate dielectric materials influences the drain conductance at Vgs= 1v. Different dielectric materials such as high-k and low-k dielectric materials can affect the tunneling characteristics and, consequently, the conductance of the device. The sub-threshold region of this TFET is transitioning between the off and on states. A steep sub-threshold region and low drain conductance in the off state are desirable and shown in Figure 4.

Transconductance plays a critical role in understanding and characterizing the behavior of this proposed SDGTFET devices, and it is an essential concept in amplifier design, digital signal processing, and analog electronics (30). This characteristic is a measure of how much the output current of a device, changes in

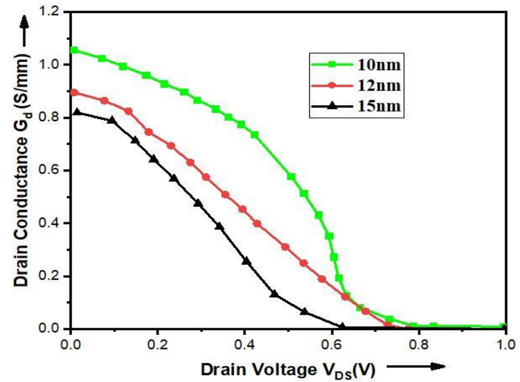

Figure 4. Characteristics of drain conductance with different technolgy node

the input voltage applied to it and it is a key factor in determining the gain and linearity of the device as it influences how effectively an electronic components can amplify an input signal. In the proposed devices, it characterizes the relationship between the input voltage and the output current when operating in the amplification or active mode. It is used to design and optimize the performance of electronic devices, ensuring they operate efficiently and accurately as shown in Figure 5.

The on resistance (Ron) is to determining the power dissipation and efficiency of a TFET. It is essentially the resistance by the current flowing between the drain and source terminals when the TFET is conducting. Ron is a static resistance that represents the resistance of the TFET in the on-state. It is typically defined as the voltage drop across the device divided by the drain current when the device is in the on-state as shown in Figure 6.

The enhanced Ion and Ioff, performance parameters of proposed device related to material and technology as shown in Tables 4 and 5. The Gm and Gd calculated parameters are shown in Tables 6 and 7. The performance parameter comparision of proposed device with existed devices are shown in Table 8.

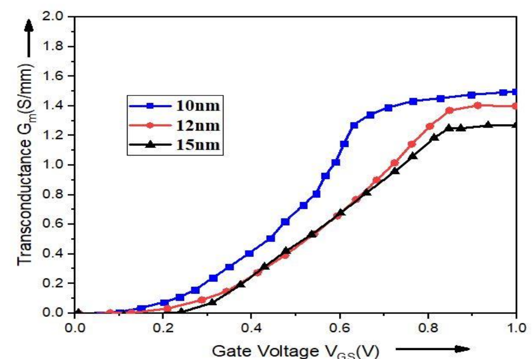

Figure 5. Characteristics of transconductance with different technolgy node

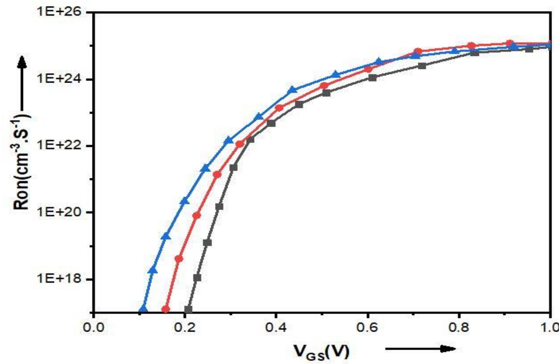

Figure 6. On resistance characteristics with different technolgy node

TABLE 4. On current and off current for different dielectric materials

Materials	Ion(A/μm)	Ioff(A/μm)	Ion/Ioff
Air	$10e^{-05}$	$10e^{-15}$	$10e^{+12}$
SiO_2	$10e^{-5}$	$10e^{-16}$	$10e^{+11}$
HfO_2	$10e^{-3}$	$10e^{-17}$	$10e^{+12}$

TABLE 5. On current and off current for different technology node

Technology (nm)	Ion (A/μm)	Ioff (A/μm)	Ion/Ioff
10	$10e^{-06}$	$10e^{-12}$	$10e^{+06}$
12	$10e^{-07}$	$10e^{-11}$	$10e^{+05}$
15	$10e^{-08}$	$10e^{-11}$	$10e^{+03}$

TABLE 6. Transconductance for different technology node

Technology (nm)	Gm (S/mm)
10	1.62
12	1.51
15	1.39

TABLE 7. Drainconductance for different technology node

Technology (nm)	Gd (S)
10	1
12	0.89
15	0.88

TABLE 8. Performance Parameters Comparision of SDGTFET

Parameters	C TFET	SG TFET	DG TFET	HD-DG TFET	HD-DMG-TFET	SDGTFET (10nm)
Ion(A/µm)	3.12	3.94	4.3	4.6	8.01	9.48
Ioff(A/µm)	9.40	8.99	4.50	4.22	1.34	1.16
Ion/Ioff	1.69	1.70	1.88	1.84	1.9	2.12
Gm(S/mm)	1.34	1.38	1.42	1.46	1.41	3.1
Gd(S/mm)	0.32	0.39	0.419	0.45	0.452	0.71
Ron(Ωmm)	1.41	1.61	1.32	0.88	0.6	0.51

4. CONCLUSION

The SDGTFET configuration has emerged as a promising device for enhancing performance and the limitations of conventional TFET. The symmetrical dual gate TFET exhibits improved subthreshold swing, reduced leakage current and its potential for enhanced operational efficiency compared to traditional device technologies. The impact of different semiconductor materials on the device, highlighting the significance of material selection in optimizing the symmetrical dual gate TFET performance. The investigation encompassed and demonstrated the influence of material properties on device characteristics.Two dimensional structure of Symmetrical Dual Gate Tunnel Field Effect Transistor (SDGTFET) is proposed in this work. The proposed device formed by high –k gate dielectric gate dielectric material being Hafnium oxide (HfO_2). The electrical characteristics of SDGTFET like drain current, transconductance and drain conductance are calculated with the influence of varied semiconductor materials. The integration of SDG enhances the device's electrostatic control, resulting in improved ON/OFF current ratios and better overall performance. The symmetrical configuration achieving a more uniform electric field distribution and enhancing reliability. The high-k gate dielectric materials is to determining the overall efficiency of the SDGTFET. By exploring and implementing advanced dielectric materials, such as high-k dielectrics, the device can achieve lower leakage currents and improved gate control. The findings of this proposed device contribute significantly to the existing and understanding of the SDGTFET behavior and performance. These insights hold substantial promise for the advancement of semiconductor technology, as they can guide the development of refined designs and optimized utilization of SDGTFET in advanced low power applications.

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Persian Abstract

چکیده

در این کار، یک ترانزیستور اثر میدانی تونل دو دروازه ای متقارن (SDGTFET) با مواد دی الکتریک گیت در فناوری ۱۰ نانومتر پیشنهاد شده است. پارامترهای عملکرد الکتریکی این دستگاه پیشنهادی با استفاده از شبیه‌ساز طراحی به کمک کامپیوتر (TCAD) مورد بررسی قرار گرفته است. SDGTFET جدید از مواد دی الکتریک با k بالا مانند اکسید هافنیوم (HfO_2) و لایه سطحی (IL)استفاده می کند. HfO2 نانومتری با ۳۰ ثابت دی الکتریک بین لایه سطحی و دروازه فلزی در دو طرف دستگاه استفاده می شود. تغییر جریان تخلیه با تغییر طول دروازه، مواد موثر دروازه و ضخامت لایه اکسیدی موثر دستگاه در این کار ارزیابی می‌شود. با بهینه سازی دستگاه پیشنهادی با مواد دی الکتریک گیت، جریان روشن ٤.٢ برابر افزایش می یابد و میانگین نوسان زیرآستانه (SSavg) از ۹۰.۲ mV/dec به ٥۳.۸ mV/dec کاهش می یابد. بنابراین، ساختار SDGTFET عملکرد بهتری نسبت به TFET تک ماده و دو ماده دارد و جریان دوقطبی کمتر و نسبت جریان به جریان خاموش بهتر را نشان می‌دهد.