International Journal of Engineering

Journal Homepage: www.ije.ir

Design and Performance Analysis of 6H-SiC Metal-Semiconductor Field-Effect Transistor with Undoped and Recessed Area under Gate in 10nm Technology

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PAPER INFO

Paper history:
Received 20 August 2023
Received in revised form 29 August 2023
Accepted 03 Spetember 2023

Keywords:
Drain Current
Transconductance
Drain Conductance
Subthreshold Slope
High Frequency

ABSTRACT

In this paper, the impact of the undoped and recessed gate structure on the performance of the silicon carbide metal semiconductor field effect transistor is presented. The importance of the silicon carbide metal semiconductor field effect transistor analyzed using technology computer aided design simulations in 10 nanometer technology. The proposed undoped gate structure has minimized ionized impurity scattering, leading to increased electron mobility and improved carrier concentration. Performance metrics such as drain current, transconductance, subthreshold slope, and cutoff frequency were evaluated and compared with conventional silicon carbide metal semiconductor field effect transistor structures. The proposed device exhibits superior current driving capabilities, enhanced transconductance, and reduced leakage currents, leading to improved power efficiency. Moreover, the recessed gate structure contributes to a significant reduction in short-channel effects, making the device more suitable for high frequency applications. The simulation parameters were calculated and compared with conventional structure with the length of the source and drain in 10 nanometer node. Therefore the drain current of this proposed device has been improved by 68%.

***doi**: 10.5829/ije.2023.36.12c.16*

NOMENCLATURE

Sic	Silicon Carbide	*Ion*	On state current
HfO_2	Hafnium oxide	*Ioff*	Off state current
SiO_2	Silicon dioxide	I_d	Drain Current
Gm	Transconductance	*Vgs*	Gate to source voltage
G_d	Drain conductance	*TCAD*	Technology Computer Aided Desisn

1. INTRODUCTION

The fundamental principle of Metal-Semiconductor Field-Eeffect Transistor (MESFET) is based on the modulation of the current flow in a semiconductor channel by an externally applied electric field. This control is achieved through the formation of a ShottkyReporting research finding barrier between the metal gate electrode and the semiconductor channel, enabling the device to act as a voltage-controlled amplifier [1]. In the present semiconductor technology, Silicon Carbide (SiC) has emerged as a revolutionary material due to its unique properties that offer significant advantages over conventional silicon-based devices. Among the various SiC devices, the Silicon Carbide Metal-Semiconductor Field-Effect Transistor (6H-SiC MESFET) stands out as a promising material for High-power and High-frequency applications. 6H-SiC has a wide band gap, which allows the device to operate at elevated temperatures while maintaining stable

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Please cite this article as: A. Krishnamurthy, D. Venkatarami Reddy, E. Radhamma, B. Jyothirmayee, D. Sreenivasa Rao, V. Agarwal, B. Balaji, Design and Performance Analysis of 6H-SiC Metal-Semiconductor Field-Effect Transistor with Undoped and Recessed Area under Gate in 10nm Technology, ***International Journal of Engineering, Transactions C: Aspects***, Vol. 36, No. 12, (2023), 2264-2271

performance [2]. The high thermal conductivity of SiC further ensures efficient heat dissipation, reducing the liability of thermal breakdown at high power level and high band gap level.

In recent years symbolic advancements in silicon carbide (6H-SiC) fabrication processes have allowed for the realization of smaller feature sizes and more complex device structures [3]. As a result, 6H-SiC MESFETs have seen continuous improvement in their performance characteristics, making them even more attractive for cutting-edge electronic systems. Moreover, the absence of reverse recovery losses in SiC devices in silicon-based devices, leads to lower switching losses and improved energy efficiency. This makes 6H-SiC MESFETs highly desirable for power amplifier applications, where minimizing losses is critical to achieving high power efficiency [4, 5]. The 6H-SiC MESFET represents a semiconductor device with exceptional material properties and its unique advantages, such as high electron mobility, wide band gap, and excellent thermal conductivity, make it an attractive one for modern electronic systems demanding superior performance and energy efficiency.

Metal semiconductor field effect transistor (MESFET) has played a crucial role in various applications, ranging from low-noise amplifiers to high-frequency communication systems [6]. To enhance the performance of MESFETs, designers have been exploring innovative design approaches [7]. One such approach involves the integration of an undoped and recessed area under the gate region, which has shown promising potential for improving device characteristics. By eliminating dopants from the gate region, ionized impurity scattering is reduced, resulting in higher electron mobility and improved carrier concentration. Furthermore, the recessed gate architecture provides precise control over the gate-to-channel distance, mitigating short-channel effects and enhancing gate control over throughout the channel [8].

The MESFET operates based on the modulation of the conductivity of a semiconductor channel between the source and drain regions by the voltage applied to the gate electrode [9]. The metal gate forms a Schottky barrier, controlling the flow of charge carriers, and electrons in the case of n-channel MESFETs through the channel. The undoped feature involves intentionally leaving the gate region free of dopants, avoiding the introduction of ionized impurities that can cause scattering and reduce carrier mobility [10]. Additionally, the incorporation of a recessed gate area provides the opportunity to achieve better control over the gate-to-channel distance. This control is essential for minimizing short-channel effects, which become more pronounced as transistor dimensions are scaled down. By effectively reducing short-channel effects, the proposed design can improve the device's subthreshold characteristics and mitigate issues related to device design miniaturization.

One of the major challenges in designing SiC MESFETs is reducing the detrimental effects of dopants in the gate region. Dopants can lead to ionized impurity scattering, degrading the device's electron mobility and overall performance. To overcome this limitation, we proposed an undoped gate structure, where the gate region remains free of any doping materials, thus minimizing scattering effects and enhancing electron mobility.

The second section presented the proposed device and utilized parameters. The result and discussions of drain current characteristics are presented in the third section. The conclusion is presented in the final section.

2. STRUCTURE OF PROPOSED DEVICE

The design of a 6H-SiC metal-semiconductor field-effect transistor (MESFET) with an undoped and recessed gate structure using 10nm technology to explore the potential benefits of advanced semiconductor manufacturing processes combined with innovative gate engineering. The proposed undoped gate structure has minimized ionized impurity scattering, leading to increased electron mobility and improved carrier. The device consists of a silicon carbide substrate that acts as the foundation for the entire device, providing a robust and thermally conductive material to support the active region. Figure 1 illustrates the proposed 6H-SiC device.

Source and drain regions are heavily doped to facilitate efficient carrier injection and extraction, ensuring low contact resistance [11, 12]. The channel region lies between the source and drain regions and is responsible for carrying the majority of carriers. The gate region comprises a metal contact on the 6H-SiC surface. In this design, the gate is intentionally left undoped, free of any ionized impurities, to enhance carrier mobility [13]. A precisely engineered recessed area is created under the gate region to optimize the gate control and reduce short-channel effects. The undoped gate design to minimize ionized impurity scattering, which can significantly impact the electron mobility in traditional doped-gate MESFETs. By avoiding dopants in the gate region, the device benefits from enhanced electron

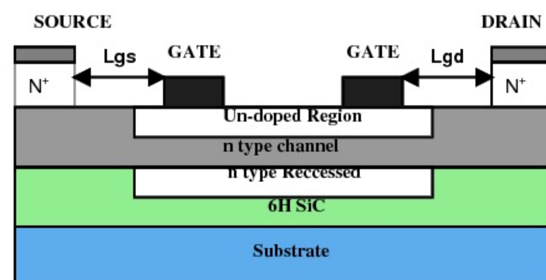

Figure 1. Proposed 6H-SiC device

mobility and improved current conduction. The recessed area under the gate allows for better control of the gate-to-channel distance. This design feature is critical for mitigating short-channel effects, such as drain-induced barrier lowering (DIBL) and subthreshold swing degradation. Precise control over the gate-to-channel distance enables improved gate control and better device performance is shown in Figure 1 compared to the conventional structure [14].

The device is designed using cutting-edge 10nm technology, which enables smaller feature sizes and advanced process techniques [15, 16]. This technology node provides enhanced gate control, reduced parasitic capacitances, and improved gate dielectric properties, enabling superior high-frequency capabilities and power efficiency.

The proposed device compared with conventional MESFET structure is shown in Figure 2.

The proposed 6H-SiC MESFET with an undoped and recessed area in 10nm node utilized the different parameters for the simulation as shown in Tables 1 and 2. Tables 3 and 4 represent the values of Ion and Ioff current, for different values of length of source and drain.

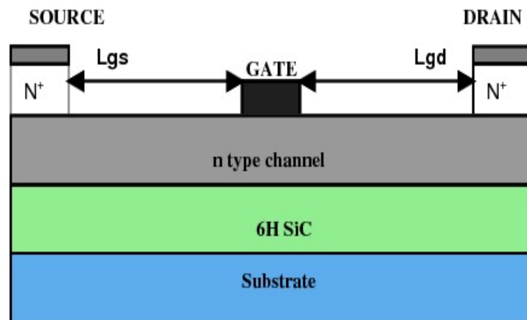

Figure 2. Conventional MESFET

TABLE 1. Used parameter for the proposed MESFET

Parameter	Proposed device
Length of device (W_L)	60 nm
Gate Length (L_G)	10 nm
Source Length (L_S)	30 nm
Drain Length (L_D)	30 nm
Channel Length (L_C)	10 nm
Doping of Source (D_S)	$1x10^{18}$ cm^{-3}
Doping of Drain (D_D)	$1x10^{19}$ cm^{-3}
Doping of Channel (D_C)	$1x10^{20}$ cm^{-3}
Work Function (W_F)	4.8eV
Thickness of SiC	2nm
Oxide thickness	3nm

TABLE 2. Ion and Ioff currents of proposed device

Architecture	I_{OFF} (A/μm)	I_{ON} (A/μm)	I_{ON} /I_{OFF}
C-MESFET	1.11E-09	4.02E-04	2.12E+04
Ls	2.02E-10	3.10E-04	3.01E+04
Ld	2.11E-10	3.12E-04	1.121E+05
Proposed device	3.17E-10	3.10E-04	4.11E+06

TABLE 3. Ion and Ioff currents of proposed device at Ls and Ld

Architecture	I_{OFF} (A/μm)	I_{ON} (A/μm)	I_{ON}/I_{OFF}
Ls	5.19E-11	4.02E-04	5.01E+06
Ld	3.11E-10	4.11E-04	3.19E+05
Proposed device	2.10E-09	5E-03	2.191E+04

TABLE 4. Ion and Ioff currents of proposed device at doping

Architecture	I_{OFF} (A/μm)	I_{ON} (A/μm)	I_{ON}/I_{OFF}
$1x10^{16}$ cm^{-3} - Source	1.10E-10	3.12E-04	1.12E+05
$1x10^{17}$ cm^{-3} - Drain	1.21E-10	3.18E-04	2.78E+05
$1x10^{18}$ cm^{-3} -Channel	3.19E-10	2.98E-04	3.80E+06

The recessed gate architecture allows for precise control over the gate-to-channel distance, effectively reducing short-channel effects [17]. This improved gate control enhances the device's overall performance and stability. The combination of the undoped gate and recessed structure contributes to higher power efficiency in the 6H-SiC MESFET [18]. The reduction in short-channel effects and improved electron mobility result in lower power dissipation, making it suitable for power-sensitive applications [19].

The incorporation of an undoped and recessed region beneath the gate introduces a novel structural modification to the traditional MESFET design. This alteration has the potential to significantly impact device performance with key limitations of conventional MESFET. The undoped and recessed gate design can substantially lower gate-source and gate-drain capacitances. This reduction in capacitance enhances the device's high-frequency operation, making it well-suited for high frequency applications with low power consumption, and high-speed signal processing. This includes fields such as wireless communication, radar systems, and high-frequency electronics. The proposed device concept paves the way for further research and development and can explore various design variations and optimize parameters to extract even more performance benefits from the undoped and recessed gate structure.

3. RESULTS AND DISCUSSIONS

3. 1. Drain Current Characteristics

The drain current vs. drain voltage characteristic of 6H-SiC represents the relationship between the drain current (Id) flowing through the device and the drain voltage (Vds) applied across the drain and source terminals [20]. Compared to conventional SiC MESFETs, the 6H-SiC MESFET with the undoped and recessed gate design is exhibited higher drain currents for a given drain voltage. The absence of dopants in the gate region reduces ionized impurity scattering, leading to enhanced electron mobility and improved carrier concentration. As a result, the device can achieve higher drain currents at different oxide thickness as shown in Figure 3. The Id-Vds curve shows a more saturation behavior for the proposed MESFET design. With the undoped and recessed gate structure, the short-channel effects are reduced, leading to improved gate control and saturation behavior. This allows the device to operate more efficiently in the saturation region, providing better linearity and stability. The undoped gate structure reducing subthreshold leakage currents. In subthreshold operation, the absence of dopants in the gate region minimizes off-state leakage, leading to improved power efficiency. The Id-Vds curve will handle higher output currents while maintaining low on-resistance [11, 21].

The recommended and typical transistors function in depletion mode, where the highest drain current occurs when the gate voltage is zero. As a result, their peak currents were compared at this point. In a new design, the gate-channel bias causes depletion at the upper region of the channel. This bias prompts carriers to move at the channel's lower region, facilitating the flow of drain current. Consequently, the lower end channel area will significantly influences drain current flow. In the new design, introducing a channel into the p-buffer layer increases the thickness of the lower silicon channel area. This augmentation boosts electron concentration and mobility in this region, thereby enhancing drain current region.

3. 2. Gate to Source Capacitance

The gate to source capacitance (Cgs) is a critical parameter that characterizes the capacitive coupling between the gate and source terminals of proposed 6H-SiC MESFET [22, 23]. It plays a significant role in determining the high-frequency performance of the device, as it directly impacts the device's switching speed and overall signal handling capabilities. By eliminating dopants in the gate region, the depletion region width is minimized, leading to lower capacitance between the gate and the channel. This reduction in gate capacitance results in improved high-frequency performance. The Cgs vs frequency curve show a more frequency response for the 6H-SiC MESFET with the undoped and recessed gate structure. The recessed gate design enables precise control over the gate-to-channel distance, mitigating short-channel effects and minimizing parasitic capacitances. As a result, the device can maintain a lower Cgs value over a broader frequency range shown in Figure 4.

The suggested configuration of the transistors alters their electrical characteristics, affecting parameters like gate-source and gate-drain capacitors. Modifications in the electric charge distribution beneath the gate on the source side cause variations in the gate-source capacitor, while changes on the drain side induce adjustments in the gate-drain capacitor. Consequently, by implementing structural alterations in these transistors, it becomes possible to decrease the charge accumulation in these regions, subsequently reducing the capacities of both gate-source and gate-drain capacitors. Introducing nondoped regions beneath the gate of the proposed transistor contributes to decreased gate capacitance, consequently enhancing the speed of the transistor and improvement in the performance.

3. 3. Gate to Drain Capacitance

The proposed undoped and recessed gate structure is resultant in reduced gate to drain capacitance compared to conventional MESFETs. The absence of dopants in the gate region leads to a narrower depletion region, reducing the capacitance between the gate and the drain. The Cgd

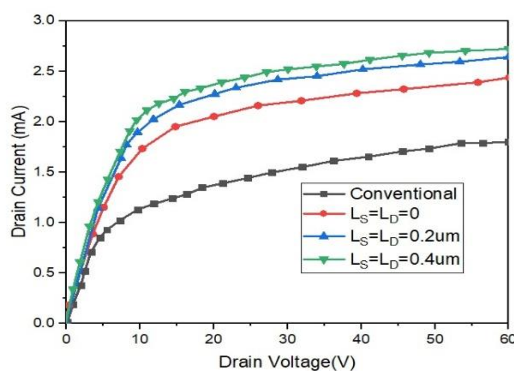

Figure 3. Drain current vs drain voltage Characteristics at different Ls and Ld

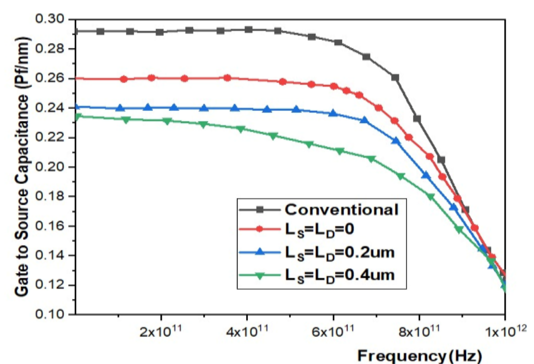

Figure 4. Gate to source capacitance vs frequency at different Ls and Ld

vs frequency shows frequency response for the 6H-SiC MESFET with the undoped and recessed gate structure. The precise control over the gate-to-channel distance achieved by the recessed gate design results in minimized parasitic capacitances, including Cgd. This characteristic allows the device to maintain a lower Cgd value across a wider frequency range. The reduction in Gate-Drain Capacitance is particularly significant in suppressing the miller effect. The miller effect is an undesirable phenomenon in amplifiers, where the Cgd couples with the output capacitance, resulting in signal feedback and potential instability. With the lower Cgd in the proposed MESFET design, the impact of the Miller effect is mitigated, contributing to better amplifier performance as shown in Figure 5.

3. 4. Lateral Electric Field The lateral electric field (E-field) distribution along the channel length of proposed MESFET is essential to analyze the E-field behavior, particularly for short-channel devices, as it directly affects carrier mobility, hot-carrier effects, and breakdown voltage [24, 25]. The undoped gate structure shows a reduction in the lateral electric field compared to conventional MESFETs at different lengths of source and drain. The absence of dopants in the gate region minimizes the potential gradients, leading to a more uniform distribution of the lateral electric field along the channel length. This reduction in E-field is beneficial for maintaining high electron mobility and reducing the impact of hot-carrier effects [26, 27]. The recessed gate design further enhances the reduction of short-channel effects by allowing better control over the gate-to-channel distance. Short-channel effects, such as drain-induced barrier lowering (DIBL) and subthreshold slope degradation, are minimized, leading to improved device performance for short-channel lengths [28]. The reduced lateral electric field in combination with precise gate control results in better subthreshold characteristics and improved transistor behavior. The lateral electric field significantly influences the breakdown voltage of the MESFET. By reducing the lateral electric field, the proposed design can enhance the device's ability to handle high voltages without encountering premature breakdown as shown in Figure 6 [29].

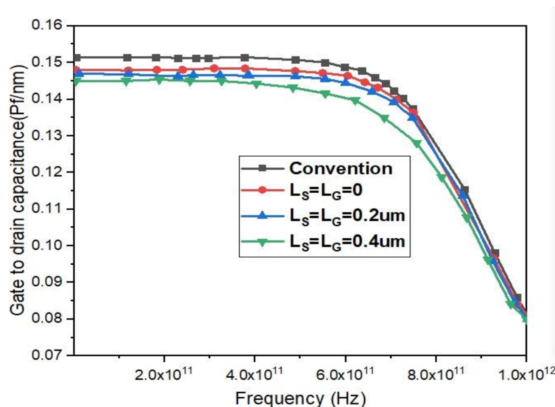

Figure 5. Gate to drain capacitance vs frequency at different Ls and Ld

The proposed structural design has the potential to cause alterations in electrical parameters, particularly in the lateral distribution of the electric field. This is attributed to the fact that the highest electric field strength is typically found at the corner of the gate in close proximity to the drain region. Modifications made to the physical structure in this specific area can result in shifts in the way the electric field is distributed. Conversely, the electric field's strength is directly linked to the impurity carrier concentrations which are the present within the channel region. Furthermore, the breakdown voltage of the device exhibits an inverse relationship with the electric field strength. Consequently, decreasing the impurity concentration beneath the gate, particularly at the drain side, serves to reduce the maximum electric field magnitude. This reduction, in turn, contributes to an increase in the device's breakdown voltage.

3. 5. Output Resistance The output resistance (Ro) is to characterize the small-signal behavior of the proposed MESFET. It represents the change in drain-source voltage (Vds) for a given change in drain current (Id) when the device is operated in its small-signal region [30, 31]. The output resistance plays a very important role in determining the gain and linearity of the device, particularly in amplifier applications. The undoped gate structure and the recessed gate design contribute to an improvement in output resistance compared to conventional MESFETs. The absence of dopants in the gate region leads to reduced scattering effects and higher electron mobility, resulting in better output resistance [32]. The enhanced output resistance contributes to improved linearity in the 6H-SiC MESFET with undoped and recessed gate structure. In amplifier applications, higher output resistance leads to a more linear relationship between the input signal and the output signal, reducing signal distortion and improving the fidelity of the amplified signal. The output resistance has a direct impact on the device's voltage gain. A higher output resistance implies a higher voltage gain for the MESFET as shown in Figure 7.

The output resistance and output conductance share an inverse relationship. Consequently, the output resistance showcases how the drain current's changes relate to alterations in the drain to source voltage reange and gate to source voltages. The performance of the suggested transistor relies on the influence of the drain voltage on drain current. Consequently, lower output conductance values are more desirable, while higher output resistance values are advantageous. In terms of variations in drain voltage, the output resistance is assessed across different Ls (source length) and Ld (drain length) values, with a constant channel thickness of T u

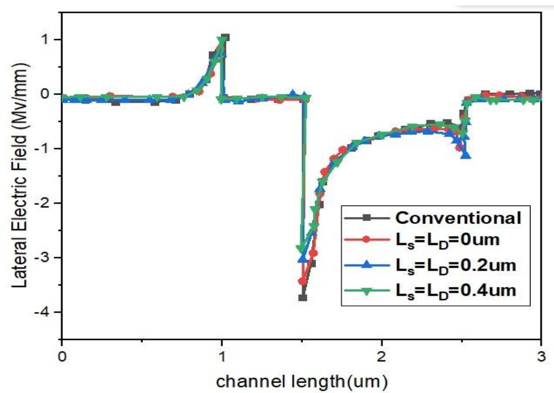

Figure 6. Lateral electric field and channel length at different values of Ls and Ld

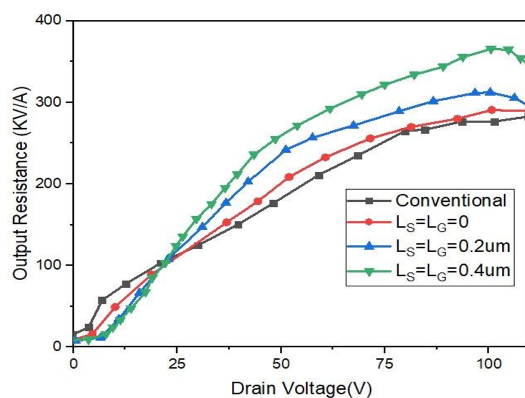

Figure 7. Output resistance vs Drain voltage at various values of Ls and Ld

= 10 nm. Notably, the proposed transistor configuration yields larger output resistance compared to the conventional structure across various combinations of Ls and Ld.

4.CONCLUSION

In this work, we have presented the drain current characteristics of 6H-SiC MESFET with UR region under the gate. The length of channel region is 10nm is considered to reduce peak electric field and improves the breakdown voltage compared to conventional device with various values of Ls and Ld. This structure is invented using silvaco tool and the simulation results of Ion and Ioff substantially increases and decreases. Due to undoped and recessed region with 10nm technology, the drain current of proposed device increases by 68%. The gate to drain capacitance and gate to source capacitance is reduced due to this new structure. The advanced structure is more efficient and suitable for high frequency and high-speed operation.

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Persian Abstract

چکیده

در این مقاله تاثیر ساختار دروازه بدون دود و فرورفته بر عملکرد ترانزیستور اثر میدان نیمه هادی فلزی کاربید سیلیکون ارائه شده است. اهمیت ترانزیستور اثر میدان نیمه هادی فلزی کاربید سیلیکون با استفاده از شبیه‌سازی‌های طراحی به کمک کامپیوتر در فناوری ۱۰ نانومتری تحلیل شد. ساختار دروازه بدون لایه پیشنهادی پراکندگی ناخالصی یونیزه شده را به حداقل رسانده است که منجر به افزایش تحرک الکترون و بهبود غلظت حامل می شود. معیارهای عملکرد مانند جریان تخلیه، رسانایی، شیب زیرآستانه، و فرکانس برش با ساختارهای ترانزیستوری اثر میدان نیمه هادی فلزی کاربید سیلیکون معمولی ارزیابی و مقایسه شدند. دستگاه پیشنهادی قابلیت‌های هدایت جریان برتر، رسانایی افزایش یافته و جریان‌های نشتی را کاهش می‌دهد که منجر به بهبود راندمان انرژی می‌شود. علاوه بر این، ساختار دروازه فرورفته به کاهش قابل توجه اثرات کانال کوتاه کمک می کند و دستگاه را برای کاربردهای فرکانس بالا مناسب تر می کند. پارامترهای شبیه سازی با ساختار معمولی با طول منبع و زهکش در گره ۱۰ نانومتری محاسبه و مقایسه شد. بنابراین جریان تخلیه این دستگاه پیشنهادی ٦٨ درصد بهبود یافته است.