IJE TRANSACTIONS C: Aspects Vol. 36 No. 09, (September 2023) 1618-1625

International Journal of Engineering

Journal Homepage: www.ije.ir

Decimal to Excess-3 and Excess-3 to Decimal Code Converters in QCA Nanotechnology

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PAPER INFO

Paper history:
Received 16 April 2023
Received in revised form 13 June 2023
Accepted 14 June 2023

Keywords:
Quantum-dot Cellular Automata
Excess-3
Decimal
Energy Dissipation
Nanotechnology

ABSTRACT

Nowadays Quantum-dot Cellular Automata (QCA) is one of the new technologies in nanoscale which can be used in future circuits. Most digital circuits are implemented with CMOS technology, but CMOS has some problems like power consumption and circuit size. So, for solving these problems a new method (QCA) is presented. It is clear that converters play a crucial role in the digital world. So, due to the aforementioned point, in this paper, two digital code converters, containing an excess-3 to decimal, and a decimal to excess-3 code converter are presented. The tile method is used to design proposed circuits in quantum-dot cellular automata (QCA) nanotechnology. The tile method gives a unique block for the majority and NOT gates. This property facilitates integration. Both of the proposed code converters have 1.75 clock cycles delay and have an energy dissipation of about 100meV. In the excess-3 code to decimal converter, 516 cells are used, which occupy an area equal to 0.43μm^2 also in the decimal to excess-3 code converter. 321 cells are used, which occupy an area equal to 0.28 μm^2.

***doi**: 10.5829/ije.2023.36.09c.05*

1. INTRODUCTION

Nowadays Quantum-dot Cellular Automata (QCA) is one of the new technologies in the nanoscale which can be used in future circuits [1]. Most digital circuits are implemented with CMOS technology, but CMOS has some problems like power consumption and circuit size [2]. So, for solving the aforementioned problems a new method (QCA) is presented. QCA technology can solve scaling issues and presents high frequency up to terahertz [3]. In 1993, this technology was first introduced by Lent et al. [4].

Systems in digital electronic like digital computers are worked in binary form. So, for working and calculating with this type of system, data should be converted to the right codes, here the importance of code converting is felt, and that's why many code converters like decimal to binary, binary to decimal, decimal to excess-3, excess-3 to decimal, etc. were presented by Gholami et al. [5]. Many ICs convert codes. ICs that are based on transistors have some issues like power dissipation and short-channel effects at very low device sizes [6]. So, utilizing a new method like QCA can be a key step toward solving these problems. Moreover, some methods are presented with the aim of making improvements in the performance of QCA circuits [7]. One of these methods is the tile which is presented by Huang et al. [8]. Tile presents a combined logic function for INV and Majority gates, so the tile method is area efficient because it presents one unique block for INV and Majority gates [9]. Since reducing the occupied area, energy dissipation, and of course, improving the performance is very vital, the technology of integrated circuits was expanded [10-12]. In this paper by using the tile method, two code converters are presented: excess-3 code to decimal (that is the topology of 7443 IC from 74 series IC) and decimal to an excess-3 code. There weren't many papers to present QCA digital code converters, particularly an excess-3 code converter [5], but in the following, some papers about code converters are presented. Raina et al. [9] presented a BCD to seven-segment code. A seven-segment has seven different parts and every part includes a light-emitted diode. This work presents seven circuits for each segment with the gate

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Please cite this article as: F. Fouladinia, M. Gholami, Decimal to Excess-3 and Excess-3 to Decimal Code Converters in QCA Nanotechnology, ***International Journal of Engineering, Transactions C: Aspects***, Vol. 36, No. 09, (2023), 1618-1625

method style. Presenting seven different circuits instead of one circuit is the most important defect of this paper. Kassa et al. [12] presented at first, a full adder (FA); then, with three of that FA, a binary to BCD converter was proposed. This circuit was implemented utilizing the gate method and wasn't optimized as much as possible. Kaity and Singh [13] just like the others, used the gate method and some digital code converters were presented. One of these converters is excess-3 code to the binary that this circuit was implemented with Feynman gate. In this converter, two of the aforementioned gate has been used. Mukherjee et al. [14] proposed a LTEx module with the gate method style in which a two-input LTEx module consisting of 26 cells and 4 clock phases was used to produce outputs. Every LTEx module is a two-input NAND gate with the new structure, then for implementation of 2 to 16 bits binary to gray code converter, this module has been utilized. Karthik [15] presented a simple converter utilizing basic structures of the QCA technology like wire, majority gate, etc. This circuit is converted BCD to excess-3 code and as mentioned before, the gate method is used in this design which has no new idea. You and Jeon [16] designed at first, a majority gate with five inputs is, this majority gate uses 3 clock phases to give an output, then with this majority and the ability to rotate cells in QCA, a BCD to Excess-3 code converter was implemented. As is clear, due to the high number of inputs and outputs in converting decimal to Excess-3 code, this type of converter has not been paid much attention. Therefore, in this paper, the main focus is on designing a decimal to excess-3 and vice versa code converters in QCA nanotechnology. To design the mentioned converters the tile method is utilized with the aim of reducing the size of the circuit and of course, enabling the circuits to be integrated.

2. QCA'S BASIC CONCEPTS

A QCA cell consists of several parts. Two freely moving electrons and four areas are used as wells to trap electrons, known as dots. All of the aforementioned parts are inside a square showing each cell's perimeter. All these cases can be seen in Figure 1. Two valid states can be defined for cells, one is used for logical zero and the other for logical one (known as binary 0 and binary 1 in Figure 1).

One of the advantages of QCA is its very low energy consumption, due to the movement of electrons only inside the cell instead of moving across a conductor like wire, which results in high energy consumption and energy loss. One of the most important gates in this technology is the majority gate, which has the function Maj (A, B, C) = AB + AC + BC, and using it, important gates can be implemented. For instance, AND and OR gates (by setting one of the three inputs as binary 0 for AND gate and binary 1 for OR gate), this gate is shown in Figure 2. As can be seen, five cells are used to implement this gate. Another important gate that is very widely used in the implementation of logic circuits is the inverter gate which is shown in Figure 3. Finally, the wire gate in this technology is presented. This gate is responsible for data transmission and has many applications, as it can be shown in Figure 4.

In QCA, clocking is very important because the simultaneous arrival of the inputs of a gate is very necessary to get the correct answer. As can be seen in Figure 5, in this technology clocking has 4 main phases. The first phase is called the switch, which is the increment of the force that prevents the movement of electrons inside each cell, and the movement of electrons gradually becomes difficult. In the next phase, which is called hold, the forces that prevented the movement of electrons inside each cell, reach their maximum amount and, because of that the location of electrons has remained stable or fixed (This way the cell gets new polarization). In the third phase, called release, the amount of the blocking force will be decreased, and electrons are slowly released. Finally, in the fourth phase, known as relax, the cell has no polarity and electrons will move completely free inside the cell. To apply clocking, it is very important to observe the order of the clock phases, at first, the cells should be in the switch phase(with green color for cells), then hold (purple color), then release (light blue color), And finally, relax

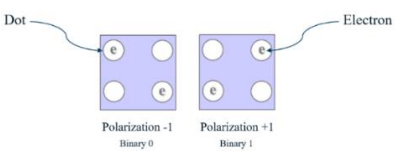

Figure 1. QCA cell and polarization states

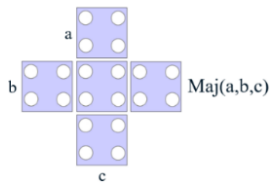

Figure 2. Majority gate in QCA

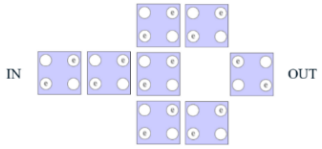

Figure 3. Inverter gate in QCA

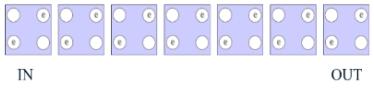

Figure 4. Wire gate in QCA

phase (white color), after a complete clocking cycle, if more phases are needed, second cycle of clocking is started and again clocking is done from the switch phase according to the mentioned method.

Generally, there are several mechanisms for designing and simulating the QCA circuits, the most common method used for design is the gate-based method, and the explanations given are all based on this method. One of the recently used methods to improve circuits is the tile method [8], which is also used in this paper to design and simulate the circuit. As seen earlier, in the gate-based method, there are unique structures for the majority and inverter gates, eliminating the possibility of integrating these circuits, but in the tile-based method, due to the proposed structure, it is possible to integrate the circuit because just one structure is used for both majority and inverter gates. As is shown in Figure 6, a majority gate with three inputs and one output is presented with a tile block. Also in Figure 7, an inverter gate with this method is shown in Figure 8. An example gate is presented that gives $a\bar{b}$ output without any use of an inverter gate.

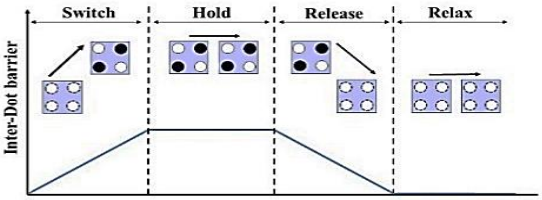

Figure 5. Clocking in QCA

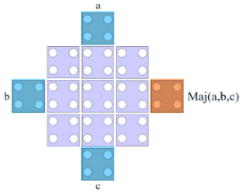

Figure 6. Majority gate in QCA using the Tile method

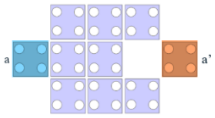

Figure 7. Inverter gate in QCA using the Tile method

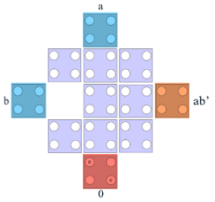

Figure 8. Majority gate in QCA using the Tile method

Also, as it can be seen the inverter gate can be implemented just like the example that is presented in Figure 8. This type of inverter is shown in Figure 9.

In this inverter, in the first place, the invert of input "a" is calculated, then that value is OR with binary "0" or that value is AND with binary "1", both of these calculations have the same results, which is the invert of input "a".

3. PROPOSED DIGITAL CODE CONVERTERS IN QCA CIRCUITS

In this section, two digital converters with tile method are proposed, excess-3 code to decimal and decimal to excess-3 code. At first, a logical circuit for the excess-3 code to decimal converter is presented, then an equivalent circuit for this converter with tile method is given, next step the QCA circuit of the excess-3 code to decimal converter is given, In the following all the mentioned steps for the second converter namely decimal to excess-3 code are presented. To explain about differences between the general and the tile method let's take the NAND gate as a sample. One of the ways to implement this widely used gate there is a need for a common majority gate plus an inverter gate which means there is a need for 16 cells and 3 phases of the clock for implementing a NAND gate. But if the implementation will be done utilizing the tile method there is a need for 12 cells with just 2 phases of the clock, so it's clear that utilizing new methods like the tile method can be a key step toward decreasing the size and of course, the latency of the designed circuit.

3. 1. Proposed Excess-3 to Decimal Converter

74 series ICs are very popular, widely used, and have many educational, research, and industrial uses. One of these ICs is 7443, which converts excess-3 code to decimal. The internal circuit of this IC can be seen in Figure 10. Also, the truth table of the aforementioned IC is given in Table 1.

As it is seen, this IC includes 4 inputs for the excess-3 numbers and ten outputs for the decimal numbers, ten NAND gates with four inputs and eight NOT gates are used in this circuit. As mentioned, the goal is to implement the circuit in Figure 10. with the tile method in QCA technology. For this purpose, NOT and NAND

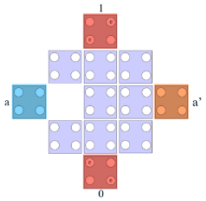

Figure 9. Inverter gate in QCA using the Tile method

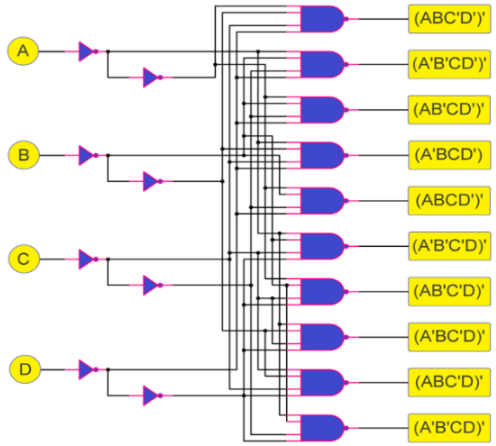

Figure 10. 7443 IC internal circuit

TABLE 1. The truth table of 7443 IC

INPUTS				OUTPUTS									
D	**C**	**B**	**A**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	0	1	1	0	1	1	1	1	1	1	1	1	1
0	1	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	1	1	1	0	1	1	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	1	0	1	1
1	0	1	1	1	1	1	1	1	1	1	1	0	1
1	1	0	0	1	1	1	1	1	1	1	1	1	0

gates are needed. For NOT gate with tile, the gate presented in Figure 9. will be used. For the NAND gate, the gate that can be seen in Figure 11 will be used.

The following QCA circuit of excess-3 to the decimal converter using tile method is shown in Figure 13.

The presented circuit is implemented in three layers, the main layer, the via layer, and the top layer, all of these layers are shown in Figures 14 to 16.

To reduce the occupied area of the circuit as much as possible, its design and implementation have been done in three layers. Also, in this circuit, 516 cells are used, occupying an area equal to 0.43μm^2. In addition, 6 clock phases have been used in this circuit. The total energy consumption for this circuit is about 1.14e-001 eV. As it can be seen from Figure 13. There are not any NOT gates that make the circuit as faster as possible. In this circuit 22 main blocks (which here are tiles and for gate method is majority gate) are used.

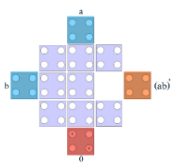

Figure 11. NAND gate in QCA using the Tile method

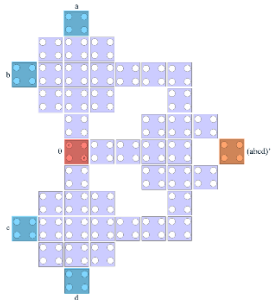

Figure 12. Four inputs NAND gate with tile

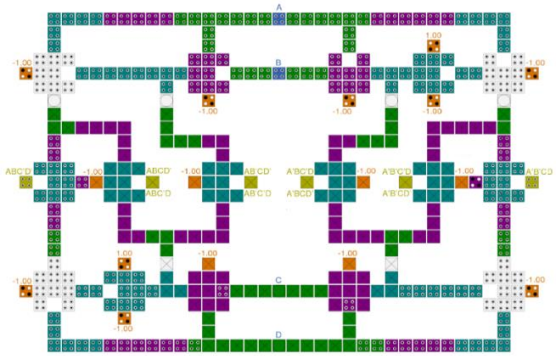

Figure 13. Proposed excess-3 to the decimal converter (7443 IC) QCA circuit

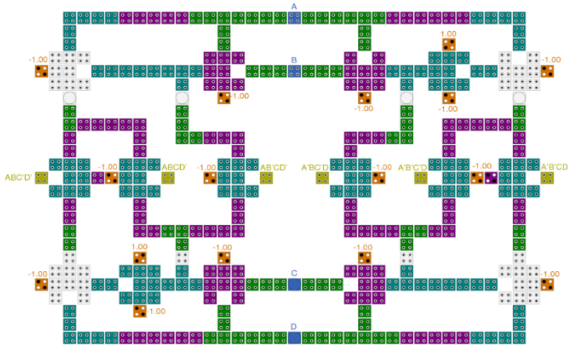

Figure 14. The main layer of the proposed excess-3 to decimal converter (7443 IC) QCA circuit.

Figure 15. The via layer of proposed excess-3 to decimal converter (7443 IC) QCA circuit.

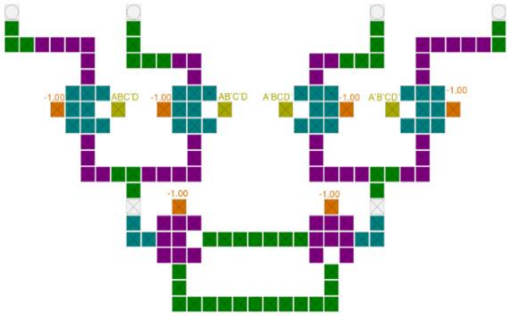

Figure 16. The top layer of proposed excess-3 to decimal converter (7443 IC) QCA circuit

3. 2. Proposed Decimal to Excess-3 Code Converter In this section, the circuit of a converter is presented which gives an excess-3 code instead of a decimal number. Just like the previously proposed circuit, this circuit is implemented with the tile method. The logical circuit for this converter is given in Figure 17. Also, the truth table for this circuit is presented in Table 2.

TABLE 2. The truth table of decimal to excess-3 code converter

INPUTS										OUTPUTS			
I0	**I1**	**I2**	**I3**	**I4**	**I5**	**I6**	**I7**	**I8**	**I9**	**O1**	**O2**	**O3**	**O4**
1	0	0	0	0	0	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	0	0	1	0	0	0	0	0	0	1	1	1
0	0	0	0	0	1	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1	0	0	1
0	0	0	0	0	0	0	1	0	0	1	0	1	0
0	0	0	0	0	0	0	0	1	0	1	0	1	1
0	0	0	0	0	0	0	0	0	1	1	1	0	0

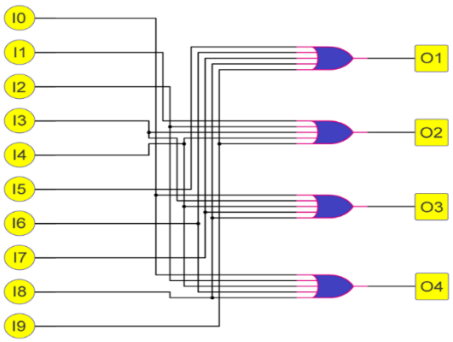

Figure 17. Decimal to excess-3 code converter logical circuit

As it is seen, this converter includes ten inputs for the decimal number (from 0 to 9) and four outputs for the excess-3 number (from 0011 to 1100), and four OR are used in this circuit. In this circuit OR gate which is implemented with the tile method is shown in Figure 18 is used.

In the following, the QCA circuit of decimal to excess-3 converter using the tile method is presented in Figure 19.

Just like the previously proposed circuit, this circuit also is implemented in three layers, the main layer, the via layer, and the top layer, all of these layers are shown in Figures 20 to 22.

Same as the previous circuit, to reduce the occupied area of the circuit as much as possible, its design and implementation have been done in three layers. Also, in this circuit, 321 cells are used occupying an area equal to 0.28 square micrometers. In addition, 7 clock phases

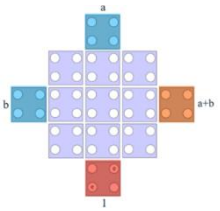

Figure 18. NAND gate in QCA using the Tile method

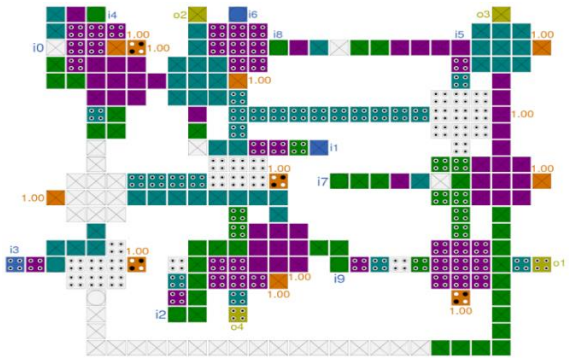

Figure 19. Proposed decimal to excess-3 converter QCA circuit

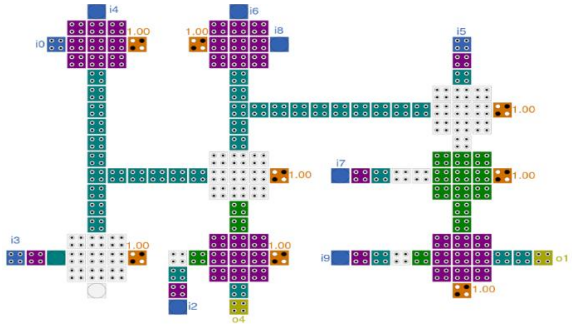

Figure 20. Main layer of proposed decimal to excess-3 converter QCA circuit

Figure 21. Via layer of proposed decimal to excess-3 converter QCA circuit

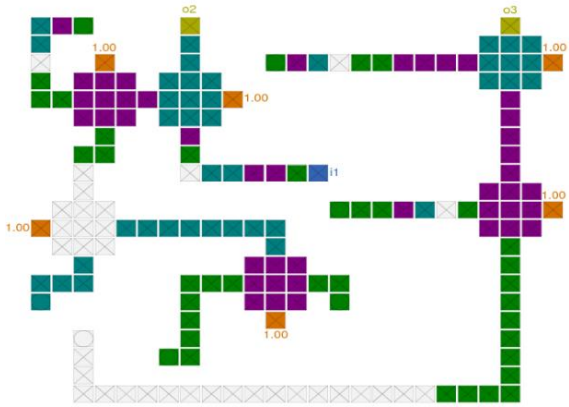

Figure 22. The top layer of the proposed decimal to excess-3 converter QCA circuit

have been used in this circuit. As can be seen from Figure 19. There are zero NOT gates which make the circuit as faster as possible. In this circuit, 14 main blocks (which here are tiles and for gate method is majority gate) are used. The total power consumption for this circuit is about 1.04e-001 eV.

4. SIMULATIONS AND RESULTS

In this section, the accuracy of the proposed circuits is checked using QCADesigner-E software. QCADesigner-E is one of the most reliable software in the field of QCA, and version 2.2 is used in this paper [17, 18]. This software was developed by the University of Calgary. Using this software, values such as the number of cells, the number of clock phases, the occupied area, and the power consumption can be extracted. In the following, the simulation results of each of the converters will be given in Figure 23. The inputs of the excess-3 code to decimal converter can be seen. These inputs have produced the outputs in Figure 24. As it is clear from the mentioned figure, the proposed circuit has correctly produced the expected values, for example, for producing (ABC'D')' inputs are A=1, B=1, C=0 and D=0 that produce ABC'D' output, with inverting this output the main output is produced (this is shown in Figures 23 and 24). For the next converter, decimal to excess-3 code, in Figure 25. the decimal inputs of this converter can be seen. These inputs have produced the outputs in Figure 26. As it is clear from the outputs, the proposed circuit has correctly produced the expected values, for example, to produce O4 output which one of I0, I2, I4, I6, or I8 is binary "1" the output will be binary "1" (this is shown in Figures 25 and 26). As mentioned before the first proposed circuit had 516 cells and 6 clock phases have been used in it. Also, the total power consumption for this circuit was about 1.14e-001 eV. The second proposed circuit had 321 cells and 7 clock phases have been used in it. Also, the total power consumption for this circuit was about 1.04e-001 eV. The most important cell in energy consumption are fixed cells and of course, the central cell which is played as the calculator cell. Because there are no similar works for this type of conversion, we cannot compare the proposed design with other related works. In Table 3. details of the proposed circuits are given.

As it was clear, in the proposed excess-3 to decimal converter, in Figure 23. An excess-3 code equal to 0100 was chosen. After 6 phases of the clocking, the answer was checked in Figure 24. (ABC'D')' was supposed to be "0", as it was. To consider another example, 1010 excess-3 code can be chosen. The answer was supposed to be "0" just for the (AB'CD')', it can be seen that the correct answer is obtained. To check the proposed decimal to excess-3 code converter is investigated. In Figure 25, there were 10 different inputs from 0 to 9 of the decimal code. Because O1 = I8 + I9 wherever one of these inputs gets the binary "1" O1 output was supposed to be "1", which can be seen in Figure 26.

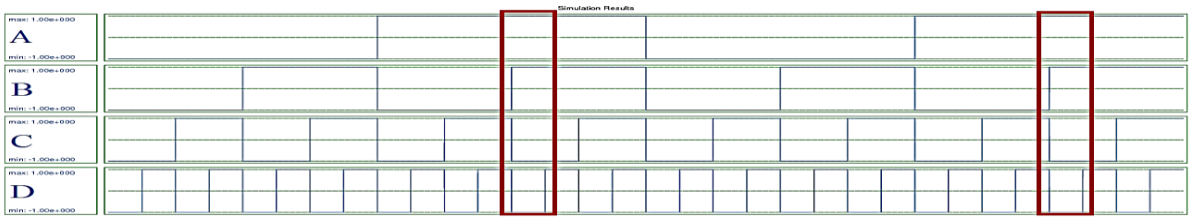

Figure 23. Inputs of proposed excess-3 to decimal converter QCA circuit

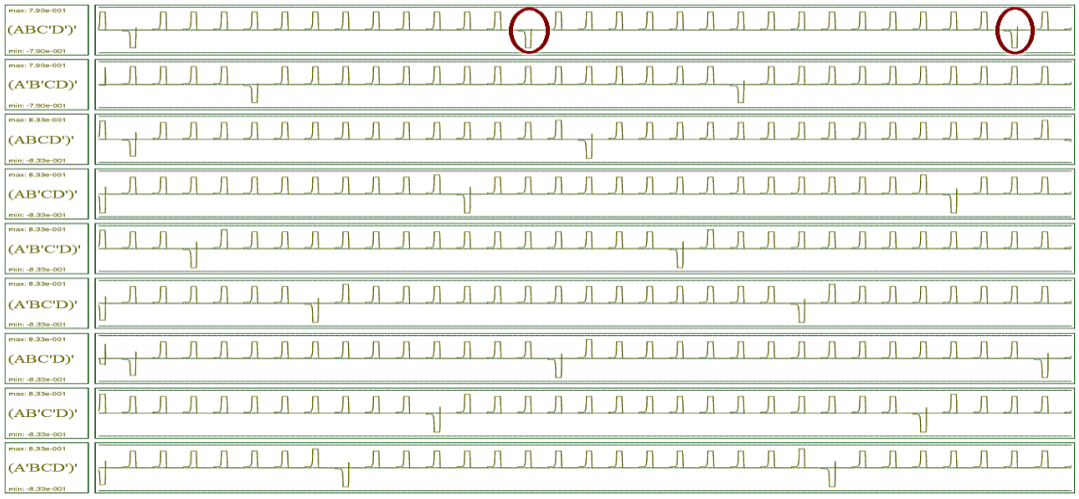

Figure 24. Outputs of proposed excess-3 to decimal converter QCA circuit

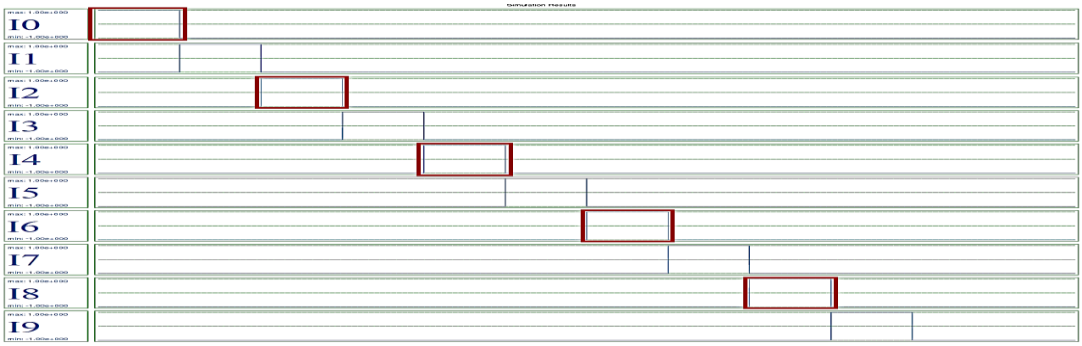

Figure 25. Inputs of proposed decimal to excess-3 converter QCA circuit

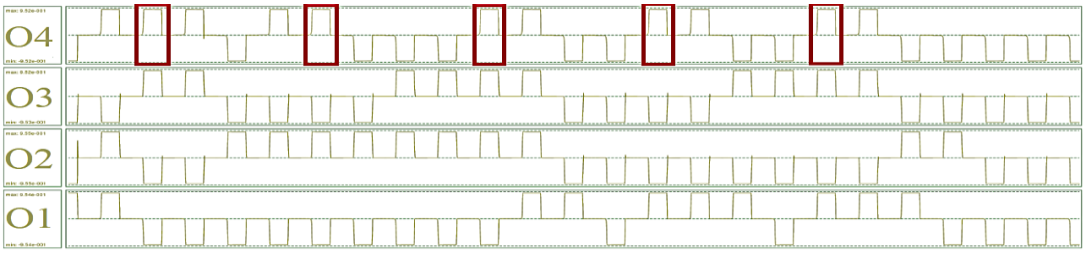

Figure 26. Outputs of proposed decimal to excess-3 converter QCA circuit

TABLE 3. Details of proposed circuits

Items	Excess-3 to Decimal converter	Decimal to Excess-3 converter
Cell count	516	311
Delay (clock phases)	6	7
Main gate count	22	14
Inverter gate count	0	0
Power consumption	1.14e-001 eV	1.04e-001 eV
Designing type	Tile method	Tile method
Ability to integrate	HIGH	HIGH

5. CONCLUSION

In this paper, two digital converters were presented, the first one was for converting excess-3 code to decimal and another one was for converting decimal to excess-3 code. The method that was used in both of them was the tile method. This method has some advantages, with this method circuits can be integrated and get faster because there is no need to use an inverter gate lonely. In the end, both of the proposed circuits were evaluated with QCADesigner-E, and some reports like cell count, delays, power consumption, etc. were presented.

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Persian Abstract

چکیده

امروزه اتوماتای سلولی نقطه کوانتومی (QCA) یکی از فناوری های جدید در مقیاس نانو است که می تواند در مدارهای آینده مورد استفاده قرار گیرد. اکثر مدارهای دیجیتال با فناوری CMOS پیاده سازی می شوند، اما CMOS دارای مشکلاتی مانند مصرف انرژی و اندازه مدار است. بنابراین برای حل این مشکلات روش جدیدی (QCA) ارائه شده است. واضح است که مبدل ها نقش مهمی در دنیای دیجیتال دارند. بنابراین، با توجه به نکته فوق، در این مقاله دو مبدل کد دیجیتال شامل مبدل کد اضافی ۳ به اعشار و یک مبدل اعشاری به بیش از ۳ ارائه شده است. روش کاشی برای طراحی مدارهای پیشنهادی در فناوری نانو اتوماتای سلولی نقطه کوانتومی (QCA) استفاده می شود. روش کاشی یک بلوک منحصر به فرد برای دروازه های اکثریت و NOT می دهد. این ویژگی یکپارچگی را تسهیل می کند. هر دو مبدل کد پیشنهادی دارای ۱.۷۵ تاخیر سیکل ساعت هستند و اتلاف انرژی در حدود ۱۰۰ مگا ولت دارند. در مبدل کد اضافی به اعشار از ۵۱۶ سلول استفاده شده است که مساحتی معادل ۰.۴۳ میکرومتر مربع را نیز در مبدل کد اعشاری به بیش از ۳ اشغال می کند. ۳۲۱ سلول استفاده شده است که مساحتی معادل ۰.۲۸ میکرومتر مربع را اشغال می کنند.