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A New Multilevel Inverter Based on Harvest of Unused Energies for Photovoltaic Applications

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A B S T R A C T

In multilevel inverters, unused energies are created due to the asynchronous use of the input DC sources. when the input DC sources are replaced by renewable systems such as photovoltaic arrays, some of the input energies remain unused. This paper presents a new multilevel inverter topology that can harvest the unused energies and return them to another output which leads to the harvest of the maximum input energy. The harvest of maximum energy (HME) based multilevel inverter structure consists of two terminals. One is connected to AC-load and another is joined to DC-load or rechargeable batteries. Another merit of the proposed multilevel inverter is that the number of its switches is comparable to other structures where unused energies cannot be harvested. Selective harmonic elimination (SHE) has been used as the switching strategy in the proposed multilevel structure. To verify the performance of the HME-based multilevel inverter topology, the experimental results for a type seven-level inverter were performed by the TMS320F28379D DSP.

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1. INTRODUCTION

In comparison with two-level inverters, multilevel inverters (MLI) have been rapidly developed by researchers due to lower total harmonic distortion (THD), lower switching frequency, the smaller size of the filter, and lower dv/dt stress on the load. They have been rapidly used in photovoltaic systems [1-8]. The MLI are classified to three main groups: neutral-point clamped (NPC) [9, 10], flying capacitor (FC) [11, 12] and cascaded H-bridge (CHB) topologies [13, 14]. In NPC and FC structures, the clamped diodes and capacitors are responsible for transmitting the input voltage to constitute the N-level voltage at the output, respectively. The main advantage of these topologies is that they require only one isolated DC source. However, to achieve higher voltage levels, they need a high number of semiconductor devices (switches and diodes) and passive elements. Another drawback of NPC and FC topologies is that the neutral point voltage is unbalanced. However, many researchers have reported several improved structures to overcome such limitation; but, there are still a high number of semiconductor devices in their topologies [15-17]. The CHB multilevel inverters are suitable for reactive power compensators, battery chargers, photovoltaic systems, electrical vehicles, and so on. Unlike the NPC and FC topologies, the CHB structure acted in asymmetric mode (inequality of input DC-sources) to achieve a number of higher voltage levels. The most important disadvantage of the CHB topology is that there are several isolated DC sources in its structure [18, 19]. Recently, the switched-source (SS) and switched-capacitor (SC) based topologies have been introduced by researchers which reduced the number of semiconductor devices [20-24]. In the SS topologies, we can obtain structures with a very low number of switches. This reduces drastically switching losses, cost, and volume of the drive system. However, there are several DC sources in this structure. The SC multilevel inverters can behave as the boost converter. So, the SC multilevel inverters can be used for applications such as photovoltaic systems that produce a low voltage on their

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inputs. They can generate a number of high voltage levels at the output with a small number of DC sources. It can be concluded from the above discussion, that in the CHB, SS, and SC topologies, to achieve the number of high voltage levels and low THD on the load, they need a number of high input DC sources. This subject leads to the appearance of unused energies in the multilevel inverters. For more understanding, according to Figure 1, consider the seven-level SS-based multilevel inverter that has been introduced by Prabaharan et al. [25].

First, assume that the switching state equals ($S_1S_2T_1T_2T_3T_4$=101010) and the current commutation paths are accords with the arrow lines shown in Figure 1a. In this condition, the input DC source u_1 is transferred to the load. Right at this moment, the input DC-source u_2 is unemployed. Moreover, according to Figure 1b, in the switching state ($S_1S_2T_1T_2T_3T_4$=011010), when the input DC source u_2 is transmitted to the load, the input DC source u_1 is unemployed. Therefore, in multilevel inverters which contain several input DC sources, there are moments when some or all of the DC sources remain unused. It means that, if the input DC sources u_1 and u_2 are replaced by the photovoltaic systems, some of the input energies will not be used by the inverter. In this paper, a new multilevel inverter is introduced so that it can harvest the unused energies and return them to another load which leads to the harvest of maximum input energy. It is obvious that the proposed topology must have the least number of semiconductor devices. For this reason, Prabaharan et al. [25] the inverter which is shown in Figure 1, is selected as the base structure for this purpose. To evaluate the performance of the HME-based multilevel inverter, the selective harmonic elimination (SHE) technique is selected as the switching strategy. The SHE is a low switching frequency strategy that provides us with low switching losses [26-29]. In summary, the benefits and properties of the proposed multilevel inverter can be listed as follows:

- The proposed HME-based multilevel inverter can harvest the maximum energy which could not be harvested by previous multilevel inverters.
- In the proposed topology, the number of switches is comparable to other structures.
- The SHE method is selected as the switching strategy.
- The proposed multilevel inverter can be implemented by an experimental setup.

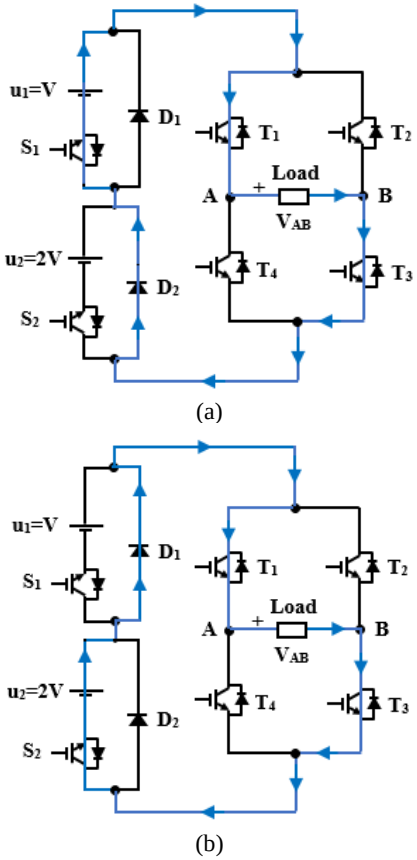


Figure 1. Introduced seven-level SS-based multilevel inverter by Prabaharan et al. [25]. (a) $S_1S_2T_1T_2T_3T_4$=101010), (b) ($S_1S_2T_1T_2T_3T_4$=011010)

2. PROPOSED HME-BASED MULTILEVEL INVERTER

2. 1. Seven-level Structure The proposed seven-level HME-based inverter is shown in Figure 2. However, it can be generalized to N-level configuration. As shown in Figure 2, the HME-based multilevel inverter consists of two terminals AB and XY which are connected to AC and DC load, respectively. It should be noted that the XY terminal is responsible for transferring the unused energies that did not previously exist on Prabaharan's inverter in Figure 1. The semiconductor

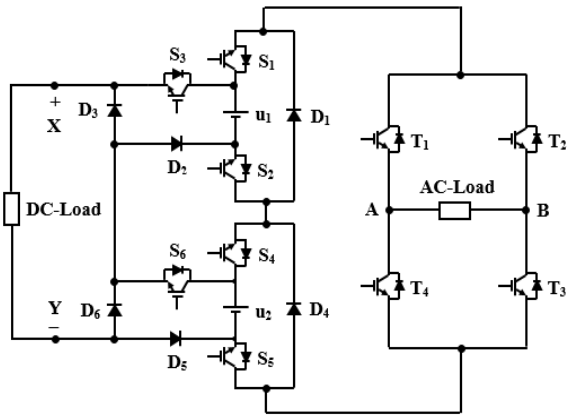


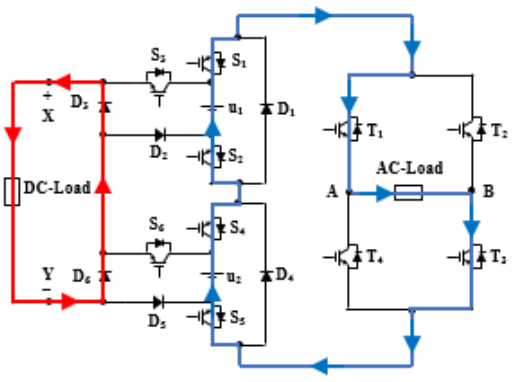
Figure 2. Proposed seven-level HME-based inverter with u_1=V and u_2=2V

devices ($S_1S_2S_4S_5D_1D_4$) and ($S_3S_6D_2D_3D_5D_6$) are arranged to transfer the power to the AB and XY terminals, respectively. They are configured in the new structure so that there is no common current path between the two terminals. For instance, when the S_3 is turned on, (S_1S_2) is turned off and D_3 is reverse biasing. In this condition, the DC-source voltage u_1 is transferred to the XY terminal through D_2 and S_3 devices.

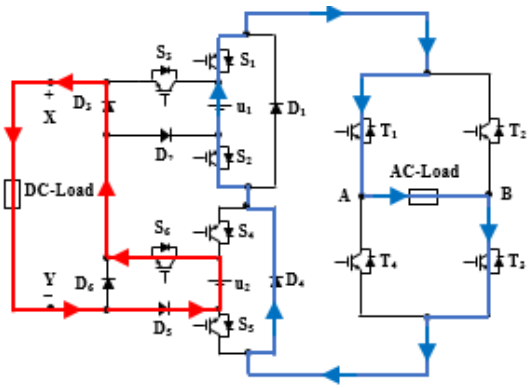
At this moment, D_1 is direct biasing and it can conduct the current to the AC load in the AB terminal. The switching states of the seven-level HME-based inverter have been listed in Table 1. As shown in Table 1, there are seven switching states for producing seven-level of voltage in the output. The switches (S_1S_2) and (S_4S_5) are logically NOT the switches S_3 and S_6, respectively. In addition, the diodes D_1 and D_2 (also D_4 and D_5) can simultaneously be turned on and off. So, it is guaranteed that there is no common current between the AB and XY terminals. The commutation pathways according to switching states have been depicted in Figure 3. For example, in Figure 3(b), the DC-sources u_1=V and u_2=2V are simultaneously transferred to the XY and AB terminals for DC and AC loads, respectively. In this condition, the V_{AB}=+2V and V_{XY}=+V. In Figures 3(e), 3(f) and 3(g), according to the activating of T_2 and T_4 in the H-bridge section, the sign of V_{AB} is negative. The other switching modes in Figure 3 are analyzed according to Table 1.

TABLE 1. The switching states of proposed seven-level HME-based inverter

S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	V_{AB}	V_{XY}
1	1	0	1	1	0	1	0	1	0	+3V	0
0	0	1	1	1	0	1	0	1	0	+2V	+V
1	1	0	0	0	1	1	0	1	0	+V	+2V
0	0	1	0	0	1	1	0	1	0	0	+3V
1	1	0	0	0	1	0	1	0	1	-V	+2V
0	0	1	1	1	0	0	1	0	1	-2V	+V
1	1	0	1	1	0	0	1	0	1	-3V	0



(a)



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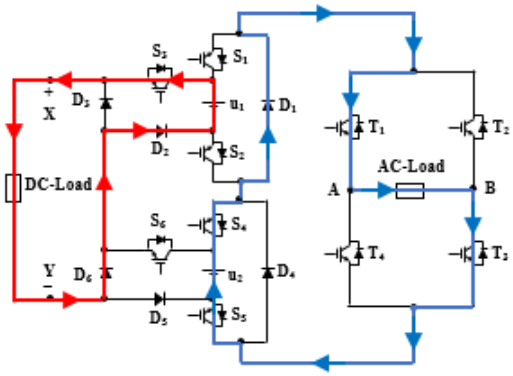
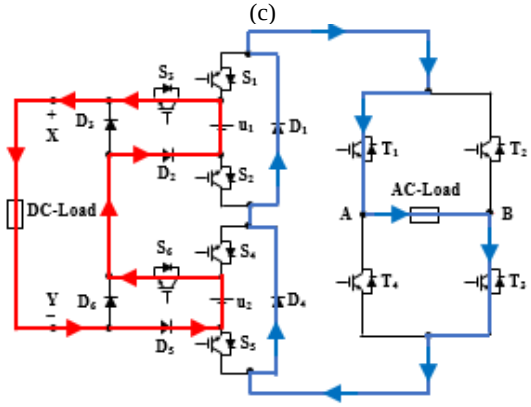


(b)



(d)

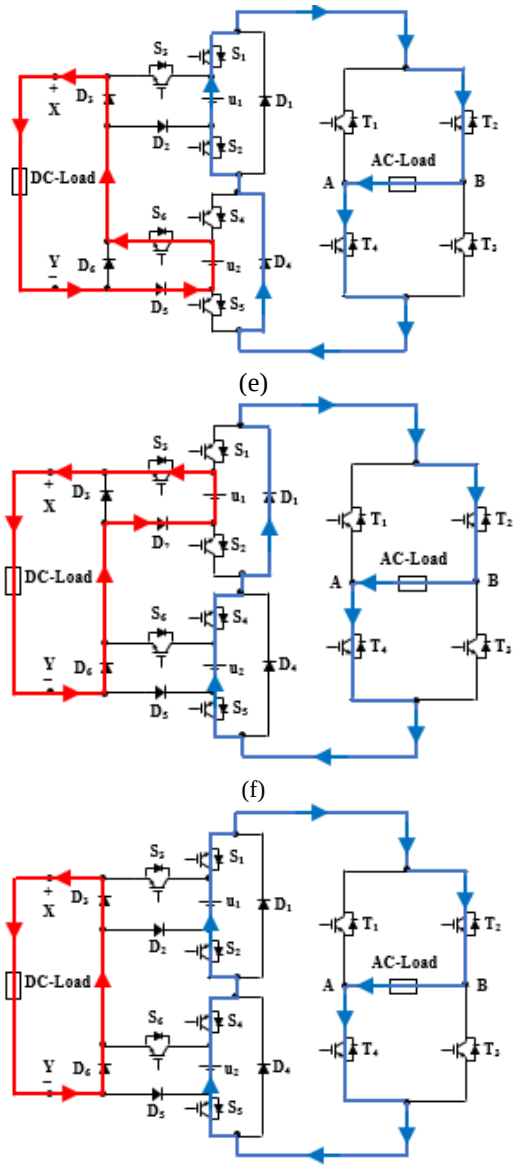


Figure 3. Schematic of switching states for generating different voltage levels on AC and DC loads with u_1=V and u_2=2V. (See Table 1): (a) State 1 for V_{AB}=+3V and V_{XY}=0V. (b) State 2 for V_{AB}=+2V and V_{XY}=+V. (c) State 3 for V_{AB}=+V and V_{XY}=+2V. (d) State 4 for V_{AB}=0V and V_{XY}=+3V. (e) State 5 for V_{AB}=-V and V_{XY}=+2V. (f) State 6 for V_{AB}=-2V and V_{XY}=+V. (g) State 7 for V_{AB}=-3V and V_{XY}=0V

It should be noted that, for decreasing the voltage ripple, we can consider a capacitor on the output XY terminal. However, in this work, to accurate calculation of the used and unused energy, we decided that it does not consider.

2. 2. Generalized HME-based Multilevel Inverter

An N-level structure can be implemented in modular form by serializing the several units of the HME-based multilevel inverter which is shown in Figure 4.

It should be noted that the terminal XY is unipolar which can generate the voltage in forming of multilevel. In symmetric mode ($u_1 = u_2 = \ldots = u_n$), the number of switches (N_{sw}) and the number of generated voltage levels on the terminals AB ($N_{level,AB}$) and XY ($N_{level,XY}$) can be calculated as follows:

$$\begin{cases} N_{sw} = \dfrac{3N_{level,AB}+5}{2} \\ N_{level,AB} = 2n+1 \\ N_{level,XY} = n+1 \end{cases} \quad (1)$$

where n is the number of units.

In asymmetric mode, by considering the pattern of DC-sources voltage as (u_1 =V, u_2 =2V, u_3 =3V,…, u_n =nV), the number of switches and voltage levels can be formulated as follows:

$$\begin{cases} N_{sw} = \dfrac{3}{2}\sqrt{4N_{level,AB}-3}+\dfrac{5}{2} \\ N_{level,AB} = n^2+n+1 \\ N_{level,XY} = \dfrac{n^2+n+2}{2} \end{cases} \quad (2)$$

Although, there are multiple voltage patterns in the asymmetric mode for achieving the number of high

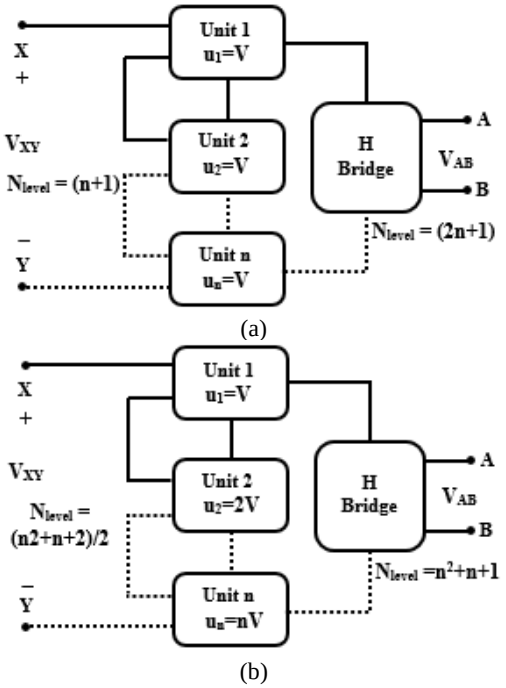


Figure 4. Generalizing of the proposed HME-based multilevel inverter to the N-level structure. (a) Symmetric mode and (b) Asymmetric mode

voltage levels such as (u_1=V, u_2=2V, u_3=4V,…, u_n=2^{n-1}V), they increase the total standing voltage (TSV) of some switches that are not appropriate.

3. COMPARISON OF THE HME-BASED MULTILEVEL INVERTER WITH OTHER TOPOLOGIES

It should be noted that harvesting maximum energy requires the use of a large number of switches. However, the proposed inverter is comparable to other structures that cannot absorb these energies. Table 2 shows the number of switches for six different multilevel inverters. In Table 2, the inverter is a multilevel inverter type of switched-source that has been introduced by Babaei and Hosseini [24]

Figure 5 shows the curve of the number of switches in terms of the number of voltage levels for multilevel inverters listed in Table 2. Any curve that has a lower slope means fewer switches in its structure. For example, in symmetric mode, as shown in Figure 5(a), to achieve a 50-level voltage in the inverter output, 28, 54, 78 and 96 switches are required for the Prabaharan, Babaei, HME and CHB topologies, respectively. Also, in asymmetric mode, according to point M shown in Figure 5(b), the HME-based multilevel inverter has a smaller number of switches than the CHB topology for voltages above 21 levels. So, the proposed HME-based multilevel inverter is comparable to other multilevel inverter topologies.

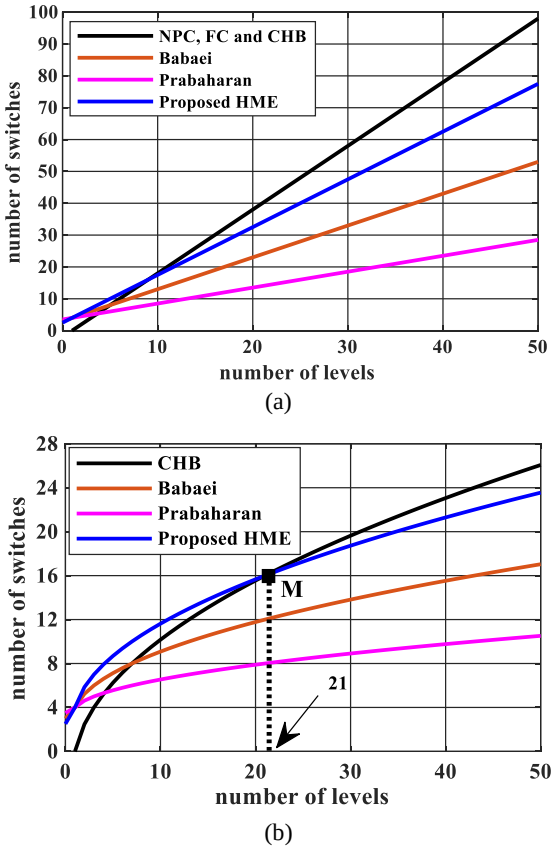


Figure 5. Comparison of the proposed HME-based multilevel inverter with other topologies. (a) Symmetric mode and (b) Asymmetric mode

4. CALCULATION OF THE TRANSFERRED ENERGY TO THE TERMINAL XY

In this section, the transferred energy to terminal XY is calculated. This is the same unused energy in conventional multilevel inverters such as Babaei and Hosseini [24], Prabaharan et al. [25], etc.

TABLE 2. The number of switches in several multilevel inverter topologies

Type of Multilevel inverter	Number of switches in symmetric mode	Number of switches in asymmetric mode
NPC [9, 10]	$2(N_{level}-1)$	----------
FC [11, 12]	$2(N_{level}-1)$	----------
CHB [13]	$2(N_{level}-1)$	$2\sqrt{4N_{level}-3}-2$
Babaei and Hosseini [24]	$N_{level}+3$	$\sqrt{4N_{level}-3}+3$
Prabaharan et al. [25]	$\frac{(N_{level}+7)}{2}$	$\frac{1}{2}\sqrt{4N_{level}-3}+\frac{7}{2}$
Proposed HME	$\frac{(3N_{level}+5)}{2}$	$\frac{3}{2}\sqrt{4N_{level}-3}+\frac{5}{2}$

For this purpose, the SHE method is considered as a switching strategy due to its staircase manner and easy analysis. Here, for facilitating the equations, it is assumed that the load is pure resistive in both terminals AB and XY. Figure 6 shows the voltage waveforms in terminals AB and XY in the proposed seven-level HME-based inverter under the SHE switching strategy. In Figure 6, V_{dcm} and (α_1, α_2, α_3) are the smallest voltage level on the loads and switching angles, respectively. For calculating the transferred energy to the terminal XY, it should be integrated from the power. According to the in-phase of voltage and current in terminal XY, the transferred energy to the terminal XY (E_{XY}) can be written as follows:

$$E_{XY}=\int_0^t V_{XY}(t)I_{XY}(t)d(t)= \int_0^{\alpha_1} 3V_{dcm}\frac{3V_{dcm}}{R}dt+\int_{\alpha_1}^{\alpha_2} 2V_{dcm}\frac{2V_{dcm}}{R}dt +.....+\int_{\pi-\alpha_1}^{\pi} 3V_{dcm}\frac{3V_{dcm}}{R}dt \quad (3)$$

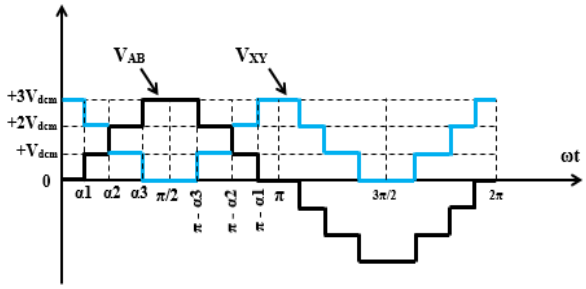


Figure 6. The voltage waveforms in terminals AB and XY under the SHE switching strategy, according to Table 1

where $V_{XY}(\omega t)$ and $I_{XY}(\omega t)$ are the instantaneous voltage and current in terminal XY, respectively.

Moreover, R is the resistance of DC load. By solving equation 3, in one complete cycle ($t=2\pi$), the E_{XY} is obtained as follows:

$$E_{XY} = \frac{2V_{dcm}^{\ 2}}{R}\left(10\alpha_1 + 6\alpha_2 + 2\alpha_3\right) \tag{4}$$

Equation (4) describes the unused energy in a seven-level inverter under the SHE switching strategy which can be harvested by the proposed HME-based inverter in the terminal XY. It can be generalized to the N-level conditions as follows:

$$\begin{aligned} E_{XY,N_{level}} = \frac{2V_{dcm}^{\ 2}}{R}[&(2N_{level}-4)\alpha_1 \\ &+(2N_{level}-8)\alpha_2 \\ &+(2N_{level}-12)\alpha_3 \\ &+.....+2\alpha_{\frac{N_{level}-1}{2}}] \end{aligned} \tag{5}$$

Now, assume that there is a relationship between switching angles as $\alpha_k = k\alpha_1 \quad (\alpha_2 = 2\alpha_1, \alpha_3 = 3\alpha_1, ...)$ which is close to the real conditions. By defining P_0 as $P_0 = \left(V_{dcm}^{\ 2}/R\right)\alpha_1$, the curve E_{XY}/P_0 in terms of the number of voltage levels can be depicted in Figure 7. By comparing the real and linear curves in Figure 7, it can be seen that as the number of inverter voltage levels increases (with increasing the number of DC inputs), the unused energy increases with nonlinear behavior. So, the harvest of maximum energy at a high number of voltage levels is more important than the inverters with a low number of voltage levels.

5. EXPERIMENTAL RESULTS

The introduced HME-based seven-level inverter can be implemented as illustrated in Figure 8.

The experimental setup consists of a TMS320F28379D DSP as the processor, a gate driver, the proposed HME-based multilevel inverter, several R-L loads, two 1/7 Ω series resistance as the current sensors, and multiple power supplies. In the gate driver circuit, the HCPL-3120 is used as both a DSP ground isolator and a switch driver. Moreover, in this circuit, two 74HC245 buffers are applied to prevent the current consumption by the DSP. The important point about the gate driver circuit is that the gate driver power supply ground should only be connected to the negative terminal of DC-source u_1 (see Figure 2). To select the switches and diodes, it should be noted that, in the experimental works, due to limitations in DC-link power supplies, the selected switches and diodes should have a low voltage drop. For this reason, the switches and diodes in our setup have been chosen as IRG41BC30S IGBTs and MBRF20100CT Schottky diodes, respectively.

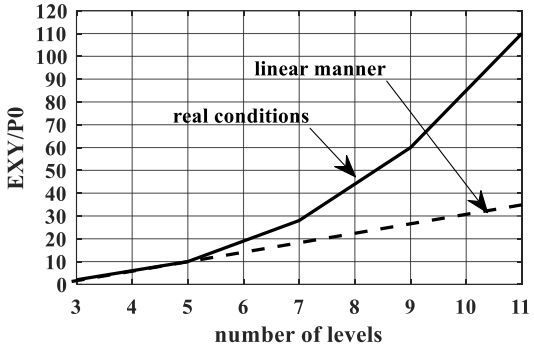


Figure 7. The energy manner in terminal XY with increasing the number of voltage levels

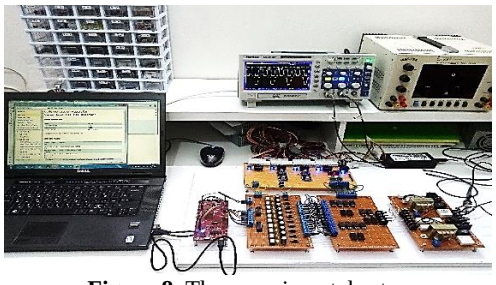


Figure 8. The experimental setup

In our experimental implementation, the values of DC-sources u_1 and u_2 are selected as 50v and 100v, respectively. For obtaining different values of DC-source voltage, they can be variable by two high current buck-boost converter modules. Figure 9 shows the inverter output voltages V_{AB} and V_{XY} with constant pure resistive load Z=50 Ω under various modulation indexes. According to a selection of DC sources as u_1=50v and u_2=100v, the maximum voltage level of both V_{AB} and V_{XY} was expected to be 150v (V=50v, 2V=100v, 3V=150v) but as shown in Figure 9(a), it is equal to 140v. This is due to the voltage drop across the switches and diodes. In Figure 9(b), as was expected, by reducing the modulation index, the width of the largest voltage AB

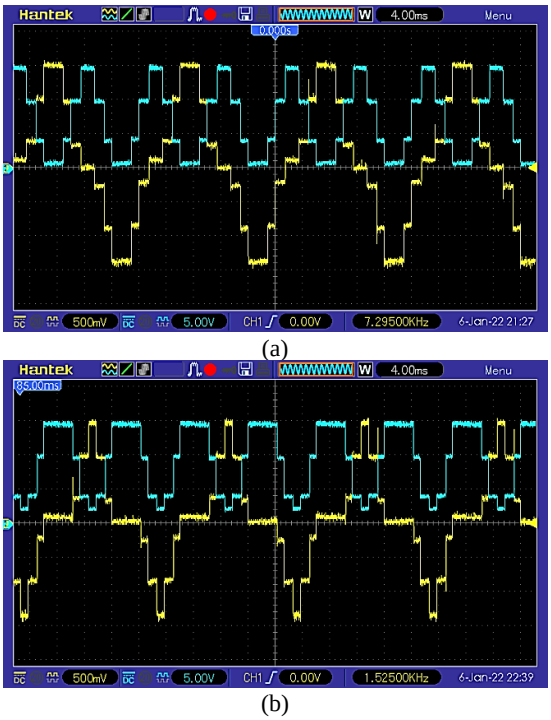


Figure 9. Experimental results with constant resistive load Z=50 Ω (for both DC and AC loads). (a) Output voltages V_{AB} (yellow wave × 50 V/div.) and V_{XY} (blue wave × 1 V/div.) under M=0.7, (b) Output voltages V_{AB} (yellow wave × 50 V/div.) and V_{XY} (blue wave × 1 V/div.) under M=0.5

level is diminished. So, it is expected that the fundamental harmonic of voltage AB is also reduced. Unlike the behavior of voltage AB, by reducing the modulation index, the width of the largest voltage XY level is increased. So, it is expected that the mean value of voltage XY is increased. It can be concluded from the above discussion, the rechargeable batteries are a suitable option for DC load when the SHE method is used as a switching strategy.

It should be noted that, in our work, two 1Ω series resistances with the AB and XY outputs have been used as current sensors. So, for achieving the real values of currents I_{AB} and I_{XY}, the amplitude of the current waveforms must be multiplied by 1. Figure 10 shows the experimental results with changing of load impedance from Z_1=58 Ω + 12 mH to Z_2=135 Ω + 66 mH under constant modulation index M=0.7. Since the impedance Z_2 is more inductive than the impedance Z_1, two events are expected to occur when the impedance Z_2 is applied to both inverter terminals.

First, according to Figure 10(a), the voltage V_{AB} becomes like a pulsating wave when the polarity changes. In this condition, due to the unipolar of the terminal XY, the voltage V_{XY} does not has the pulsating-shaped wave. Second, as shown in Figures 10(b) and 10(c), the currents I_{AB} and I_{XY} get closer to the sine wave. However, the amplitude of currents I_{AB} and I_{XY} has

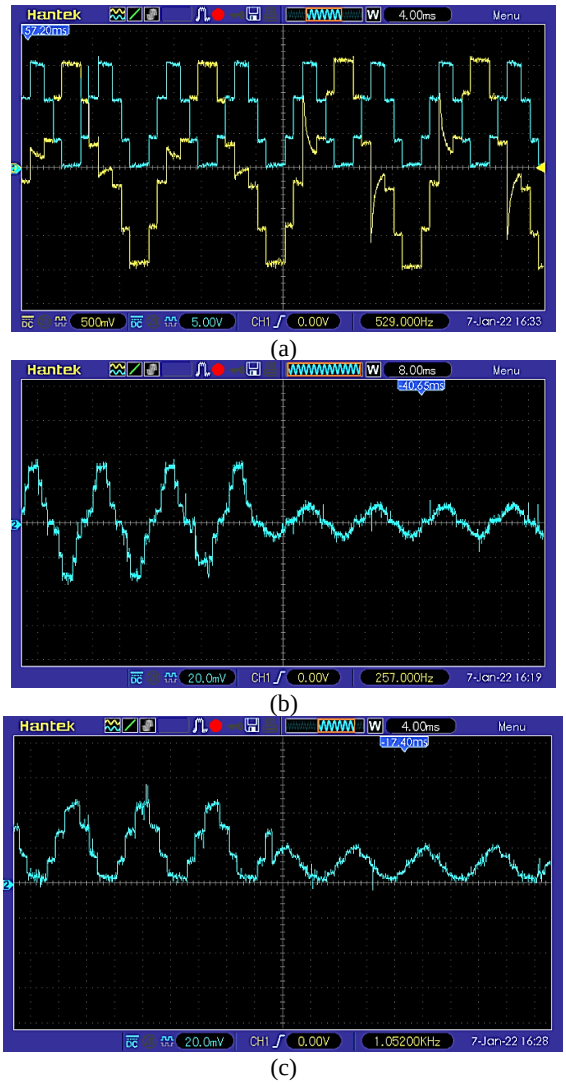


Figure 10. Experimental results with change of load impedance from Z_1=58 Ω + 12 mH to Z_2=135 Ω + 66 mH (for both DC and AC loads) under constant modulation index M=0.7. (a) Output voltages V_{AB} (yellow wave × 50 V/div.) and V_{XY} (blue wave × 1 V/div.), (b) current I_{AB}, (c) current I_{XY}. (To obtain the real values of the currents, the amplitudes of the waves (b) and (c) must be multiplied by 1 due to compensation for use of the 1-ohm series resistance as the current sensor)

been diminished from 1.8 A to 0.5 A and from 2.4 A to 1 A, respectively.

6. CONCLUSION

A new multilevel inverter based on the harvest of maximum energy was proposed in this paper. The HME-based multilevel inverter consists of two independent AC and DC outputs which can be harvested the unused energies from the XY terminal. The new structure can be

modular form. The most important merit of the proposed topology is that if the inverter input DC sources are replaced by photovoltaic systems, they can be harvested the maximum power and energy from them. So, in future work, we intend to connect the inverter to the grid with photovoltaic arrays so that it can be injected the maximum energy into it. Moreover, the number of semiconductor devices of the proposed multilevel inverter is comparable to traditional inverters. The simulation and experimental results indicate that the HME-based inverter has a good performance for the constant and variable loads under the SHE switching strategy.

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Persian Abstract

چکیده

در اینورترهای چند سطحی، انرژی های استفاده نشده به دلیل استفاده غیر همزمان از منابع DC ورودی ایجاد می‌شوند. هنگامیکه منابع DC ورودی به وسیله سیستم‌های تجدیدپذیر مانند آرایه‌های فتوولتائیک جایگزین می‌شوند، برخی از انرژی‌های ورودی بلا استفاده می‌مانند. این مقاله یک توپولوژی اینورتر چند سطحی جدید ارائه می‌کند که می‌تواند انرژی‌های استفاده‌نشده را برداشت کند و آنها را برای یک بار دیگر برگرداند که منجر به برداشت حداکثر انرژی ورودی می‌شود. ساختار اینورتر چند سطحی مبتنی بر برداشت حداکثر انرژی (HME) از دو پایانه تشکیل شده است. یکی به بار AC و دیگری به بار DC یا باتری‌های قابل شارژ می‌تواند متصل شود. یکی دیگر از مزایای اینورتر چند سطحی پیشنهادی این است که تعداد سوئیچ‌های آن با ساختارهایی قابل مقایسه است که در آنها انرژی‌های استفاده نشده قابل برداشت نیست. روش حذف هارمونیک‌های منتخب به عنوان استراتژی سوئیچ زنی در ساختار چند سطحی پیشنهادی استفاده شده است. به منظور تأیید عملکرد توپولوژی اینورتر چند سطحی مبتنی بر HME، نتایج آزمایشگاهی برای یک اینورتر هفت سطحی توسط پردازشگر سیگنال دیجیتال TMS320F28379D DSP انجام شده است.