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An Advanced Modulation Technique Featuring Common Mode Voltage Suppression for Three-Phase Neutral Point Clamped Back to Back Converters

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ABSTRACT

Three-phase back-to-back converters are widely applied in various industrial, commercial, and domestic applications, such as AC motor drives. Due to the non-sinusoidal voltages they generate, a common mode voltage (CMV) appears, leading to problems in electrical drive systems and high-frequency applications. The CMV and rapid voltage changes can cause serious problems, including leakage currents flowing through the parasitic capacitors inside the motor, electromagnetic interference, shaft voltage, and bearing currents that reduce the motor's lifespan. In general, research to reduce these effects is divided into two methods: modifying the drive system's physical structure or improving the inverter's control algorithm. Pulse Width Modulation (PWM) methods are commonly used in control algorithms of converters to reduce the CMV. However, adding pulse amplitude modulation to the PWM helps reduce the CMV. The technique of simultaneous pulse width and amplitude modulation of space vectors is proposed in this paper to reduce the CMV and its destructive effects in drive systems. The proposed technique is based on the elimination of zero vectors and the inherent reduction of DC link voltage by amplitude modulation leading to a further reduction of the CMV; The obtained results of applying the proposed strategy to a three-phase back-to-back NPC converter with 738-watt steady-state operating point power showed the system's sufficient behavior with the efficiency of 98.62 percent. Finally, the transient performance of the converter from no-load to full-load condition ensures its sufficient behavior for industrial applications.

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1. INTRODUCTION

Electric drives are used in a wide range of power (from a few watts to several thousand kilowatts) in many applications such as pumps, textile and paper mills, elevators, cement and steel mills, and robotics. In Adjustable Speed Drive (ASD) systems, pulse width modulation (PWM) inverters are widely used to control the speed and position between the input and motor. PWM inverters convert DC input voltage to a three-phase AC voltage with adjustable frequency and amplitude for controlling the motor speed. ASD systems use power electronic switching devices to produce pulsed voltages to achieve the objective. With the development of semiconductor power devices such as IGBTs and MOSFETs, the high-frequency operation of PWM converters resulted in improvement of their performance [1]. However, these advances have also increased the adverse effects of these inverters. Due to the non-sinusoidal output waveforms of three-phase PWM inverters, a voltage appears between the neutral point of the load and ground, known as the Common Mode Voltage (CMV), which is the source of many problems in ASD systems. This voltage generates leakage currents that go to the ground through parasitic capacitors inside the motor [2]. These currents may adversely affect motor current control and cause electromagnetic interference, resulting in the malfunction of electronic devices nearby [3]. During the operation of the ASD system, various parasitic capacitors appeared in the motor structure, whereas they

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are negligible in low frequencies. Thanks to the development of switching devices and the possibility of applying higher switching frequencies, the impedance of these parasitic capacitors have become more significant, where they provide an easy path for leakage current at high frequencies.

Furthermore, the CMV contributes to the generation of shaft voltage and bearing currents, resulting in premature failure of the motor bearings [4]. These destructive effects reduce the motor's lifespan and adversely affect the surrounding electronic systems [5]. Therefore, CMV is an essential factor in designing and developing AC electrical drives, and its reduction techniques play a crucial role in reducing the high-frequency problems of these systems. Therefore, numerous techniques for reducing CMV have been discussed in the literature, where optimization is based on pulse width. However, this paper presents simultaneous amplitude and pulse width modulation (PWAM) modulation of space vectors as a new strategy, namely Space Vector Pulse Width and Amplitude Modulation (SVPWAM). This scheme is suitable for medium voltage and high-power AC electrical drive applications. In the proposed method, the ability to change the pulse amplitude is added to the control algorithm of the converter along with the pulse width. In this way, it will further improve the quality of the conventional PWM methods.

Nevertheless, the realization of the PAM part requires changing the DC sources with ones having appropriate transient behavior. Due to the variability of intermediate DC sources in the system, the design of converter parameters is associated with various challenges. The CMV is significantly reduced by regulating the DC link voltage, reducing the harmonic amplitude using PAM, and realizing the SVM method in it (leading to eliminating zero vectors). Moreover, the motor torque ripple is reduced, and a significant improvement in the THD of output voltage and current is achieved [6]. Therefore, the control circuit of the back-to-back converter must be designed to respond to the dynamic speed and produce the DC link voltage with mentioned specifications. In other words, the mentioned parameters have different values in the whole range of the amplitude modulation index.

For this purpose, a solution to select the optimal values is proposed. Despite proposing several reduction methods, it is an evolving field of research required a vast range of theoretical and laboratory analysis. Therefore, less costly and more flexible methods are worth promoting and using in modern industrial applications. Hence, this paper proposed a novel strategy to reduce the CMV, ergo its associated adverse effects in inverters. Implementation of the new SVPWAM modulation strategy is recommended to reduce these effects. Applying the proposed method results in a CMV reduction and low-order harmonics. Therefore, it significantly improves the THD of output voltage and current and decreases the torque ripple of the motor. The proposed strategy is applied to a three-phase three-level back-to-back NPC converter as a more suitable converter for industrial and residential applications. In this regard, the rest of the paper represents the proposed strategy. The second section presents the structure of a three-level back-to-back converter, describing the operation of both the rectifier and inverter. Furthermore, discussing the traditional methods, the CMV generated by them, and conventional methods to reduce the CMV in three-level three-phase inverters are surveyed in section three. Also, these methods' implementation and expansion problems are examined, and the PWAM modulation method is briefly reviewed. Section 4 verifies the proposed control structure's mathematical analyses via MATLAB software simulation results. Then, the harmonic content of the new strategy's output voltage, current, and switching losses are investigated. Afterward, a laboratory prototype is implemented to confirm the simulation results. Finally, the conclusion of the article is presented in the last section.

2. MULTILEVEL INVERTER

Multilevel inverters (MLIs) have attracted many researchers in high power applications such as Flexible AC Transmission (FACT) systems, Static Synchronous Compensators (STATCOM), High Voltage DC (HVDC) transmission, motor drives, active filters, as well as in distributed generation systems such as wind farms, due to the need for high output power and frequency [7]. Compared to two-level inverters, these inverters have advantages in high power applications, such as lower voltage stress on switching devices, reduction of harmonic content, and reduction of (dv/dt) stresses [8, 9]. Cascaded H-bridge, flying capacitor, neutral point (diode) clamped (NPC), and switched capacitors are the most popular topologies of MLIs [10, 11]. NPC MLIs can be configured as three, four, and five-level topologies, but only the three-level ones have been widely utilized in high-power drives [12].

Due to generating non-sinusoidal (asymmetric) pulses in these inverters, a CMV is produced, causing many unwanted problems in motors and drive systems, intensified in high-frequency applications [13]. One inexpensive way to reduce the CMV is to modify the modulation techniques used to control three-phase inverters. The main idea of these methods in MLIs is to select vectors that produce zero or the minimum possible amount of CMV [4, 14]. Zhang et al. [15] provided modulation methods for eliminating CMV based on space vector modulation and sinusoidal PWM

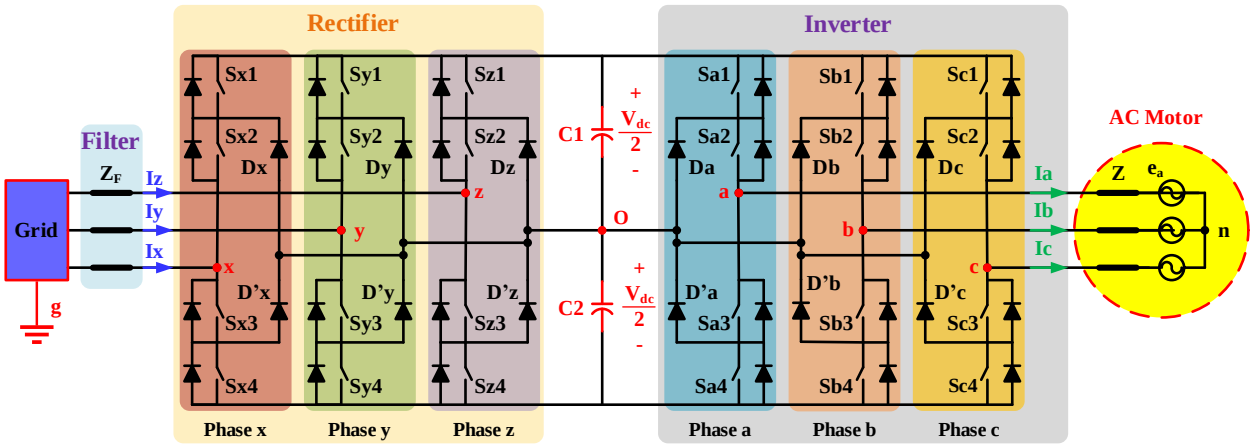


Figure 1. Circuit diagram of a three-level NPC back-to-back converter

in NPC MLI. A carrier-based CMV elimination method, along with neutral-balancing, is bybZheng et al. [16]. This method somewhat decreases the CMV; however, the output voltage's THD is considerably high. Furthermore, Xu et al. [17] proposed a zero voltage sequence (ZVS) injection method based on the phase-disposition pulse width modulation (PDPWM).

This method reduced the CMV up to Vdc/6. However, the output voltage THD significantly increases. Adabi et al. [4] proposed a PWM technique to reduce the CMV. These methods reduce the quality of the inverter's output currents because they are based on voltage control and eliminate some voltage vectors to achieve the desired CMV. In this regard, Figure 1 shows the circuit diagram of a three-level NPC-based back-to-back converter used in medium voltage AC drives. The operating conditions of the NPC MLI can be defined by the switching modes shown in Table 1. For example, for leg a of the inverter, the switching state P indicates that the upper two switches on this leg are ON, and the voltage between terminal a and the neutral point O (*Vao*) is $+V_{dc}/2$. Likewise, the N switching state indicates that the two lower switches on this leg are turned on and *Vao* $=-V_{dc}/2$. The state O indicates that the two internal switches are ON; in this case, *Vao* will be zero.

Hence, considering the total of three phases, there would be 27 combinations of switching states for the NPC inverter, which are listed in Table 2, along with the CMV and the resulting voltage vectors. These 27 switching states produce 19 different voltage vectors, of which the space vector diagrams are shown in Figure 2. This means that depending on the switching modes, some voltage vectors represent more than one switching mode and have different CMV. From Table 2, seven switching states result in a zero CMV, whereas twelve modes have a CMV with Vdc/6 amplitude. Also, 6 have a CMV of Vdc/3, and the two remaining modes produce a CMV of Vdc/2. As shown in Figure 2, the space vector diagram can be divided into six triangular sectors (1 to 6), and each of these sectors can again be divided into four triangular areas (regions or subsectors) (1 to 4) [12]. When the reference voltage (V_{ref}) rests in an area of a sector, it can be made by the three nearest vectors based on the voltage-sec balance rule. For instance, when the reference voltage is located in region 3 of Sector 1, the voltage-sec balance rule can be written as Equation (1). For a sample time (Ts), the terms T1, T7, and T13 are the times corresponding to the vectors V1, V7, and V13, respectively. Notably, other voltage vectors can also be used to form a reference voltage, yet they adversely distort the harmonic content of the output waveforms.

$$V_{ref}T_S = V_1T_1 + V_7T_7 + V_{13}T_{13}$$
$$T_S = T_1 + T_7 + T_{13} \quad (1)$$

3. OPERATION AND MODULATION STRATEGY

3. 1. sinusoidal pulse width Modulation (SPWM)

SPWM, widely used in converters, is based on comparing sinusoidal reference and triangular carrier signals [18] due to its simplicity. This scheme can be applied to achieve zero CMV, where a triangular signal with three balanced sinusoidal modulation signals (V_{m1},

TABLE 1. Possible states of the NPC inverter per each phase

State	Phase a switches				Terminal Voltage
	S1	S2	S3	S4	
P	ON	ON	OFF	OFF	+Vdc/2
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-Vdc/2

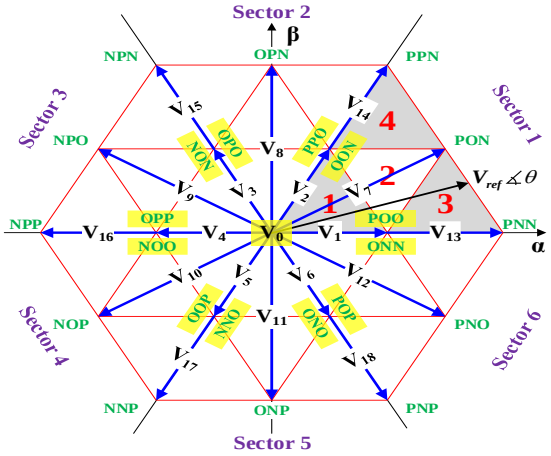


Figure 2. Space vector diagram for three-phase NPC inverter

TABLE 2. Overall switching states of the three-level NPC

State	Vector	Amplitude	CMV
[OOO]	V0	0	0
[NNN]	V0	0	-Vdc/2
[PPP]	V0	0	+Vdc/2
[POO]	V1	Vdc/3	+Vdc/6
[ONN]	V1	Vdc/3	-Vdc/3
[PPO]	V2	Vdc/3	+Vdc/3
[OON]	V2	Vdc/3	-Vdc/6
[OPO]	V3	Vdc/3	+Vdc/6
[NON]	V3	Vdc/3	-Vdc/3
[OPP]	V4	Vdc/3	+Vdc/3
[NOO]	V4	Vdc/3	-Vdc/6
[OOP]	V5	Vdc/3	+Vdc/6
[NNO]	V5	Vdc/3	-Vdc/3
[POP]	V6	Vdc/3	+Vdc/3
[ONO]	V6	Vdc/3	-Vdc/6
[PON]	V7	√3Vdc/3	0
[OPN]	V8	√3Vdc/3	0
[NPO]	V9	√3Vdc/3	0
[NOP]	V10	√3Vdc/3	0
[ONP]	V11	√3Vdc/3	0
[PNO]	V12	√3Vdc/3	0
[PNN]	V13	2Vdc/3	-Vdc/6
[PPN]	V14	2Vdc/3	+Vdc/6
[NPN]	V15	2Vdc/3	-Vdc/6
[NPP]	V16	2Vdc/3	+Vdc/6
[NNP]	V17	2Vdc/3	-Vdc/6
[PNP]	V18	2Vdc/3	+Vdc/6

V_{m2}, and V_{m3}) is used [15]. The following formulas describe this modulation method:

$$\begin{cases} V_a = m_a.\sin(\omega t) \\ V_b = m_a.\sin(\omega t - 2\pi/3) \\ V_c = m_a.\sin(\omega t + 2\pi/3) \end{cases}, \quad \begin{cases} V_{pulse,a} = (V_1 - V_2)/2 \\ V_{pulse,b} = (V_2 - V_3)/2 \\ V_{pulse,c} = (V_3 - V_1)/2 \end{cases} \tag{2}$$

where m_a is the index modulation, V_a, V_b, and V_c are the phase a, b, and c reference waveforms. Moreover, $V_{pulse,a\text{-}c}$ are the pulses of the NPC inverter, in which V_1-V_3 are the generated signals obtained from comparing reference waveforms and carriers. Then, considering Figure 1, the CMV (V_{no}) can be calculated as follows:

$$V_{no} = \frac{V_{ao}+V_{bo}+V_{co}}{3} = \frac{(V_1-V_2)+(V_2-V_3)+(V_3-V_1)}{3} = 0 \tag{3}$$

Note that the switching modes are selected only from the ones that produce a zero CMV. The voltage vectors mentioned above are used to generate the reference voltage in a way to eliminate the CMV. For example, when the reference voltage is in sector 1, the switching modes are selected sequentially from the ones according to the vectors V_0, V_7, and V_{14}. So, the voltage-second balance rule can be used to determine the time of each switching state as follows:

$$\begin{cases} V_{ref}.T_s = V_0.T_0 + V_7.T_7 + V_{12}.T_{12} \\ T_s = T_0 + T_7 + T_{12} \end{cases} \tag{4}$$

In practical applications, implementation of the modulation method depends on the system structure, applications, customer demand, etc. Therefore, other methods have been proposed in addition to the mentioned ones. A SHEPWM method with a passive typical mode filter is proposed to reduce the CMV and shaft voltage [19]. Yulin et al. [20] proposed two strategies to reduce the switching losses and increase the quality of the output waveform in their CMV reduction method, which is based on the injection of zero vectors by calculating the optimal time of (ΔT^s). Current predictive control has been increasingly used in power inverters due to precise current control, nonlinearity and system limitations, and low current ripple [21]. Hoseini et al. [22] proposed the AZSPWM-based predictive current control method is to reduce electromagnetic interference. Also, Vargas et al. [23] proposed a method based on sine wave pulse width modulation to reduce the CMV in a three-level NPC MLI.

3. 2. Simultaneous Modulation of Pulse width and Amplitude The pulse amplitude modulation (PAM) is applied simultaneously to PWM MLI. Suppose that the ability to change the pulse amplitude could be added to the power inverter, like changing the pulse width. In that case, the quality of conventional PWM control methods will be further improved [6]. The

PAM technique stabilizes the amplitude modulation index at specific values and instead changes the DC link voltage in the middle. Thus, a decrease in THD and improving the size of the output filter without increasing the switching frequency are resulted [24, 25]. According to the common methods of SHE-PWM and SHM-PWM, if the value of V_i (i = 1,2,…, n) is fixed as a coefficient of the DC link voltage, i.e., $V_i = V_{dc}$, the odd coefficients of b_n are represented as follows:

$$b_n = \frac{4v_{dc}}{n\pi}(cos(n\alpha_1)+cos(n\alpha_2)+...+cos(n\alpha_n)) \quad (5)$$

Accordingly, unknown angles (n) of α are considered degrees of freedom in solving equations resulting from this equation. Furthermore, by the equations obtained, the amplitude of the first harmonic can be controlled at $m_a \times nV_{dc}$, and the amplitude of the first (n-1) odd harmonics that are not a multiple of 3 can be decreased. In the SHM-PWM method, the problem-simplifying assumption of keeping the V_i constant is removed So that all V_i amplitudes can vary between 0 and Vdc. In this case, the degrees of freedom increase from n to 2n, and consequently, the variables of Equation (5) also increase. So, the optimal amplitude or amplitudes are found by solving the obtained equations and the optimal angles. Then, they can be used to control the amplitude of the first harmonic and lower harmonics to a higher order than before (6n-1) and reduce them even to zero [6, 26]. Considering m_a as the modulation index (defined by Equation (6)), the phase voltage for a two-level CB-PWM with a triangular carrier signal has a harmonic spectrum as Equation (7), where ω_F and ω_c represent the reference and the carrier frequencies, respectively. Also, i is the group index, j is the side band harmonic index of each group, φ is the carrier wave phase shift, θ is the phase shift of the reference wave, and J_0 and J_1 are the first-type Bessel functions.

$$m_a = \frac{\sqrt{3}\ V_{ref}}{V_{dc}}, \quad 0 \le m_a \le 1 \quad (6)$$

By generalizing Equation (7) for multilevel inverters, the phase voltage of an N-level inverter is as Equation (8). V is the voltage amplitude of the inverter's output, $h=h_0$ (N-1)/2, and h_0 is the phase voltage group index. This relation consists of three expressions: The first denotes the fundamental harmonic amplitude and directly relates to the amplitude modulation index. The second expression represents the amplitude of the output voltage harmonics at frequencies equal to the natural coefficients of the carrier frequency (the central harmonics of each group). It shows that if h is a natural number, there will be no harmonics at these frequencies. The third expression defines the amplitude of the sideband harmonics on both sides of the central harmonic. Regarding $\sin((2h+j)\frac{\pi}{2})$, odd-order sideband harmonics for even-order harmonics and even-order sideband harmonics for odd-order center harmonics exist. Figure 3 shows the calculated per unit (based on V) values of the phase voltage harmonics in terms of modulation index for three-level converters. Equation (8) states that each harmonic solely depends on the amplitude modulation index and is independent of the frequency modulation index (m_f) and the reference's angles and carrier waves.

It can be deduced that each modulation index's critical harmonic is the first group's central harmonic. If this harmonic equals zero, the sideband harmonics will be the most important and harmful. Otherwise, they lead to more losses. The dominant harmonic amplitude of the phase voltage reaches zero or its minimum value at one or more points on the horizontal axis. Therefore, if the amplitude modulation index is adjusted at these points, the effect of the dominant harmonic is minimized. This is the main advantage of the proposed CB-PWAM technique. According to Equation (8), the harmonic amplitude depends only on the size of the modulation index. It is independent of the frequency modulation index and angles of the reference and carrier waves. Accordingly, m_a and V_{dc} are the main factors determining the value of the fundamental component of the output waveform. The CB-PWAM technique eliminates or reduces the central or sideband harmonics of the first group without increasing the frequency. For this purpose, instead of using different modulation indices, m_a can always be considered equal to m_{opt}. In this case, to keep the amplitude of the fundamental harmonic constant, V_{dc} must vary by $V_{dc} \times m_a/m_{opt}$. An alternative method is to use the hybrid solution (9), in which $V_{dc\text{-}new}$ is the new value of the bus voltage [6].

4. PERFORMANCE EVALUATION

To evaluate the proposed method, the three-phase back-to-back NPC converter was simulated in MATLAB Simulink based on the parameters of Table 3. Accordingly, the simulation results for the input and

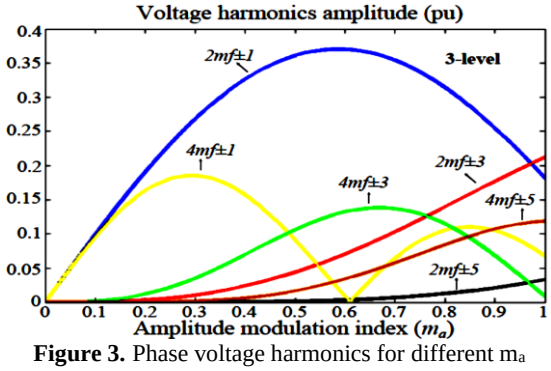


Figure 3. Phase voltage harmonics for different m_a

$$V_p(t)=m_a\frac{V_{dc}}{2}\cos(\omega_F t+\theta)+\frac{2V_{dc}}{\pi}\sum_{i=1}^{\infty}\frac{J_0(im_a\frac{\pi}{2})}{i}\sin(\frac{i\pi}{2})\cos(i(\omega_c t+\varphi)) + \frac{2V_{dc}}{\pi}\sum_{i=1}^{\infty}\sum_{j=\pm1}^{\infty}[\frac{Jj(im_a\frac{\pi}{2})}{i}\sin((i+j)\frac{\pi}{2})\times\cos(i(\omega_c t+\varphi)+j(\omega_F t+\theta))] \quad (7)$$

$$V_p(t)=m_aV_{dc}\cos(\omega_F t+\theta)+\frac{V_{dc}}{\pi}\sum_{h=1}^{\infty}\frac{J_0(hm_a\pi)}{h}\sin(h\pi)\cos(2h(\omega_c t+\varphi)) + \frac{V_{dc}}{\pi}\sum_{h=1}^{\infty}\sum_{j=\pm1}^{\infty}[\frac{Jj(hm_a\pi)}{h}\sin(2h+j)\frac{\pi}{2})\times\cos(2h(\omega_c t+\varphi)+j(\omega_F t+\theta))] \quad (8)$$

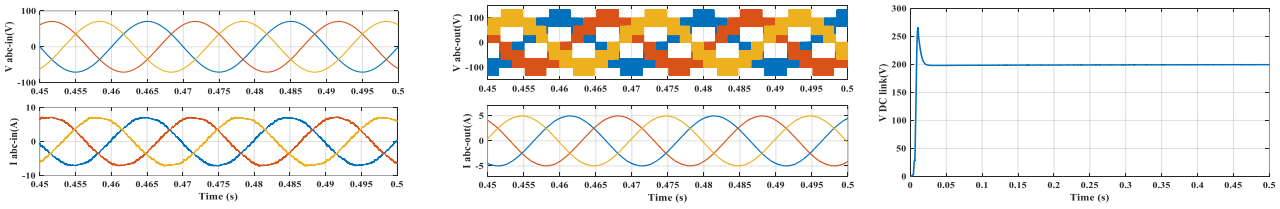
$$\begin{cases} m_a\le 0.61\rightarrow m_a=m_{opt}, & V_{dc,new}=V_{dc}\times\dfrac{m_a}{m_{opt}} \\ m_a>0.61\rightarrow m_a=1, & V_{dc,new}=V_{dc}\times m_a \end{cases} \quad (9)$$

output phase waveforms of the whole converter in steady-state mode are presented in Figure 4. The output power is 738 W leading to a 98.62 percent efficiency. Figure 4(c) shows that the DC link voltage overshoots initially and quickly settle on 200 V afterward. Yet, choosing larger capacitors dampens the overshoot and slows reaching the reference value. Applying the proposed method leads to a smooth input current with a unity power factor. In this condition, the harmonic content of the input current, output current, and voltage (without applying any filters) lead to a 2.73, 0.52, and 30.16 percent THD, respectively. Furthermore, the input and output line waveforms are included in Figure 5, where the output line voltage reaches 200 V. After all, the waveforms of resultant common mode voltages are shown in Figure 5(c), for the rectifier, inverter, and overall back-to-back converter. Notably, the amplitude of each CMV is less than 60 V, which is almost a quarter of the DC link voltage. To better evaluate the proposed method, the converter was also examined for various modulation indexes of the inverter ranging from 0.8 to 1.15 (Figure 6). The output power ranges from 500 to 900 W, while the efficiency slightly changes above 98 percent.

Obviously, the output power curve, as well as the efficiency one, varies according to the application, resulting in a different intersection point as a reference to choose the optimal modulation index. Moreover, the selection of M_a depends on the desired input current THD, as well. Since the utility grid supplies the converter, it is essential that the input current THD remains below 5 percent (IEEE std.519-2014). Meanwhile, increasing M_a leads to a decline in input current THD and a significant drop in the load voltage THD. A 700 W prototype of the three-level back-to-back converter was implemented to verify the simulation results (Figure 7). The proposed controller is applied by the DSP TMS320F28335. Figure 7.a depicts the rectifier side waveforms where the phase 'a' input current is in phase with the corresponding input voltage signifying the unity power factor. Moreover, the DC link voltage is regulated at 200 V with the help of the proposed method.

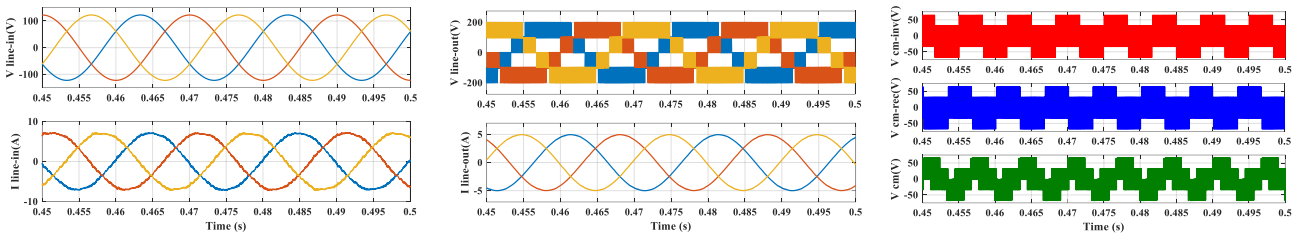
TABLE 3. Switching states of the three-level NPC inverter

Parameter	Value
Grid phase voltage (RMS)	50 V
Grid frequency	50 Hz
Switching Frequency	10 kHz
DC link voltage	200 V
DC link capacitors	C1=C2=3300 µF
Modulation index	0.95
Input filter	0.014 Ω+2 mH
Load	20 Ω+30 mH



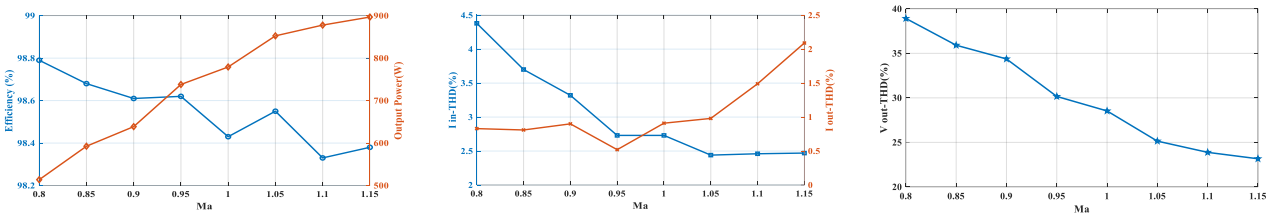
(a) (b) (c)

Figure 4. Phase waveforms: (a) rectifier's input and (b) inverter's output, (c) DC-Link voltage



(a) (b) (c)

Figure 5. Line waveforms: (a) rectifier's input and (b) inverter's output, and (c) CMV



(a) (b) (c)

Figure 6. Simulation results for the converter: (a) efficiency, (b) current THD, and (c) load voltage THD for various values of Ma

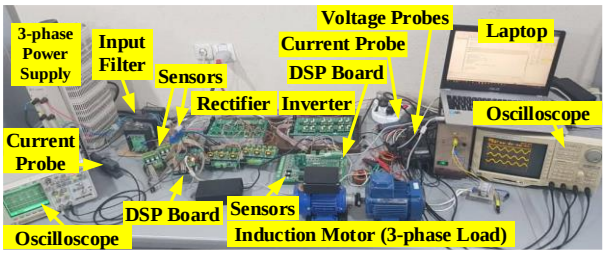
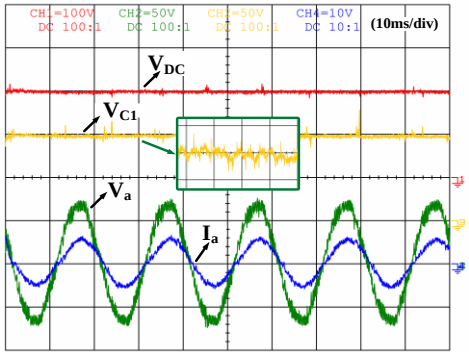
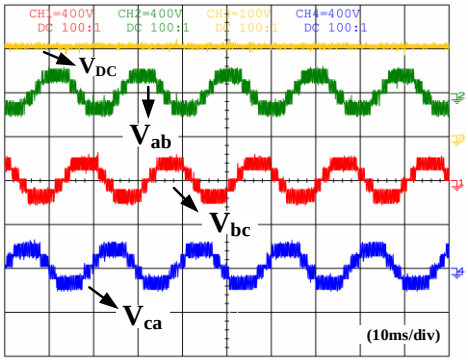


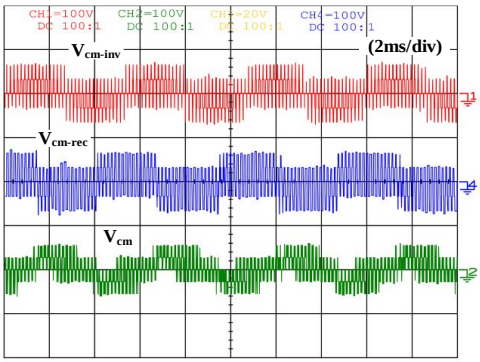
Figure 7. Test setup



(a)



(b)



(c)

Figure 8. Experimental results for the waveforms of (a) rectifier, (b) inverter, and (c) CMV

In addition, as it is noticeable from the DC link and C_1 voltages, the capacitors' voltages are balanced. Figure 8.b describes the inverter's three-phase voltages. As can be perceived, all three voltages are symmetrical, and the proposed method can properly generate the reference voltage. Figure 8.c shows the common mode voltage of the inverter, rectifier, and the total back-to-back system. Notably, the total CMV's amplitude is also considerably low and symmetrical. In such conditions, the harmonic spectrum of the inverter's phase 'a' voltage is displayed in Figure 9.a, where its THD is 10.4 percent. Also, the harmonic spectrum of the rectifier's phase 'a' current is demonstrated in Figure 9.b, having a THD of 1.4 percent, satisfying the IEEE-519-STD.

Figure 10 illustrates the transient response of the converter when the output load alters from full-load to no-load and then from no-load to full-load condition. As can be seen, the controller reacts rapidly to this change

and the DC-link and C1 voltages. Moreover, the rectifier responds smoothly to this variation. It is noticed that the inverter output voltage performance is acceptable and follows the reference value during the test. Consequently, the system's stability is ensured despite sudden changes in the converter's operating point.

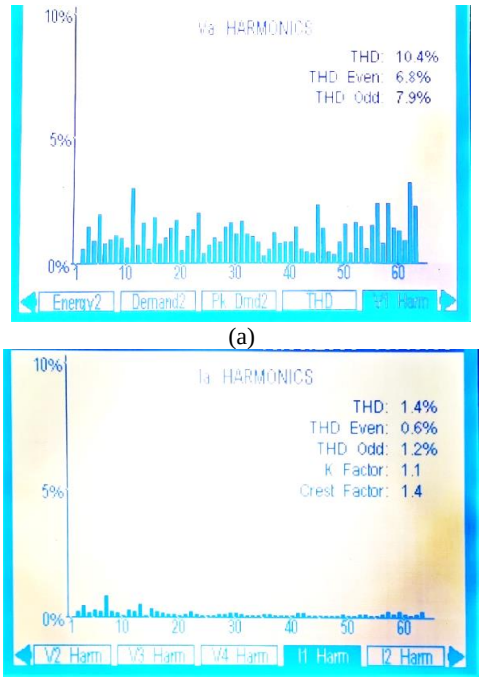


Figure 9. The experimental harmonic content of the output waveforms for phase A of (a) inverter's voltage and (b) rectifier's current

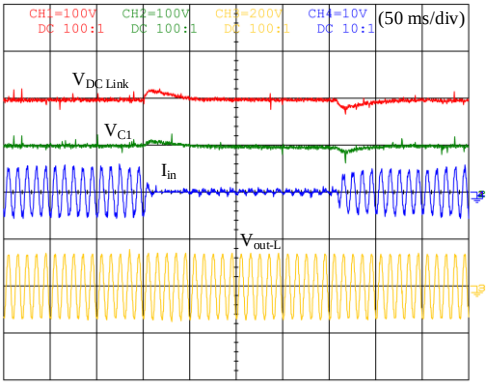


Figure 10. Transient response of the proposed technique

5. CONCLUSION

This paper proposed a novel modulation strategy to reduce the common mode voltage of non-sinusoidal voltages generated by multilevel inverters. Considering the significance of the back-to-back converters in industries on the one hand and the possible adverse impacts of CMV along with rapid voltage changes in high-frequency switching, on the other hand, requires further attention. Accordingly, a combination of simultaneous pulse width and amplitude modulation with space vector modulation technique is addressed to tackle this issue. In this regard, eliminating the zero vectors of the voltage waveform and regulation of the DC link voltage by amplitude modulation are applied. Applying the proposed strategy to a three-phase three-level NPC back-to-back converter resulted in an efficiency of 96.62 percent. Also, the input current THD of 2.73 percent was achieved with a unity power factor, whereas the THD for the output current was 0.52. These results are for a 738-watt prototype at the operating point with a 0.95 modulation index. Consequently, the proposed technique is suitable for various ASD, transmission lines, industrial, and residential applications.

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Persian Abstract

چکیده

مبدل‌های پشت‌به‌پشت سه‌فاز به‌طور گسترده در کاربردهای مختلف صنعتی، تجاری و خانگی مانند درایوهای موتور AC کاربرد دارند. با توجه به ولتاژهای غیرسینوسی که تولید می‌کنند، یک ولتاژ حالت مشترک ظاهر می‌شود که منجر به مشکلاتی در سیستم‌های محرک الکتریکی و کاربردهای فرکانس بالا می‌شود. CMV، همراه با تغییرات سریع ولتاژ، می‌تواند باعث مشکلات جدی از جمله جریان‌های نشتی که از خازن‌های انگلی داخل موتور عبور می‌کنند، تداخلات الکترومغناطیسی، ولتاژ شفت و جریان‌های بلبرینگ که طول عمر موتور را کاهش می‌دهند، شود. بنابراین، طراحان سیستم محرکه می‌بایست CMV و تداخل الکترومغناطیسی و همچنین، روش‌های کاهش آن‌ها را به‌عنوان عوامل مهم در طراحی خود در نظر بگیرند تا از اثرات نامطلوب آنها جلوگیری شود. به طور کلی، تحقیقات برای کاهش این اثرات به دو روش اصلاح ساختار فیزیکی سیستم محرک یا بهبود الگوریتم کنترل اینورتر تقسیم می‌شود. روش‌های مدولاسیون عرض پالس معمولاً در الگوریتم‌های کنترل مبدل‌ها برای کاهش CMV استفاده می‌شوند. با این حال، روش مدولاسیون همزمان پهنای پالس و دامنه بردارهای فضایی در این مقاله برای کاهش CMV و اثرات مخرب آن در سیستم های محرک پیشنهاد شده‌است. روش پیشنهادی، بر اساس حذف بردارهای صفر و کاهش ولتاژ لینک DC ناشی از مدولاسیون دامنه، منجر به کاهش بیشتر CMV می‌شود. سپس، استراتژی پیشنهادی روی یک مبدل NPC پشت‌به‌پشت سه‌فاز در نقطه کار ۷۳۸ وات اعمال می‌شود. نتایج به‌دست‌آمده، رفتار مناسب سیستم را با بازده ۹۸.۶۲ درصد را نشان می‌دهد. در نهایت، عملکرد گذرا مبدل از حالت بی‌باری به بار کامل، رفتار مناسب آن را برای کاربردهای صنعتی تضمین می‌کند.