



Dual Output Voltage Differencing Buffered Amplifier Based Active -C Multiphase Sinusoidal Oscillator

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ABSTRACT

A multiphase sinusoidal oscillator (MSO) using dual output voltage differencing buffered amplifier (DO-VDBA) is presented in this paper which provides n equally spaced phase sinusoids of equal magnitudes. The proposed MSO topology is realized using the first order all pass network (APN). In the proposed structure the output voltages are made available at low impedance nodes which makes the proposed MSO easy for cascading. Making the proposed structure a resistorless structure is a major challenge. The main benefits of the structure are easy integration and less power losses. The formulation of frequency and condition of oscillation is derived mathematically. The oscillation frequency can be tuned electronically, is an added advantage of the proposed MSO. The effect of device non-idealities is also discussed in the study. To assess the proposed MSO performance further Monte Carlo analysis was carried out. The workability of the proposed structure is verified through SPICE simulations for a three ($n=3$) and four ($n=4$) phases MSO, and the obtained simulated results are in close agreement with the theoretical values. The total harmonic distortion (THD) is found to be quite low.

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NOMENCLATURE

C	Capacitance
n	Nano
A	Ampere
V	Volt
μ	Micro

Greek Symbols

ε	Tracking Error
α	$1-\varepsilon_{gm}$
β	$1-\varepsilon$

1. INTRODUCTION

The multiphase sinusoidal oscillators (MSO) generate multiple (≥ 3) sinusoidal signals of the same frequency which are equally spaced in phase. The widespread usage of MSO in telecommunication systems, power electronics, instrumentation, radar system and control systems is well known.

A large number of MSOs realization are available in the literature [1-22]. The available literature suggests that VDBA based MSO has not been realized so far; though a variety of MSOs has been designed using different active building blocks (ABB). These existing structures use n cascaded phase shifting networks such as first order low pass networks (LPNs) [1-4, 6-10, 12, 13, 17, 19], first

order all pass networks (APNs) [5, 14-16, 18, 20] or first order high pass networks (HPNs) [11] in closed loop.

The available literature can be classified as voltage mode (VM) [1-9, 11, 12, 19, 20], or current mode (CM) [10, 11, 13-15, 18] configurations according to the output signal provided by MSO. The MSOs [1-5] realized using operational amplifiers (Op-Amp) have limited high frequency operation due to constant gain-bandwidth product and lower slew rate. To produce high frequency oscillations different current mode ABBs have been used such as second generation current conveyor (CCII) [6-11, 22] current differencing transconductance amplifier (CDTA) [14, 15], current differencing unit (CDU) [16], current feedback operational amplifier (CFOA) [17, 21], current controlled CDTA (CCCDTA) [18], and

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operational transresistance amplifier (OTRA) [19, 20]. Moreover, these structures are capable of producing the high frequency oscillation. However, they suffer from few limitations including the number of active blocks per phase, the number of passive components, availability of output voltage at high impedance node. This paper presents a dual output voltage differencing buffered amplifier (DO-VDBA) based MSO consisting of n APN in a closed loop.

The DO-VDBA consists of an input voltage differencing stage and the output current is equal to transconductance times the difference of voltages. Further, a voltage terminal at low impedance is also available, thus adding design flexibility. Thus it can be understood as a transconductance amplifier (TA) followed by a voltage buffer (inverting/non-inverting). Bias dependent transconductance adds the feature of electronic tunability

of circuit parameters. Thus, the DO-VDBA has emerged as a promising choice for both VM and CM analog applications in the recent past. Since several structures of MSOs are available, a comparison Table 1 is drawn based on a) ABB, b) number of ABB required for per phase generation, c) mode of signal d) output impedance, e) design methodology f) no of passive components g) electronic tunability and h) the technology used.

It may be observed from Table 1 that, Opamp based structures have limited high-frequency operations [1-5]. MSOs provide voltage output at high impedance [6-9, 11, 12]. Structures presented in literature [1, 2, 8, 17] are not tunable as they make use of parasitic capacitance; MSOs provide current outputs so additional circuitry is required to convert it to voltage for driving voltage inputs circuits [10, 11, 13-15, 18], only limited structures provide electronic tunability [12-15, 18]. The MSO uses two

TABLE 1. Comparison with the previously available Multiphase sinusoidal oscillators

Ref.	ABB	No of ABB/ Phase	Mode of Output CM/VM operation Or mode of operation	Output Impedance	Design Technique	(R+C)/ Phase	Tunability/ Electronic control	Technology used
[1]	OpAmp	1	VM	Low	LPN	2+0	N/N	Op-Amp 741
[2]	OpAmp	1	VM	Low	LPN	2+0	N/N	Op-Amp 741
[3]	OpAmp	1	VM	Low	LPN	3+1	Y/N	LF351
[4]	OpAmp	1	VM	Low	LPN	2+1	Y/N	OPA 351 HA 2544
[5]	OpAmp	1	VM	Low	APN	3+1	Y/N	LF 351 HA 2533C Exp
[6]	CCII	1	VM	High	LPN	2+1	Y/N	AD844AN
[7]	CCII	1	VM	High	LPN	2+1	Y/N	AD844
[8]	CCII	1	VM	High	LPN	2+0	N/N	--
[9]	CCII	1	VM	High	LPN	2+1	Y/N	AD844Exp
[10]	CCII	1	CM	High	LPN	0+2	Y/N	Bipolar PR200N and R200N
[11]	CCII	1	VM	High	HPN	1+2	Y/N	CA 3096 E
[12]	OTA	1	VM	High	LPN	1+1	Y/N	CA3080
	OTA+buffer	1	VM	High	LPN	2+1	Y/N	
	OTA	2	VM	High	LPN	0+1	Y/Y	
[13]	OTA+buffer	1	VM	High	LPN	0+3	Y/Y	BipolarPR100N and NP100N
	CDTA	1	CM	High	LPN	0+1	Y/Y	
	CDTA	2	CM	High	APN	0+1	Y/Y	
[14]	CDTA	2	CM	High	APN	0+1	Y/Y	BipolarPR100N and NP100N
[15]	CDTA	1	CM	High	APN	2+1	Y/Y	BipolarPR200N and NP200N
[16]	CDU	1	VM	High	APN	1+1	Y/N	CMOS 0.7 μ m technology
[17]	CFOA	1	VM	Low	LPN	2+0	Y/N	AD844AN
[18]	CCCDTA	1	CM	High	APN	1+1	Y/Y	0.25 μ m CMOS technology
[19]	OTRA	1	VM	Low	LPN	2+1	Y/N	AD 844
[20]	OTRA	1	VM	Low	APN	3+1	Y/N	0.35 μ m TSMC CMOS technology
[21]	AOFC	2	MV	woL	APN	5+1	N/N	AD 844
Proposed	DO-VDBA	1	VM	Low	APN	0+1	Y/Y	0.18 μ m CMOS

ABBs per phase as against the rest of the structures [14, 21], only a few realizations are active C structures [10, 12-14].

Thus, this communication aims at presenting a new active – C MSO design using DO-VDBA based on APNs which overcomes all the limitations of existing structures and is the best suitable for voltage mode operations. Several applications have been used by many researchers in different fields including electronics [23-27] and others [28-32] using new advancements in technologies. The pros of the proposed MSO, when compared to the existing structures are that

- The proposed is resistorless giving the advantage of low power losses and better integration.
- The novelty of the current study is that MSO designed using DO-VDBA with zero resistors were explored very limited in previous researches.
- Moreover, a resistorless multiphase oscillator with DO-VDBA has not been studied in the past that makes the work new in the area.
- The proposed MSO provides a voltage output at a low impedance node. Therefore, no extra circuitry is required.
- The frequency of oscillation is electronically tunable.

2. PROPOSED DO-VDBA BASED ACTIVE -C MSO

The DO-VDBA is a five terminal element characterized by two high impedance voltage input terminals (p and n), one high output impedance terminal z and two low impedance inverted/non-inverted buffered output terminals (w-,w+), respectively; which makes it more flexible for circuit design applications as compared to other ABBs [22, 25-26].

The symbolic representation of DO-VDBA is given in Figure 1 and the port relationship is described by the matrix (1).

$$\begin{bmatrix} I_z \\ V_{w+} \\ V_{w-} \\ I_p \\ I_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & g_m & -g_m \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_{w+} \\ I_{w-} \\ V_p \\ V_n \end{bmatrix} \tag{1}$$

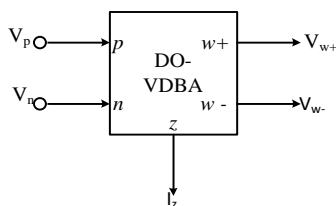


Figure 1. The circuit symbol of VDBA

where g_m represents the transconductance gain from input to z terminal of DO-VDBA. The DO-VDBA [24] based APN presented by Sotner et al. [23] and reproduced in Figure 2 is used for the proposed MSO realization.

The transfer function of the APN may be written as follows:

$$G(s) = \frac{V_o}{V_{in}} = \frac{g_m - sC}{g_m + sC} = \frac{1 - s \frac{C}{g_m}}{1 + s \frac{C}{g_m}} \tag{2}$$

The proposed MSO is shown in Figure 3 and its loop gain can be expressed as follows:

$$L(s) = - \left(\frac{1 - s \frac{C}{g_m}}{1 + s \frac{C}{g_m}} \right)^n \tag{3}$$

As per Barkhausen's criterion if the loop gain at a frequency ω_0 , is unity the system results in sustained oscillation. Thus the proposed topology will provide sinusoidal oscillations if its loop gain is expressed as follows:

$$L(j\omega_0) = -A^n \left(\frac{1 - j\omega_0 \frac{C}{g_m}}{1 + j\omega_0 \frac{C}{g_m}} \right)^n = 1 \tag{4}$$

Thus the magnitude and phase response for Equation (4) can be found as Equations (5) and (6), respectively.

$$|L(j\omega_0)| = 1 \tag{5}$$

$$\angle L(j\omega_0) = 0 \tag{6}$$

As each APN provides an identical phase shift (ϕ), then the total phase shift of the loop (ϕ_t) to satisfy the Barkhausen Criteria for oscillations is given by the following expressions:

$$\phi_t = n\phi + \pi = 2\pi \tag{7}$$

$$\phi = \frac{\pi}{n} \tag{8}$$

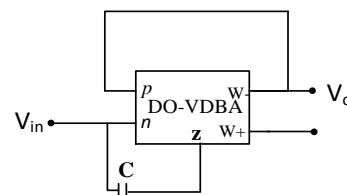


Figure 2. APN using DO-VDBA [25]

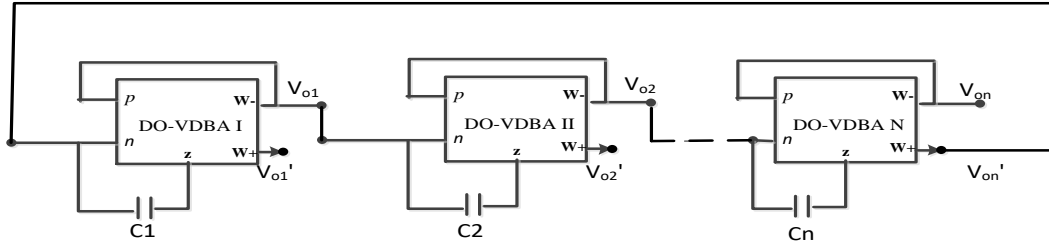


Figure 3. The proposed DO -VDBA based Active C MSO

Thus the condition of oscillation (CO) can be computed as CO: $A=1$ (9)

and the frequency of oscillation (FO) can be enumerated as follows:

$$f_o = \frac{g_m}{2\pi C} \tan\left(\frac{\pi}{2n}\right) \quad (10)$$

It may be observed from Equation (10) that the FO can be varied either by changing the value of C or can be electronically tuned through gm by varying the bias current.

3. NON-IDEALITY

The performance of the proposed MSO may deviate from the ideal one due to the deviation of the internal current and voltage transfer of VDBA from unity. These deviations amend the terminal characteristics as follow:

$$\begin{bmatrix} I_z \\ V_{w+} \\ V_{w-} \\ I_p \\ I_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \alpha g_m & -\alpha g_m \\ \beta_p & 0 & 0 & 0 & 0 \\ -\beta_p & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_{w+} \\ I_{w-} \\ V_p \\ V_n \end{bmatrix} \quad (11)$$

where $\alpha=1-\epsilon_{gm}$. The ϵ_{gm} ($|\epsilon_{gm}| \ll 1$) are transconductance tracking errors. The $\beta_p=1-\epsilon_p$ where ϵ_p ($|\epsilon_p| \ll 1$) represents the voltage tracking error from z terminal to w+. Similarly $\beta_n=1-\epsilon_n$ with ϵ_n ($|\epsilon_n| \ll 1$) being the voltage tracking error from z terminal to w- terminal. Considering these non-idealities into account the G(s) is modified as G(s)_{-n}.

$$G(s)_{-n} = \frac{1}{\beta_n} \frac{1-s \frac{C}{\alpha g_m}}{1+s \frac{C}{\alpha \beta_n g_m}} \quad (12)$$

$$L(s)_{-n} = -\beta_p \left(\frac{1}{\beta_n}\right)^n \left(\frac{1-s \frac{C}{\alpha g_m}}{1+s \frac{C}{\alpha \beta_n g_m}}\right)^n \quad (13)$$

The non-ideal gains create some deviation in the transfer function. However, these small deviations can be compensated by properly adjusting the transconductance gains (g_m) of the VDBAs.

4. SIMULATION RESULTS

The proposed MSO has been validated through SPICE simulations using TSMC CMOS 0.18 μm technology. The CMOS DO-VDBA [23] which is reproduced in Figure 4 is used for simulation. Table 2 enlists the aspect ratios of the respective transistors. The supply voltages used are ± 1 V and the bias current I_b is set to $40\mu\text{A}$. The g_m of the DO-VDBA is given by the following expression:

$$g_m = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{3,4} I_b} \quad (14)$$

The simulated value of g_m is observed to be $200\mu\text{A/V}$ against its theoretical value of $209\mu\text{A/V}$. The power consumption is observed to be 4 mW.

A simulation setup is arranged to get the output of the MSO of Figure 3 for $n=3$, for which values of all capacitors ($C_1=C_2=C_3$) are chosen as 5 pF. The steady-state output is shown in Figure 5(a) while the frequency spectrum is depicted in Figure 5(b). The simulated frequency of oscillations is observed to be 3.5 MHz against the theoretical value of 3.6 MHz. Total harmonic distortion (THD) was observed to be 0.78% which is a substantially low value.

Further, the proposed MSO was simulated for $n = 4$ and while capacitance values are still set as 5 pF. This results in a theoretically calculated FO of 2.6 MHz. The simulated steady-state output and corresponding frequency spectrum are depicted in Figures 6(a) and 6(b),

TABLE 2. Aspect Ratios

Transistor	(W/L) μm
M ₁ -M ₄	7.2/1.8
M ₅ -M ₈	27/0.54

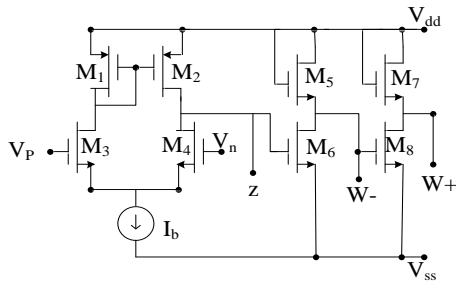


Figure 4. CMOS implementation of DO-VDBA [23]

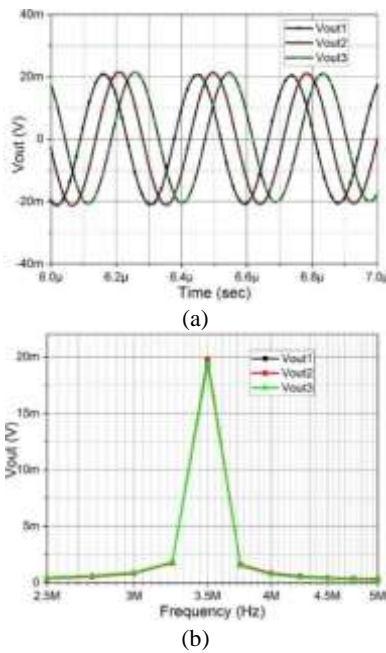


Figure 5. Simulated output for 3 phase MSO (a) Steady-state; (b) frequency spectrum

respectively. The simulated FO is observed to be 2.5 MHz and the THD as 1.19%.

Tuning of FO of 3 phase MSO with capacitance is depicted in Figure 7(a) and the variation of oscillating frequency with bias current I_{bias} is presented in Figure 7(b). It may be observed that the simulated frequencies closely follow the theoretical values.

To check the robustness and effect of parameter variations of the proposed MSO, the Monte-Carlo statistical analysis is done via simulation. Monte carlo analysis was carried out keeping $n=4$ and the resultant histogram obtained is shown in Figure 8. First, the 5% variation in the value of C is done and followed by considering 5% deviation in mobility, threshold voltage and oxide thickness to investigate the effect of mismatch on the frequency of oscillation. It is observed that the value of oscillation frequency remains close to its theoretical value of 2.6 MHz and hence almost unaffected by the parameter variations. Thus, it is worth mentioning

that proposed structure is almost immune to parametric variations.

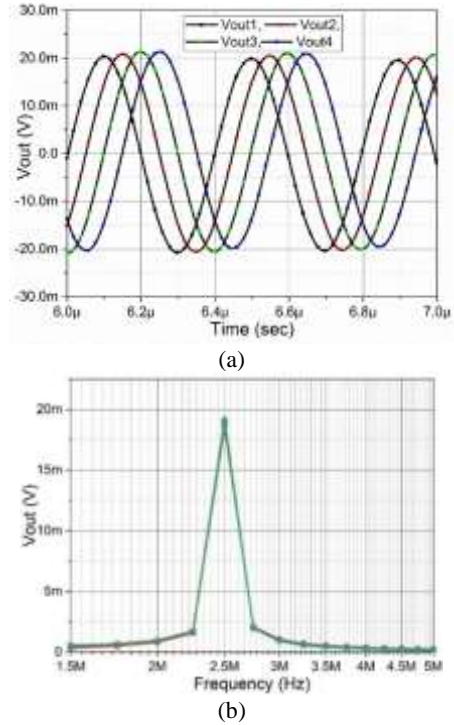


Figure 6. Simulated output for 4 phase MSO (a) Steady-state; (b) frequency spectrum

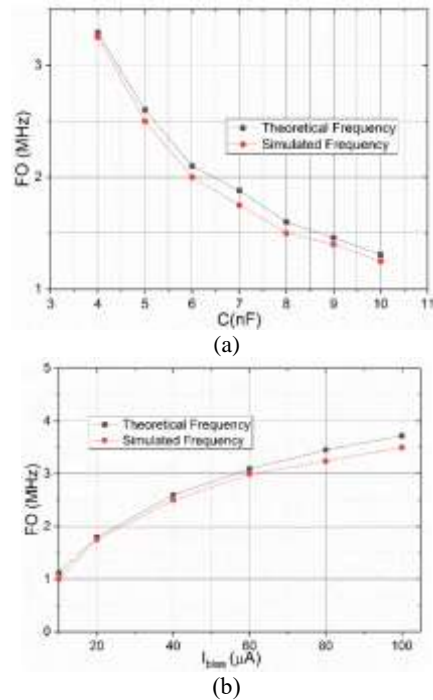


Figure 7. (a) FO vs C; (b) FO vs I_{bias}

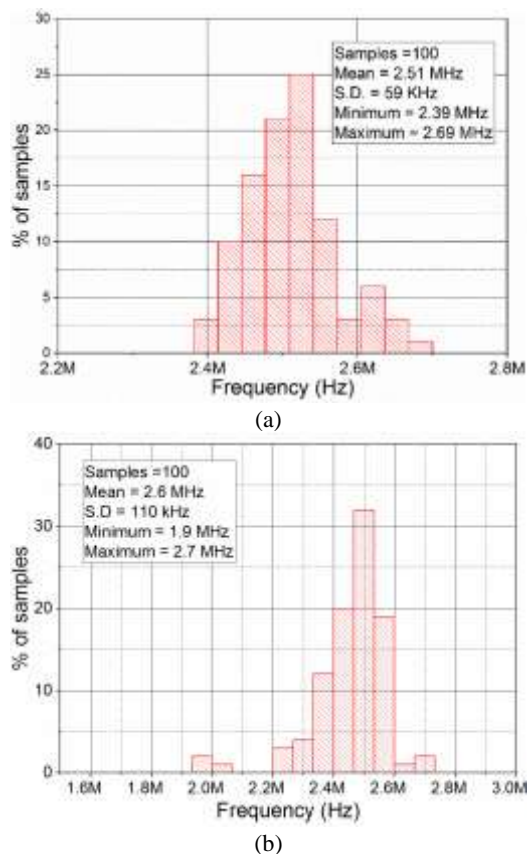


Figure 9. Monte Carlo simulation

5. CONCLUSION

An n phase Active-C MSO topology using DO-VDBAs was proposed in this paper. The proposed structure is a resistorless structure. The proposed structure provides n phase oscillations at low impedance nodes. As the proposed circuit provides output at low impedance nodes, so it can be readily used to drive voltage input circuits without needing any extra circuitry. Also, the frequency of oscillation can be tuned electronically. The effect of device non-idealities on the proposed MSO was analyzed. The functionality of the proposed MSO is verified through SPICE simulations for two instance cases (three and four-phase MSOs). The simulation results are found to be in close agreement with the theoretical values. Monte Carlo analyses have also been carried out to evaluate the robustness of the proposed structure. For future works, experimental analysis and validation of results shall be carried out using the off shelf ICs.

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Persian Abstract

چکیده

یک اسپلاتور سینوسی چند فازی (MSO) با استفاده از تقویت کننده بافر تفکیک کننده ولتاژ خروجی دوگانه (DO-VDBA) در این مقاله ارائه شده است که n سینوسی فازی با اندازه مساوی با فاصله یکسان را ارائه می دهد. توپولوژی پیشنهادی MSO با استفاده از شبکه مرتب سازی برای اولین بار (APN) تحقق می یابد. در ساختار پیشنهادی ولتاژهای خروجی در گره های با امپدانس کم در دسترس قرار می گیرند که MSO پیشنهادی را برای انعطاف پذیری آسان می کند. ساخت ساختار پیشنهادی به عنوان سازه ای بدون مقاومت یک چالش اساسی است. مزایای اصلی سازه یکپارچه سازی آسان و اتلاف انرژی کمتر است. فرمول بندی فرکانس و شرایط نوسان از نظر ریاضی مشتق شده است. فرکانس نوسان را می توان به صورت الکترونیکی تنظیم کرد، یک مزیت اضافی برای MSO پیشنهادی است. اثر غیر ایده آل بودن دستگاه نیز در این مطالعه مورد بحث قرار گرفته است. برای ارزیابی عملکرد پیشنهادی MSO تجزیه و تحلیل مونت کارلو بیشتر انجام شد. کارایی ساختار پیشنهادی از طریق شبیه سازی SPICE برای سه فاز MSO ($n = 3$) و چهار ($n = 4$) تأیید می شود و نتایج شبیه سازی شده به دست آمده با مقادیر نظری مطابقت نزدیک دارند. اعوجاج هارمونیک کل (THD) کاملاً کم است.
