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Reducing Quantum Cost for Reversible Realization of Densely-packed-decimal Converters

S. Diamond Thabah, P. Saha*

Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, Shillong, India

P A P E R I N F O

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A B S T R A C T

At present, the reduction of circuit design power is a prime research topic. The reversible computation satisfies the criteria of the power consumption reduction compared to the traditional logic design. Thereby, reversible computation is gaining much attention in recent decades. Two reversible design approaches of binary-coded-decimal (BCD) to densely-packed-decimal (DPD) converter (encoder) and two design approaches of DPD to BCD converter (decoder) are proposed in this paper. The designs are carried out through the appropriate selection of the gates and further proper organization of such gates with parallel implementation. The proposed design approaches offer a low quantum cost implementation compared to state-of-the-art design. The cost results analysis of reversible DPD encoder shows appreciable reduction by at least ~23%, and that of decoder by at least ~62% compared to the state-of-art design found in the literature. Furthermore, the structures are decomposed into the primitive-quantum-gates and compressed in compact form for delay calculation.

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NOMENCLATURE

K	Boltzmann's constant	**Symbols**	
T	Absolute temperature	Δ	A unit delay

1. INTRODUCTION

The inaccuracy errors and exactness problem using the binary representation of decimal numbers for decimal calculations are not acceptable in commercial and financial systems. Thus, decimal representation is necessary for decimal calculations of such data sets. In 2019, the IEEE standard for floating-point arithmetic [1] was revised (from the IEEE 754-2008), where the significand part of the decimal number format is represented by the densely-packed-decimal (DPD) encoding [2]. The DPD encoding is an approach where three decimal digits can be represented by 10 bits than 12 bits in pure binary-coded-decimal (BCD). The hardware encoding/decoding approach of such coding can be achieved with only 2-3 gate delays. However, circuit design for low power consumption of such an encoder/decoder is challenging for researchers.

In 1961, Landauer [3]stated that the circuits' hardware computation through the classical gates results in information loss; that is, each bit loss contributed at least $KTln2$ Joules of energy, where K is the Boltzmann's constant and T is the absolute temperature. However, in 1973, Bennett [4] showed that such energy loss was removed using reversible methodology, which can be achieved through reversible gates. These reversible gates/circuits sustained their reversibility with the equivalent number of input and output lines. Also, the mapping between inputs and outputs must be unique such that the information can be processed from the outcomes uniquely. Some restrictions in reversible computing are the fan-out as well as feedback.

Reversible implementation of arithmetics circuits such as reversible adder and reversible multiplier [5-6] has gained interest over the last decades, where low power designs are achievable. In 2006, an approach for

*Corresponding Author Institutional Email: *prabir.saha@nitm.ac.in* (P. Saha)

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the reversible implementation of DPD encoder and decoder from and to BCD was proposed [7], where they use two reversible gates, namely, Feynman gate (FG) [8] and Toffoli gate (TG) [9]. However, both the design approaches (for encoder and decoder) possess a higher quantum cost (QC) of 199 and 612, respectively. Thus, in this paper, two reversible design approaches for encoder and decoder respectively are proposed to minimize the QC where it utilizes reversible gates such as FG, TG, Peres gate (PG) [10], and BJN gate [11]. The cost results analysis of reversible DPD encoder shows appreciable reduction by at least ~23%, and that of decoder shows a significant reduction of at least ~62% compared to the state-of-art design found in the literature.

2. REVERSIBLE LOGIC CONCEPTS

Reversible logic involves designing hardware circuits using the same count of input lines and output lines. Reversible gates used in this paper are listed and shown in Table 1.

3. DENSELY-PACKED-DECIMAL CONVERTERS

3. 1. Encoder Design The encoder converts the three decimal digits from BCD (letters a through k, and m) format into DPD (p through y) format, where it constitutes twelve inputs and ten outputs. The encoder implementation is according to the following simplified expression shown in Equation (1) [2]:

$$\begin{aligned} p &= b + (a\,j) + (a\,f\,i) \\ q &= c + (a\,k) + (a\,g\,i) \\ r &= d \\ s &= (f\,(\bar{a} + \bar{\imath})) + (\bar{a}\,e\,j) + (e\,i) \\ t &= g + (\bar{a}\,e\,k) + (a\,i) \\ u &= h \\ v &= a + e + i \\ w &= a + (e\,i) + (\bar{e}\,j) \\ x &= e + (a\,i) + (\bar{a}\,k) \\ y &= m \end{aligned} \tag{1}$$

3. 2. Decoder Design The decoder performs the conversion of the DPD data into original BCD data. The decoder with ten inputs (letters, p through y) and twelve outputs (letters a through k, and m) has the following simplified Boolean expression shown in Equation (2) [2]:

TABLE 1. Reversible gates with logic equations and QC

GATES	EQUATIONS	QC
FG [8]	P=A, Q=A⊕B	1
TG [9]	P=A, Q=B, R=AB ⊕C	5
PG [10]	P=A, Q=A⊕B, R=AB⊕C	4
BJN [11]	P=A, Q=B, R=(A+B)⊕C	5

$$\begin{aligned} a &= (v\,w)\,(\bar{s} + t + \bar{x}) \\ b &= p\,(\bar{v} + \bar{w} + (x\,s\,\bar{t})) \\ c &= q\,(\bar{v} + \bar{w} + (x\,s\,\bar{t})) \\ d &= r \\ e &= v\,((\bar{w}\,x) + (\bar{t}\,x) + (s\,x)) \\ f &= \big(s\,(\bar{v} + \bar{x})\big) + (p\,v\,w\,x\,\bar{s}\,t) \\ g &= \big(t\,(\bar{v} + \bar{x})\big) + (q\,w\,\bar{s}\,t) \\ h &= u \\ i &= v\,((\bar{w}\,\bar{x}) + \big(w\,x\,(s + t)\big)) \\ j &= (w\,\bar{v}) + (s\,v\,\bar{w}\,x) + (p\,w\,\big(\bar{x} + (\bar{s}\,\bar{t})\big)) \\ k &= (x\,\bar{v}) + (t\,\bar{w}\,x) + (q\,v\,w\,\big(\bar{x} + (\bar{s}\,\bar{t})\big)) \\ m &= y \end{aligned} \tag{2}$$

4. PROPOSED DESIGN APPROACHES FOR REVERSIBLE DENSELY-PACKED-DECIMAL CONVERTERS

4. 1. Reversible Encoder From BCD to DPD Two design approaches are proposed for the reversible realization of the BCD-to-DPD encoder (B2DE). The realization of the first proposal (design 1) of reversible B2DE is through twenty-seven gates (that is, with the combination of the three gates, namely, FG, TG, and PG) as shown in Figure 1. The encoder's inputs are letters, a through c, e through g, and i through k, whereas the outputs are letters p, q, s, t, v, w, and x as shown in Figure 1. However, the inputs d, h, and m and the outputs r, u, and y are not engaged in the circuit (Figure 1) since the inputs directly contributed to the outputs. To obtained the required B2DE circuit (using Equation (1)), twenty-seven constant inputs (CIs) were integrated into the inputs of the reversible gates, which results in a total of twenty-nine garbage outputs (GOs) in the circuit.

The second proposal (design 2) implemented with twenty-nine reversible gates where an additional gate, namely, BJN gate, is combined with FG, TG, and PG, as shown in Figure 2. Similarly, the encoder's inputs are letters, a through c, e through g, and i through k, whereas the outputs are letters p, q, s, t, v, w, and x as shown in Figure 2. The inputs d, h, and m are directly conferred to the outputs r, u, and y, respectively. As shown in Figure 2, the design involved twenty-nine CIs to achieve the circuit's necessary function, directing thirty-one GOs in the outputs.

4. 2. Reversible Decoder From DPD to BCD For the reversible realization of DPD-to-BCD decoder (D2BD), two design approaches are proposed: design 1 and design 2, respectively. Design 1 of reversible D2BD is implemented with the help of FG, TG, and PG, as shown in Figure 3, where it employed a total of fourty eight reversible gates to perfect the circuit (using Equation (2)). The decoder's inputs are p, q, s, t, v, w, and x and the outputs are a through c, e through g, and i

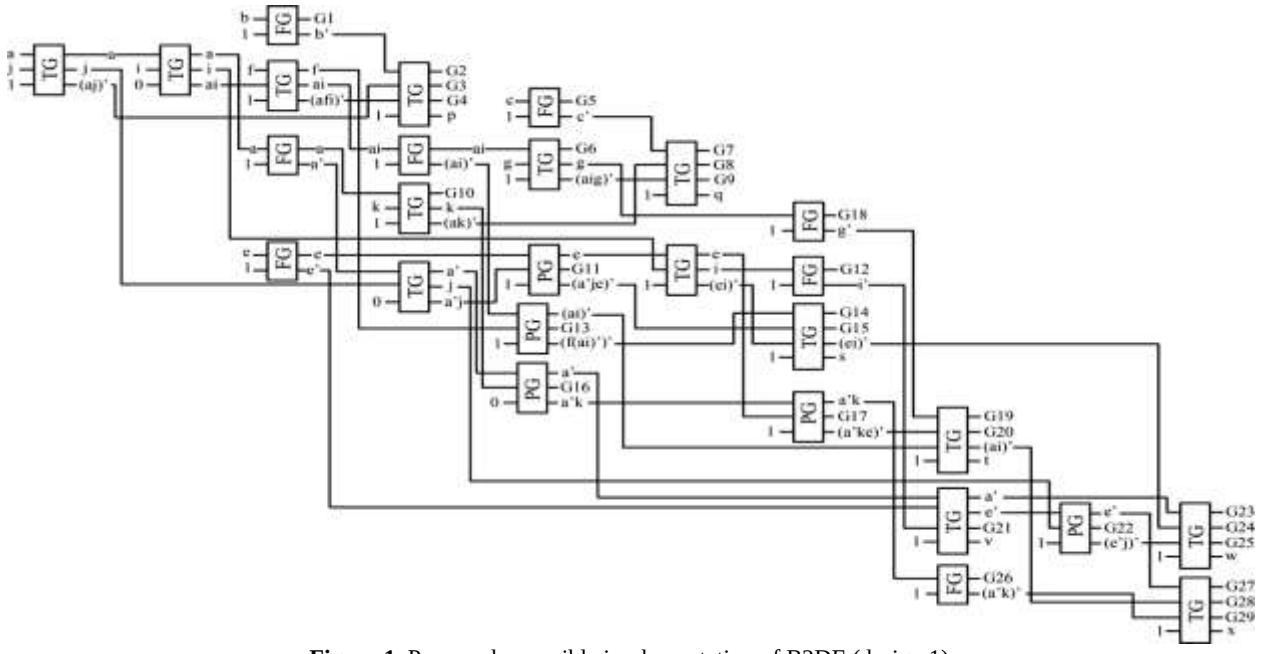

Figure 1. Proposed reversible implementation of B2DE (design 1)

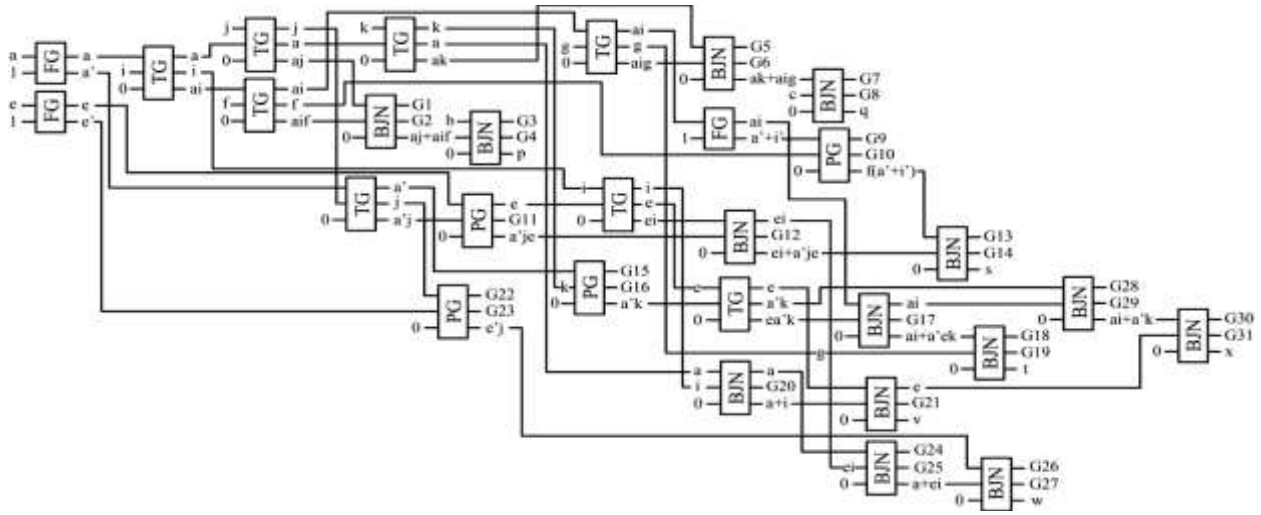

Figure 2. Proposed reversible implementation of B2DE (design 2)

through k, respectively, as shown in Figure 3. The inputs r, u, and y and the outputs d, h, and m not communicated in the circuit (Figure 3) since the inputs contributed directly to the circuit's outputs. The decoder circuit of design 1 integrated fourty-eight CIs to acquired the essential decoder functions, which results in fourty-six of GOs in the circuit's outputs. Design 2 of reversible D2BD realizes with the combinations of FG, TG, PG, and BJN gates. It necessitates a total of fifty reversible gates to achieve the essential function, as shown in Figure 4. The circuit makes use of fifty CIs and produced fourty-eight GOs in the circuit.

5. RESULTS, ANALYSIS AND, DISCUSSIONS

Table 2 shows the analysis results of the proposed designs of the DPD converters. The performance parameters, such as the gate count (GC), CI, GO, and QC, is summarized for each of the two proposed designs and are verified using the RCViewer+ tool [12]. The proposed designs compared with the existing design [7] found in the technical literature are shown in Table 2. The gate counts (GCs), CIs, and GOs of the proposed design 1 of B2DE are 27, 27, and 29, respectively, and

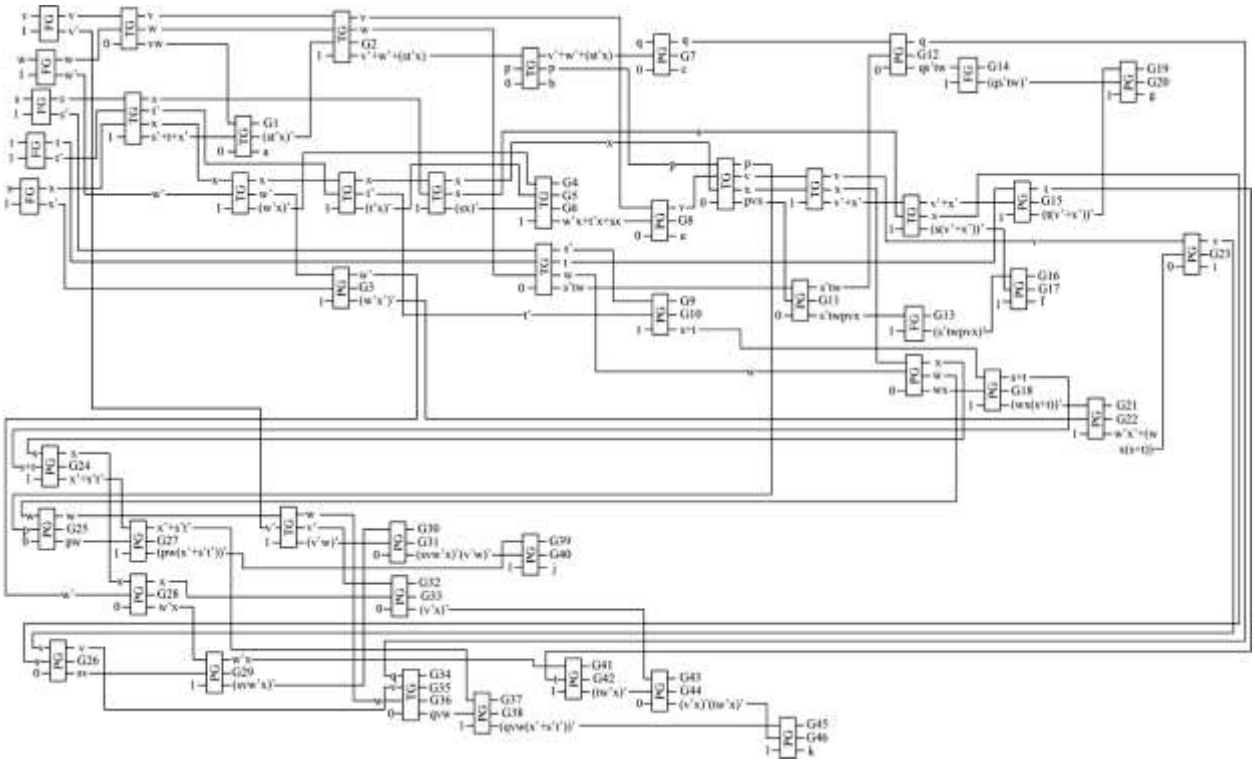

Figure 3. Proposed reversible implementation of D2BD (design 1)

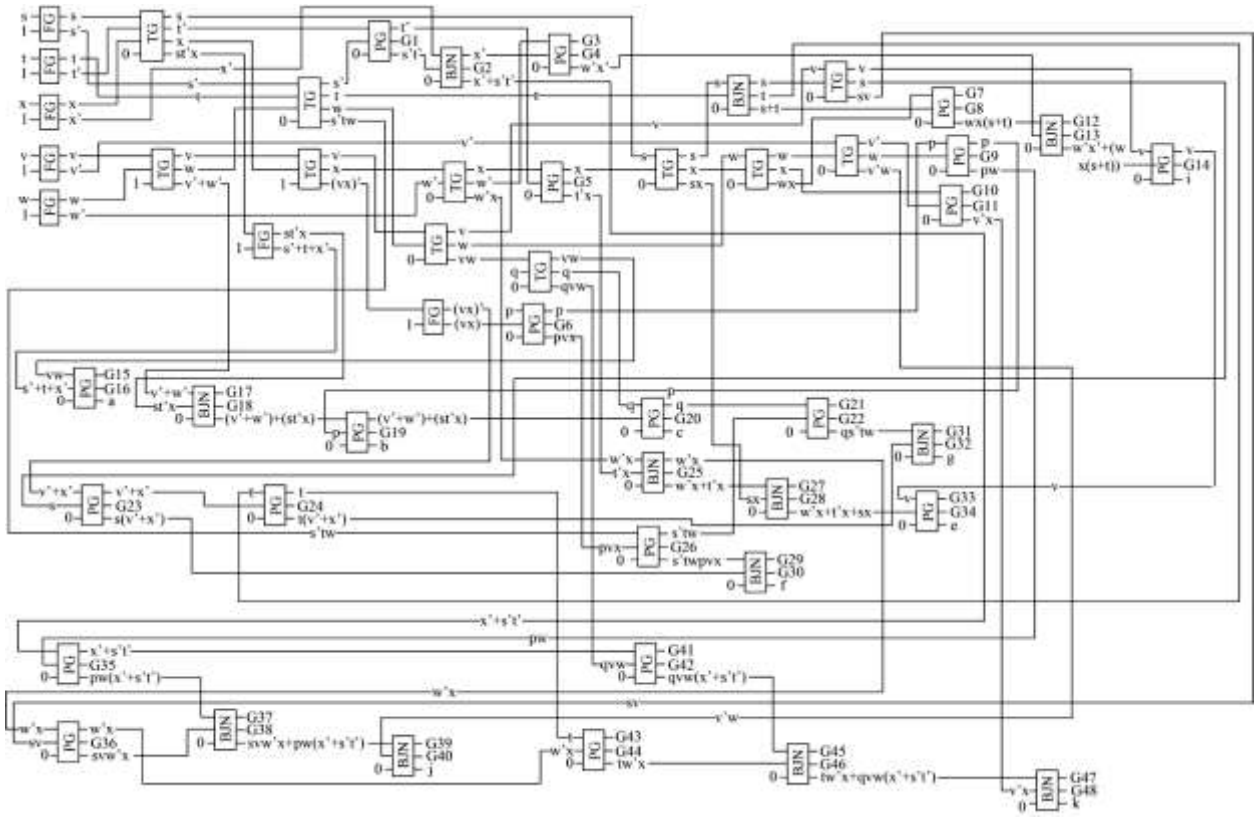

Figure 4. Proposed reversible implementation of D2BD (design 2)

that of the proposed design 2 of B2DE is 29, 29, and 31, respectively. The encoder's existing design by Kaivani et al. [7] engaged 22, 22, and 24 of GCs, CIs, and GOs, respectively. There is an increase of 5 units and 7 units in the proposed design 1 and design 2 of encoder compared with the encoder design of Kaivani et al. [7] in the three (GC, CI, and GO) parameters, as shown in Table 2. However, the proposed design 1 and design 2 of B2DE significantly reduce the QC by 23.11% and 35.17%, respectively.

The proposed design 1 of the D2BD has GCs, CIs, and GOs of 48, 48, and 46, respectively, and that of proposed design 2 of D2BD has 50, 50, and 48, respectively, as shown in Table 2. The existing approach by Kaivani et al. [7] possessed 43 GCs, 43 CIs, and 41 GOs. Similarly, as the encoder, the proposed design 1 and design 2 of D2BD utilize 5 units and 7 units more of GCs, CIs, and GOs, respectively, compared with the existing design [7]. The existing design [7] has a QC of 612, whereas the proposed design 1 of the decoder reduces the QC to 234 and further reduces to 218 by proposed design 2 of D2BD. The proposed design 1 and design 2 of D2BD impressively show improvements of 61.76% and 64.54%, respectively, when compared with the existing design [7] found in the literature.

Furthermore, the delay is calculated with the help of the RCViewer+ tool and noted, as shown in Table 2. All (four designs) the proposed designs and existing designs [7] are decomposed into primitive-quantum-gates (PQGs) and arranged into a compact form (parallel form), where the number of levels is evaluated. Each level comprises a primitive gate or several primitive gates in parallel, and each of them is realized to have a unit delay, denoted as Δ. The total number of levels represents the total delay of the circuit. As shown in Table 2, the delay (or the total number of levels) of the proposed B2DE of design 1 and design 2 is 99Δ and 25Δ, respectively, and the proposed D2BD of design 1 and design 2 is 93Δ and 48Δ, respectively. However, the delay of the existing encoder and decoder of Kaivani et al. [7] were 163Δ and 561Δ, respectively. Therefore, it is noted that the proposed designs show significant improvements in terms of delay compared to the existing design [7] found in the literature.

TABLE 2. Results of the proposed designs and comparison analysis with previous works

DESIGNS	GC	CI	GO	QC	DELAY
Encoder [7]	22	22	24	199	163Δ
Proposed B2DE: a) Design 1	27	27	29	154	99Δ
b) Design 2	29	29	31	129	25Δ
Decoder [7]	43	43	41	612	561Δ
Proposed D2BD: a) Design 1	48	48	46	234	93Δ
b) Design 2	50	50	48	218	48Δ

6. CONCLUSIONS

In this paper, two design approaches of reversible BCD to DPD converter and two reversible DPD to BCD converter are proposed. The proposed designs' analysis results show a significant reduction of QC than the existing design found in the literature with a considerable promotion of 5 units to 7 units in the other performance parameters. Also, since reversible computation has its one application in quantum computation, the designs which offer a low QC and high-speed circuit are the encouraging steps towards the complex reversible system computation.

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Persian Abstract

چکیده

در حال حاضر ، کاهش قدرت طراحی مدار یک موضوع اصلی تحقیق است. محاسبه برگشت پذیر معیارهای کاهش مصرف برق را در مقایسه با طراحی منطق سنتی برآورده می کند. بدین ترتیب ، محاسبات برگشت پذیر در دهه های اخیر بسیار مورد توجه قرار گرفته است. در این مقاله دو رویکرد طراحی برگشت پذیر مبدل دودویی کد گذاری شده ((BCDبه دهانه متراکم بسته بندی شده (DPD) (رمزگذار) و دو رویکرد طراحی مبدل DPD به) BCDرسیور) ارائه شده است. طراحی ها از طریق انتخاب مناسب دروازه ها و سازماندهی مناسب بیشتر چنین دروازه هایی با اجرای موازی انجام می شود. رویکردهای طراحی پیشنهادی ، اجرای کم هزینه کوانتومی را در مقایسه با طراحی پیشرفته ارائه می دهند. تجزیه و تحلیل نتایج هزینه رمزگذار برگشت پذیر DPD نشان می دهد کاهش قابل توجهی حداقل ۲۳% ~ و رمزگشای حداقل ۶۲% ~ نسبت به طراحی پیشرفته موجود در ادبیات. علاوه بر این ، ساختارها به دروازه های کوانتومی بدوی تجزیه می شوند و برای محاسبه تأخیر به صورت فشرده فشرده می شوند.