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Energy Efficient Novel Design of Static Random Access Memory Memory Cell in Quantum-dot Cellular Automata Approach

S. Kassa*, S. Nema

Electronics Engineering Department, SNDT Womens University, Mumbai, India

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A B S T R A C T

This paper introduces a peculiar approach of designing Static Random Access Memory (SRAM) memory cell in Quantum-dot Cellular Automata (QCA) technique. The proposed design consists of one 3-input MG, one 5-input MG in addition to a (2×1) Multiplexer block utilizing the loop-based approach. The simulation results reveals the excellence of the proposed design. The proposed SRAM cell achieves 16% and 15% improvement in terms of total number of Cell counts and Area. Similarly, the proposed design structure realizes the overall power dissipation savings up to 35.3% at maximum energy dissipation of circuit, 38.6% at average energy dissipation of circuit, 36.1% at minimum energy dissipation of circuit, 36.4% at average energy dissipation of circuit and 40.1% at average switching energy dissipation compared to the latest reported designs. The power analysis and structural analysis of the proposed design is compared with its state-of-the-art counterpart designs, using QCAPro and QCADesigner 2.0.3 tools. The proposed QCA based SRAM cell design can be taken as a base design in building an ultra-low power information generating systems like Microprocessors.

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1. INDTRODUCTION

Over the last few decades, CMOS technology has almost reached to its fundamental physical limits. The demands of high speed operation with low power consumption have compelled the scientists all over the world to investigate for new alternative technology. Many technologies such as Tunneling Phase Logic (TPL), Single Electron Tunneling (SET), Quantum-dot Cellular Automata (QCA) and Carbon Nano Tube Field Effect Transistor (CNT-FET) [1–4] are presented at nano-scale level for replacing CMOS technique. Among them, QCA is more fascinating because of its attractive features of high speed operation, extremely high density capacity, low power consumption and small dimension. Lent et al. proposed a physical implementation of an automaton using quantum-dot cells in 1994 [4] which quickly gained popularity among researchers worldwide and it was first fabricated in 1997 [5].

The QCA technology is still at its infancy stage; therefore many different options are available for its fabrication. Techniques like Semiconductor QCA, Metal-Island QCA, Magnetic QCA and Molecular QCA are available in literature but none of them has been proven as a leading one at this point. The basic idea of QCA cell in which bi-stable state is there, in which one state will interact with other state locally and with other neighboring cells as well for passing information. QCA cells are not required to be connected with each other physically [6–9].

1. 1. QCA Building Blocks A basic QCA cell consists of four quantum dots in a single cell, arranged in a square pattern. Two extra electrons are inserted, which always resides diagonally to each other inside a cell. By tunneling these electrons, mutual electrostatic repulsive force is created between them and as a result, one gets either logic 0 or logic 1. QCA Inverter and Majority gate

Corresponding Author's Email: rel1356@mnnit.ac.in* (S. Kassa)

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are the primary gates for building any QCA based logic circuits [6, 7]. Figure 1 shows the QCA cell, QCA inverter and QCA wire while Figure 2 shows the Original, Rotated and 5-input majority gate consequently.

At the moment, there is a growing demand for memory cell design which works as one of the bottom-line requirements for QCA devices [10–13]. In this article, loop-based approach have been taken for designing well-optimized SRAM cell compared to traditional CMOS based SRAM memory cell, which is a pioneering approach.

Two main approaches are by and large available for designing QCA circuits: loop-based and line-based. In loop-based approach, all the clock zones are correlated to hold data in a loop of QCA cells while in line-based approach, a line of QCA cells is utilized for saving earlier values of the data. In the proposed design here, loop-based approach has been utilized for its simplicity and robustness in designing circuit.

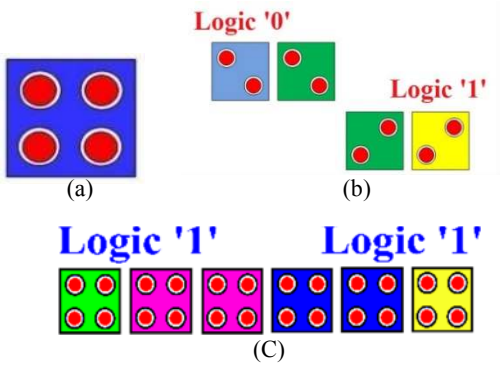


Figure 1. QCA (a) Cell (b) Inverter (c) Wire

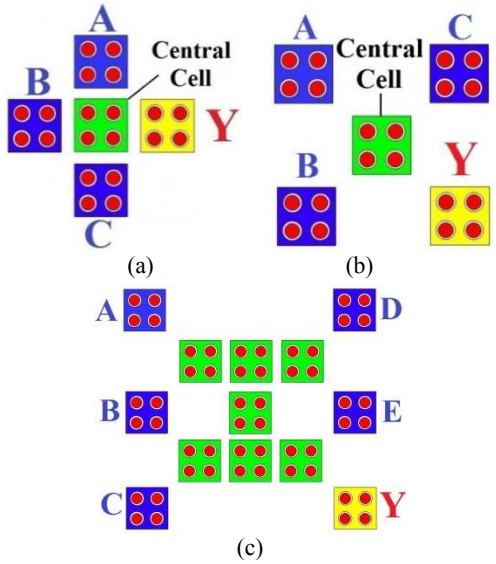


Figure 2. QCA based (a) Original (b) Rotated (c) 5-input Majority Gate

2. PROPOSED QCA SRAM CELL DESIGN

Discussion about the robust and efficient structure of QCA SRAM cell has been preceded in this section. Figures 3 and 4 show the SRAM cell designs from previous papers. Figures 5a, 5b and 5c show logical diagram, layout and simulation result for the proposed QCA SRAM cell accordingly.

3. OPERATION OF PROPOSED SRAM CELL

The proposed design configuration join one 3-input MG (MG-3) and one 5-input MG (MG-5) in addition to one (2×1) Multiplexer block as shown in Figure 5a. While the Enable signal is set to logic 1, the write operation can also be accomplished by setting W/R signal to logic 1. Along this line, the 3-input MG produces logic 1 since most of the inputs are at logic 1. Most of the time, one gets odd number of inputs, so they don't have to deal with the question of what happens when exactly half the inputs are logic 0. During the write operation, the input data (Input),

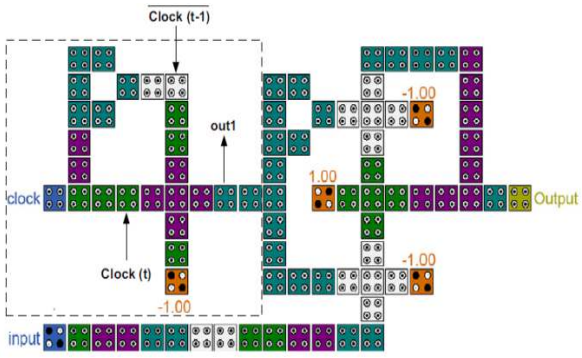


Figure 3. SRAM cell design as reported in [14]

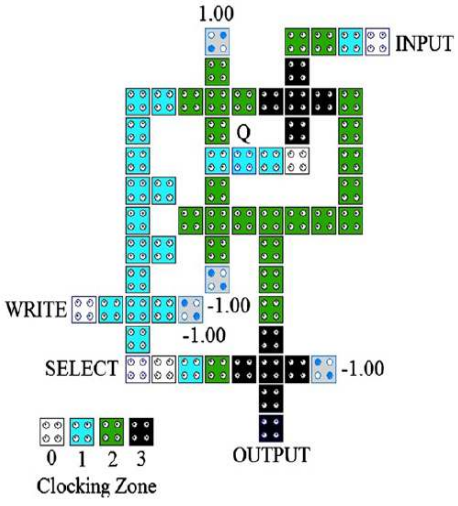


Figure 4. SRAM cell design as reported in [15]

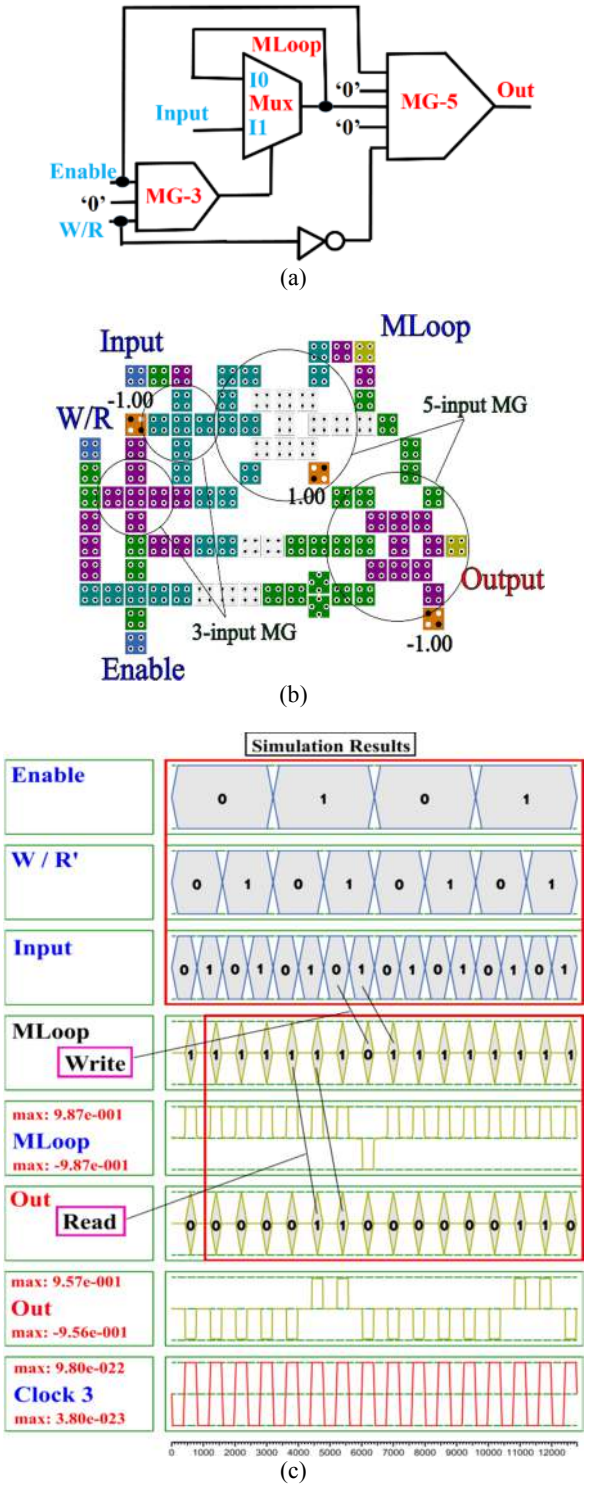


Figure 5. QCA SRAM cell (a) logical diagram (b) layout (c) simulation result

which is fed to the second input of the (2×1) Multiplexer (I1), will be written to the memory loop (MLoop) and also transmitted to the 5-input MG together with the Enable signal, two static logic 0 inputs and the inverted W/R signal (logic 0). The MG-5 with three static logic 0 inputs gives outputs as logic 0.

It is worthy to take note of that, there is not any tri-state support idea in QCA innovation available, which totally eliminates the particular information in a circuit. Typically, logic 0 has been considered as the output of memory cell in write mode when output circuit is deactivated.

The complete operation of the proposed SRAM cell is given in Table 1. When Enable input is '0', the output will hold the previous output as it is for whatever input it would be. When Write operation is enabled, W/R should be '1' and if Input is '1', so '1' will be written in MLoop and if Input is '0', so '0' will be written in MLoop. Like that, when Read operation is enabled, W/R should be '0'. Now, based on the signal in MLoop, Output will read the particular signal '0'/'1' at an Output.

4. RESULT ANALYSIS

Comparison of proposed SRAM cell design with previous designs is given in Table 2 for different parameters. Structural analysis of the proposed cell is verified utilizing QCADesigner 2.0.3 tool [16]. Table 3 shows the comparison of different types of power dissipation for the proposed and reported designs obtaining the results from QCAPro tool [17].

Figure 6 shows the power dissipation analysis of the proposed SRAM cell design with previous designs at different kink energies (Ek). The results show the dominance of the proposed design on the former reported designs.

TABEL 1. Complete operation of proposed QCA SRAM Memory Cell

Operation	Enable	Input	W/R	MLoop	Output
Write	1	1	1	1	0
	1	0	1	0	0
Read	1	×	0	0	0
	1	×	0	1	1
Hold	0	×	×	Hold	0

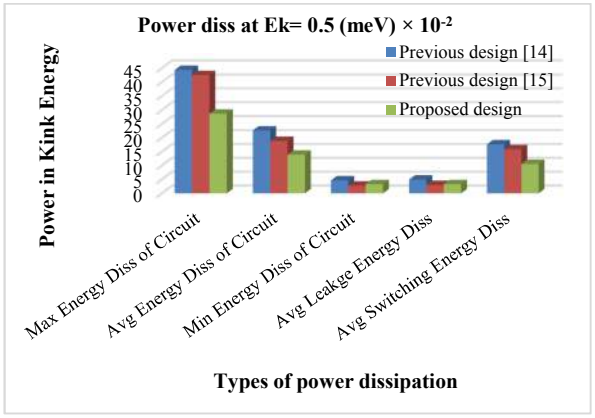
TABLE 2. Comparison of the proposed QCA SRAM Circuit

QCA SRAM cells	Type of wire crossing	Cell Count	Area (μm²)	Cycles	Output (via W/R and Enable signals)
Proposed	Logical	92	0.10	1.5	YES
Previous design [14]	Coplanar	100	0.12	2	NO
Previous design [15]	Coplanar	109	0.13	2	NO

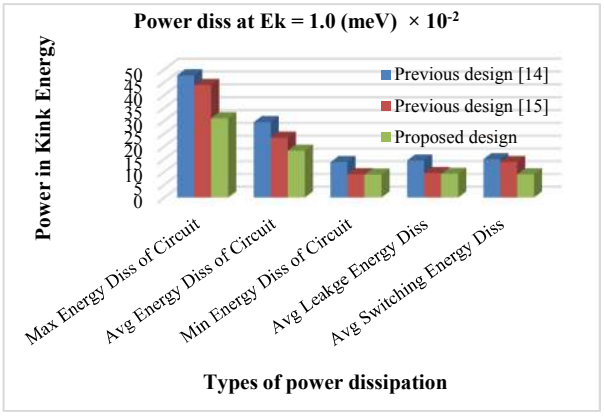
TABLE 3. SRAM Power dissipation analysis

	Ek=0.5 (meV) × 10^{-2}			Ek=1 (meV) × 10^{-2}			Ek=1.5 (meV) × 10^{-2}		
	Previous design [14]	**Previous design** [15]	**Proposed design**	**Previous design** [14]	**Previous design** [15]	**Proposed design**	**Previous design** [14]	**Previous design** [15]	**Proposed design**
Max Energy Diss of Circuit	44.41	42.55	28.69	47.69	43.93	30.97	53.25	46.82	34.42
Avg Energy Diss of Circuit	22.68	18.89	13.92	29.46	23.38	18.31	37.85	29.19	23.63
Min Energy Diss of Circuit	4.69	2.77	3.33	13.83	9.12	8.97	24.45	16.88	15.62
Avg Leakage Energy Diss	4.98	3.01	3.33	14.46	9.55	9.26	25.26	17.4	15.92
Avg Switching Energy Diss	17.69	15.89	10.59	14.99	13.83	9.05	12.59	11.79	7.71

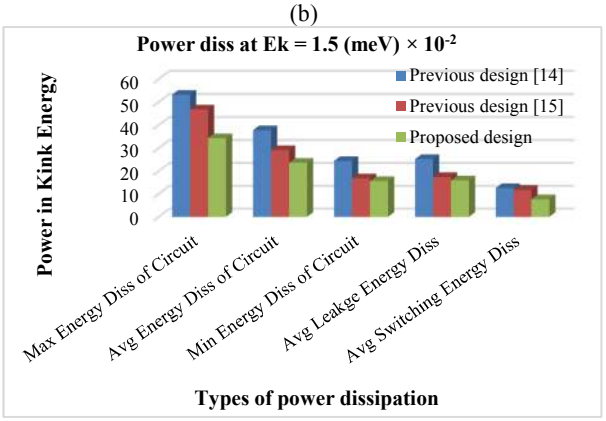
4. 1. Sram Power Dissipation Analysis Figure 7 shows the power dissipation analysis for the proposed SRAM cell. The red color cell shows the lowest level of energy dissipation by a particular cell while the black color spot shows the highest level of energy dissipation by the cell. From the figure, one can analyze that, at a Majority gate, there are some black spot cells available, as well as many less number of cells are there which dissipate power in black color. This shows the superiority of the proposed SRAM cell design compared to the previous designs in terms of power dissipation.



(a)



(b)



(c)

Figure 6. Power dissipation analysis at different kink energies (a) Ek = 0.5 × 10^{-2} (meV) (b) Ek = 1.0 × 10^{-2} (meV) and (c) Ek = 1.5 × 10^{-2} (meV)

Analysis of polarization for different input combinations is an interesting area to take care for a particular QCA based design because the proposed design must give the correct polarization for each of the input combinations.

Figure 8 shows the polarization design for the proposed SRAM cell. The Blue color cell depicts logic '1' while black color cell depicts logic '0'. Figure 8 shows the output polarization result for (1,1,1,1) input combination. From the figure, one can easily analyze that the proposed SRAM cell gives the correct polarization for a particular input combination. The same can be realized for other input combinations also.

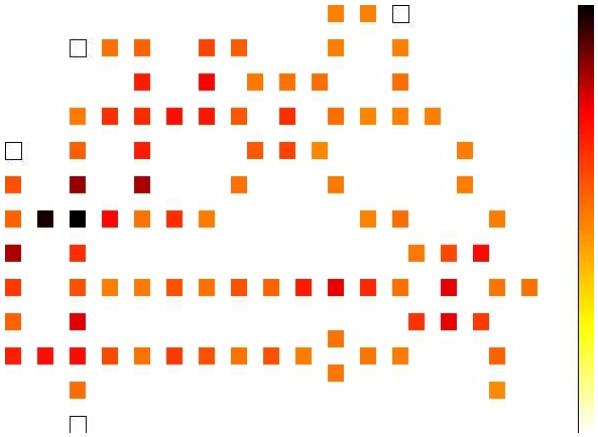


Figure 7. Power dissipation analysis of proposed SRAM Cell

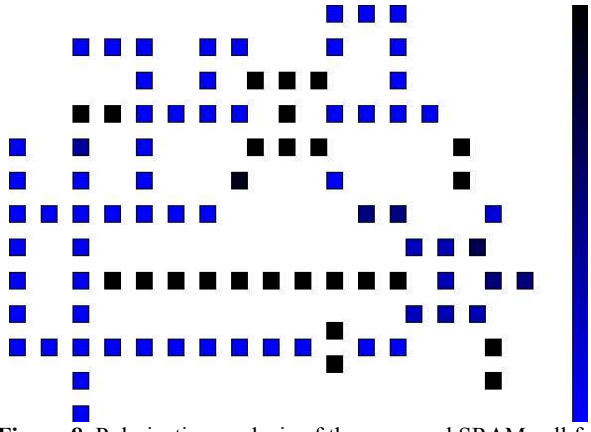


Figure 8. Polarization analysis of the proposed SRAM cell for (1,1,1,1) input

5. CONCLUSION

The proposed SRAM memory cell is designed by utilizing an open loop-based approach. It gives a proficient and robust end result SRAM memory cell structure as far as area, delay, cell counts and power consumption is compared with the reported designs. The proposed design structure saves the overall power up to 35.3% at maximum energy dissipation of circuit, 38.6% at average energy dissipation of circuit, 36.1% at minimum energy dissipation of circuit, 36.4% at average energy dissipation of circuit and 40.1% at average switching energy dissipation compared to the latest reported designs. Polarization analysis also supports the accuracy of the proposed SRAM cell design for different combination of inputs. The proposed design is energy efficient which can be considered as a base design for planning large systems similar to Microprocessors.

6. ACKNOWLEDGEMENT

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چکیده

این مقاله روشی خاص را برای طراحی سلول حافظه SRAM در روش کوانتوم دات (Quantum-dot Cellular Automata) معرفی می‌کند. طرح پیشنهادی شامل یک MG با ۳ ورودی، یک MG با ۵ ورودی به علاوه یک بلوک مالتی پلکسر (۲ × ۱) با استفاده از رویکرد مبتنی بر حلقه است. نتایج شبیه‌سازی بیانگر برتر بودن طراحی پیشنهادی است. سلول پیشنهادی SRAM به میزان ۱۶ و ۱۵ درصد از نظر تعداد کل شماره سلول‌ها و مساحت بهبود یافته است. به طور مشابه، ساختار طراحی پیشنهادی، صرفه‌جویی در مصرف توان را به میزان ۳۵/۳٪ در حداکثر اتلاف انرژی مدار، ۳۸/۶٪ در اتلاف انرژی متوسط مدار، ۳۶/۱٪ در حداقل اتلاف انرژی مدار، ۳۶/۴٪ در تخلیه انرژی متوسط مدار و ۴۰/۱٪ از میانگین تلفات انرژی سوئیچینگ در مقایسه با آخرین طرح‌های گزارش‌شده محقق کرده است. تجزیه و تحلیل توان و ساختاری طراحی پیشنهادی با طرح‌های همتای آن تاکنون، با استفاده از ابزار QCAPro و QCADesigner 2.0.3 مقایسه شده است. طرح سلولی SRAM مبتنی بر QCA می‌تواند به عنوان یک طراحی پایه در ساخت یک سیستم تولیدکننده اطلاعات فوق‌العاده کم توان مانند ریزپردازنده ها مورد استفاده قرار گیرد.

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