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A Modified Noise Analysis of a Common Source − Common Gate Low Noise Transconductance Amplifier for Sub-micron Technologies

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ABSTRACT

This paper is based on analysis of a common source - common gate low noise transconductance amplifier (CS-CG LNTA). Conventional noise analyses equations are modified by considering to the low output impedance of the sub-micron transistors and also, parasitic gate-source capacitance. The calculated equations are more accurate than calculated equations in other works. Also, analyses show that the noise of the tail transistor, which is utilized to bias the common gate transistor, will limit noise canceling advantages. So, the common gate transistor is biased by a resistor. That leads to a significant improvement in noise figure. By utilizing a Taylor series expression, a closed-form equation is obtained to calculate IIA3 for the first time. Finally, based on the calculated equation a design procedure is proposed.

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NOMENCLATURE

R_{ocs}	Output resistance of the CS stage	C_{gscs}	parasitic gate-source capacitor of the CS transistor
R_{ocg}	Output resistance of the CG stage	α	Voltage divider factor between C_{bcs} & C_{gscs}
R_{mixer}	Input resistance of the mixer	C_{bcs}	coupling capacitor
R_{cs}	Equvalent gain of mixer & TIA in CS path	r_{ob}	Output resistanc of the tail transistor
R_{cg}	Equivalent gain of mixer & TIA in CG path	R_s	Antenna resistance
g_{mcg}	Transconductance of the CG stage	F	Noise factor
g_{mcs}	Transconductance of the CS stage		

1. INTRODUCTION

Commercial advantages of multi-standard devices play a crucial role in the growth of the modern receivers in recent years. Multi-standard receivers must be high linear, low noise figure (NF), and low power consumption to obtain the best performance [1]. The current-mode receiver is more linear than the voltage mode counterpart, mainly due to having lower voltage gain and one-time use of the nonlinear voltage to current conversion. Another important feature of the multi-standard receivers is the ability to work in several frequency bands. Surface Acoustic Wave (SAW) filters, which pass signals only on a special frequency band, are not utilized in highly integrated multi-standard applications [2-6].

Some problems such as gain compression, intermodulation, harmonic mixing, and noise folding can occur without SAW band-pass filter. Therefore, the SAW-less receivers should have a low voltage gain while have appropriate NF [7]. Most designs of SAW-less receivers employ the impedance translation feature of the current driven passive mixer (CDPM). Mixer-first receiver is one of the commonly used architectures utilized for the implementation of SAW-less receivers [2, 3, 8]. In this structure, low noise amplifier (LNA) is removed, and a down- conversion passive mixer is placed at the first stage of the receiver. Although this

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approach results in a linear receiver, NF increases due to the absence of the LNA [2]. Utilizing a low noise transconductance amplifier (LNTA) is another structure for a SAW-less receiver to drive CDPM and reduce the noise effect of the next blocks including the mixer and Trans-Impedance amplifier (TIA). This approach improves NF in comparison with mixer-first topology while degrades the overall linearity of the receiver [4].

Although there is usually a trade-off between NF and linearity, there are noise and nonlinearity cancellation techniques that improve both parameters, concurrently. In these approaches, noise and nonlinearity of the main path are approximately canceled out by an auxiliary path [9]. CS-CG LNA is one of the popular structure which utilizes this technique. In the structure, the noise of the main path (CG path) is canceled out by auxiliary path (CS path).

The reduction of the output resistor in transistors, which is cuased by the ongoing scaling of semiconductor technologies, introduces new challenges for the design of a current-mode analog circuit.

In this work, the effect of the low output resistor of the transistors on linearity and NF are investigated for a CS- CG LNTA. We have obtained the closed form equations to compute the noise factor and IIP3. The noise factor of the CS-CG LNA is obtained but the noise of the tail transistor and also the output impedance of the transistors is ignored [10]. In this work, the effect of the low output resistor of the transistors on linearity and NF are investigated for the CS-CG LNTA. Besides, we present a closed-form equation to calculate the IIP3 for the CS-CG LNTA for the first time that also can be utilized for CS-CG LNA.

The rest of the paper is as follows. NF of The conventional CS-CG LNTA with two kinds of biasing methods are studied in section II and section III. The linearity of the CS-CG LNTA is calculated in section IV. In section V, the design procedure is proposed.

2. NOISE ANALYSIS OF A CURRENT SOURCE BIASING CS-CG LNTA

The main idea of the noise canceling is introduced in Figure 1. There are two paths to cancel out the noise of the matching resistor. In one path, the matching resistor current is measured and is amplified by β, and in another path. The voltage of the matching resistor is measured and is gained by δ. In an ideal situation, there is a ratio of β/δ that the noise of the matching resistor can be completely canceled out at differential output. Figure 2 shows a current mode implementation of a noise canceling receiver. In the Figure, $g_{m,main}$ and $g_{m,aux}$ are transconductance of the CG and CS transistor, respectively. In current mode topology, noise/nonlinearity of the main path transistors is usually canceled out by recombining signals of two paths. A simplified circuit of this technique in current mode is shown in Figure 3.

The common gate configuration, implemented by M_{cg}, is utilized as an active matching circuit while that also measures the current in the input resistance as well. M_{cs} has a common source structure to amplify the voltage of the active input resistance (input seen impedance from the gate of the M_{cg}). To simplification, mixer and TIA are modeled as a trans-impedance amplifier.

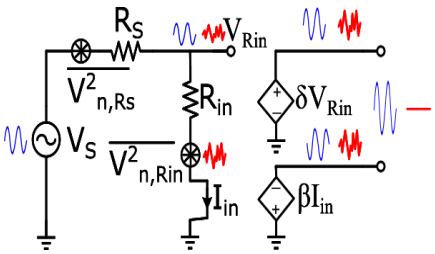

Figure 1. Conceptual circuit of the noise canceling method

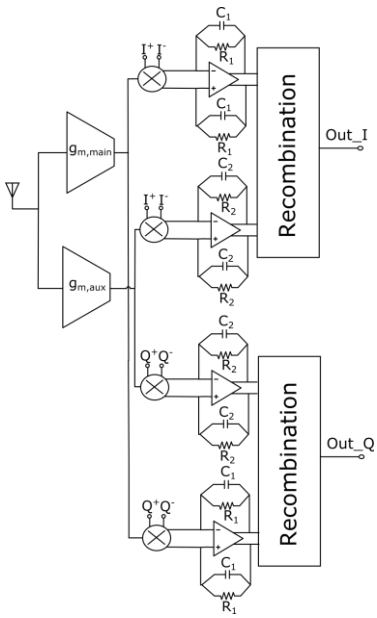

Figure 2. Current-mode noise/nonlinearity cancellation receiver

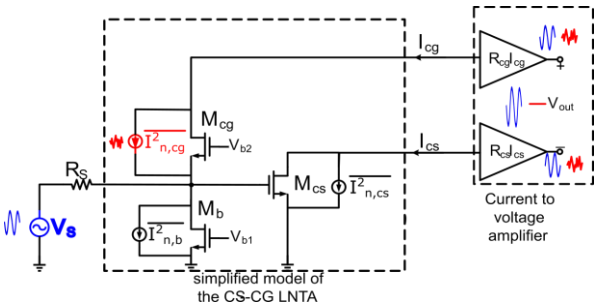

Figure 3. Simplified model of the CS-CG LNTA + baseband

In this figure, $\overline{I_{n,cg}^2}$, $\overline{I_{n,cs}^2}$ and $\overline{I_{n,b}^2}$ are noise of the M_{cg}, M_{cs} and M_b, respectively. The differential output noise is computed as follows:

$$\begin{aligned}\overline{V_{n,out}^2} &= \left[\left(1-\frac{g_{mcg}R_S}{2}\right)\frac{R_{ocg}}{R_{ocg}+R_{mixer}}R_{cg}\right. \\ &\left.-\frac{\alpha g_{mcs}R_S}{2}\frac{R_{ocs}}{R_{ocs}+R_{mixer}}R_{cs}\right]^2\overline{I_{n,cg}^2} \\ &+\left[\frac{g_{mcg}R_S}{2}\frac{R_{ocg}}{R_{ocg}+R_{mixer}}R_{cg}\right. \\ &\left.-\frac{\alpha g_{mcs}R_S}{2}\frac{R_{ocs}}{R_{ocs}+R_{mixer}}R_{cs}\right]^2\left(\overline{I_{n,b}^2}+\overline{I_{n,R_s}^2}\right) \\ &+\left[\frac{R_{ocs}}{R_{ocs}+R_{mixer}}R_{cs}\right]^2\overline{I_{n,cs}^2}\end{aligned} \quad (1)$$

where $\overline{I_{n,R_s}^2}$ represents the noise of the antenna resistor (R_s) g_{mcs}, and g_{mcg} are trans-conductance of the CS transistor and the CG transistor, respectively. R_{ocg} and R_{ocs} demonstrate the output impedance of the CG and CS stage, respectively. R_{mixer} is input impedance of the Mixer. The channel Noise of the M_1 and M_2 have a negligible impact on the total noise factor. So, the effect of them is ignored on the noise factor calculations. α is voltage divider factor between coupling capacitor (C_{bcs}) and parasitic gate-source capacitor of the CS transistor (C_{gscs}) that is obtained from Equation (2).

$$\alpha=\frac{C_{bcs}}{C_{bcs}+C_{gscs}} \quad (2)$$

The ratio of the baseband gain of the main path per baseband gain of the auxiliary path should be set as Equation (3) to cancel out the noise of the CG transistor.

$$\frac{R_{cg}}{R_{cs}}=\frac{\alpha g_{mcs}R_s\frac{R_{ocs}}{R_{ocs}+R_{mixer}}}{\left(2-g_{mcg}R_s\right)\frac{R_{ocg}}{R_{ocg}+R_{mixer}}}=\frac{\alpha\alpha_{cs}g_{mcs}R_s}{\left(2-g_{mcg}R_s\right)\alpha_{cg}} \quad (3)$$

Suppose that output impedance of the bias transistor is r_{ob}. Thus, g_{mcg} should be chosen $R_s^{-1}—2r_{ob}^{-1}$ to satisfy matching condition. Therefore, we can calculate noise factor as:

$$\begin{aligned}F&=1+\gamma g_{mb}R_s+\frac{\gamma\left(2-g_{mcg}R_s\right)^2}{\alpha^2 g_{mcs}R_s} \\ &=1+\gamma\left(1-\frac{2R_s}{r_{ob}}\right)+\frac{\gamma\left(1+\frac{2R_s}{r_{ob}}\right)^2}{\alpha^2 g_{mcs}R_s}\end{aligned} \quad (4)$$

According to (4), the low output impedance of the bias transistor increases the noise factor. In the derived expression, noise factor of the conventional noise/nonlinearity ca ncellation can be decreased by increasing g_{mcs} but the minimum achievable noise factor of this structure is limited to $1+\gamma$. The second term of (4) is caused by the M_b. Noise of the tail transistor, low output impedance of the transistors and also voltage divider factor (α) is ignored in [11] while these can have a significant effect on the total noise factor. In [12], without considering to the noise of the load resistance of the LNA, the noise factor after simplification is obtained as:

$$F=1+\frac{\gamma}{g_{mcs}R_s} \quad (5)$$

Please notice that the computed noise factor in literature [13] is for an LNA. We ignore the noise of the load resistances in Equation (5) to have a fair comparison. Simulated noise contribution of the transistors in current-biasing CS-CG LNTA (Figure 4) is introduced in Figure 5. All of the simulations are done in cadence. The noise of CS transistors (M_{ncs} and M_{pcs}) goes down by increasing g_{mcs} while the noise of the other elements is constant approximately. The noise of M_1, M_2, M_{pcg}, and M_{ncg} are negligible. For a high value of g_{mcs}, the noise of tail, transistors play a major role in the overall noise factor. Figure 6 shows the NF of the current-biasing CS-CG LNTA versus g_{mcs} for various α. By increasing g_{mcs}, the NF is improved but it is limited because of the noise of the current biasing transistor (M_b). An inductor can be utilized instead of M_b to provide bias path for M_{cg}. However, this topology occupies a large area. Therefore, a resistor can be utilized to bias the CG transistor instead of the use of an inductor for very large scale integrated receivers.

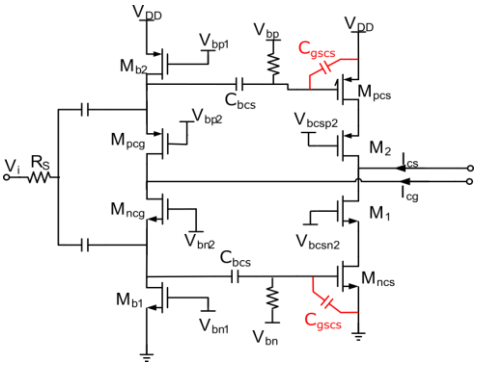

Figure 4. Conventional CS-CG LNTA by current biasing

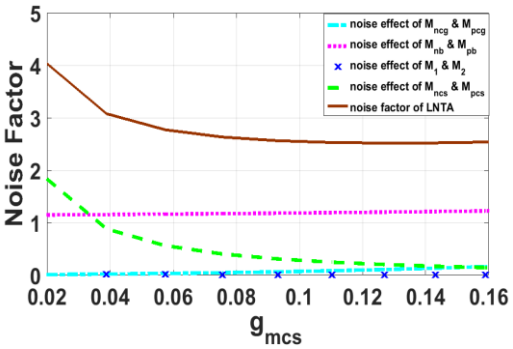

Figure 5. Noise contribution of transistors in current-biasing CS-CG LNTA versus gmcs (α=0.9)

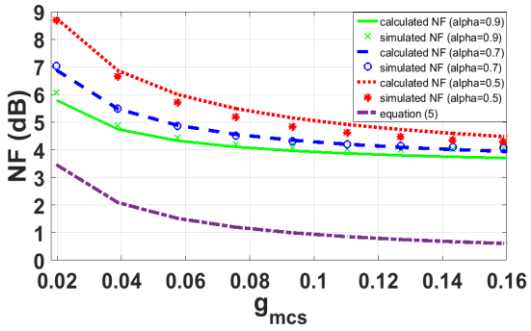

Figure 6. NF of current-biasing CS-CG LNTA versus gmcs for various α

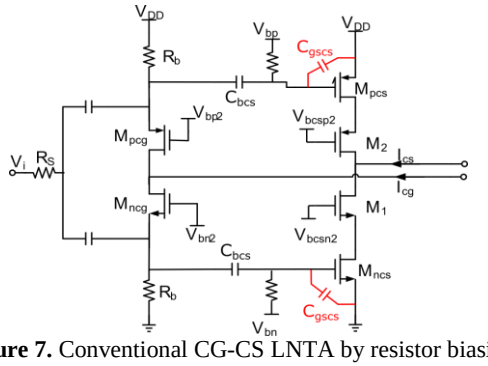

Figure 7. Conventional CG-CS LNTA by resistor biasing

3. NOISE ANALYSES OF A RESISTOR-BIASING CS-CG LNTA

A complementary structure for RF transconductance stages is usually utilized to save area and power consumption. A wide CG transistor or a low bias resistor can be used to satisfy matching condition. The first degrades the maximum operating frequency and mistunes the noise canceling of the CG transistors because of parasitic capacitances. The second increases power consumption in comparison with the first way and also increases noise factor because a lower g_{mcg} will be needed for CG transistor to match the input impedance of the LNTA. On the other hand, the input impedance of the LNTA is $g_{mcgp} + g_{mcgn} + (2/R_b)$. So, by decreasing R_b, the value of the overall $g_{mcg}(g_{mcgp} + g_{mcgn})$ should be reduced to satisfy the exact matching condition. The noise factor of this structure can be calculated by Equation (6).

$$F = 1 + \frac{2R_s}{R_b} + \frac{\gamma\left(2 - g_{mcg}R_s\right)^2}{\alpha^2 g_{mcs}R_s} = 1 + \frac{2R_s}{R_b} + \frac{\gamma\left(1 + \frac{2R_s}{R_b}\right)^2}{\alpha^2 g_{mcs}R_s} \quad (6)$$

The low value of the R_b increases noise factor directly (second term of Equation (6)) and indirectly (third term of (6)). The second term of Equation (6) goes up by reducing R_b. Low value of the R_b leads the $g_{mcg}R_s$ to lower value than one. So, the third term of Equation (6) is increased by lower R_b too. However, the LNTA by a CG transistor which is biased by a resistor (Figure 7) has a lower noise figure than the LNTA by a current–biasing CG transistor.

Figure 8 presents the noise contribution of the elements in Figure 7. Unlike the current-biasing CS-CG LNTA, CS transistors play a major role in total noise factor. Noise contribution of the CS transistors goes down by increasing g_{mcs}. Figure 9 shows NF of resistor-biasing CS-CG LNTA for various α. Same as the current-biasing CS-CG LNTA, the NF of the resistor-biasing CS-CG LNTA goes up by decreasing α.

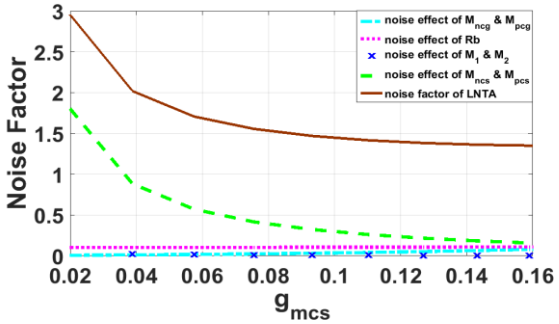

Figure 8. Noise contribution of transistors in resistor-biasing CS-CG LNTA versus g_{mcs} (α=0.9)

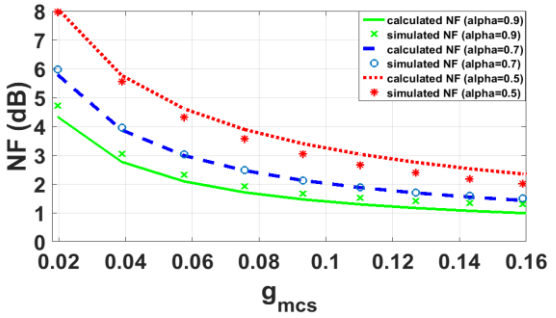

Figure 9. NF of resistor-biasing CS-CG LNTA versus g_{mcs} for various α

4. LINEARITY ANALYSIS

A Taylor series expression is utilized to calculate the lin- earity of the LNTA (see Appendix). By considering to low voltage gain for the LNTA, nonlinear transconductance (g_m) of the transistors plays a major role in overall nonlinearity. The output voltage of the noise/nonlinearity cancellation receiver (Figure 3) can be illustrated as follows:

$$V_{out} = H_1 V_s + H_2 V_s^2 + H_3 V_s^3 \quad (7)$$

where H_1, H_2, and H_3 represent first-order, second-order, and third-order Taylor series coefficients of the output voltage after combination of the main and auxiliary path. V_s is the input RF signal. H_1 and H_3 can be calculated by Equations (8) and (9), respectively.

$$H_1 = \frac{1}{2} g_{mcg} \alpha_{cg} R_{cg} + \frac{1}{2} \alpha g_{mcs} \alpha_{cs} R_{cs} \tag{8}$$

$$\begin{aligned} H_3 = & -\alpha_{cg} R_{cg} \left(2 - g_{mcg} R_s\right) \left(\frac{R_S g_{mcg}^{'}}{16} + \frac{g_{mcg}^{''}}{16} \right) \\ & -\alpha \alpha_{cs} R_{cs} [\frac{\alpha^2 g_{mcs}^{''}}{16} - \frac{g_{mcs} R_S g_{mcg}^{''}}{16} - \frac{g_{mcs} R_S^2 g_{mcg}^{,2}}{16} \\ & + \frac{2\alpha R_S g_{mcs}^{'} g_{mcg}^{'}}{16}] \end{aligned} \tag{9}$$

Using Equation (3), receiver gain ($H1$) and IIA3 can be calculated by Equations (10) and (11), respectively.

$$H_1 = \frac{\alpha_{cg} R_{cg}}{R_S} \tag{10}$$

$$\begin{aligned} IIA3^{-2} = & -\frac{3\alpha}{32 g_{mcs} R_S} \left(1 + \frac{2R_s}{R_b}\right) \\ & \times \left(\alpha g_{mcs}^{''} + R_S g_{mcg}^{'} g_{mcs}^{'}\right) \end{aligned} \tag{11}$$

Regarding utilize a complementary structure for CS and CG transconductance stage; the second order nonlinearity has a very low value in comparison with the third-order nonlinearity. So, the second term of the nonlinearity can be ignored for the designed transconductore stage. Also, decreasing α can help to improve linearity, but it goes up the NF. IIP3 of the current- biasing and resistor-biasing LNTA versus g_{mcs} for various α is plotted in Figures 10 and 11, respectively.

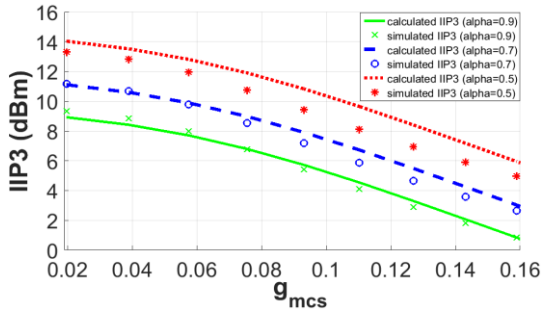

Figure 10. IIP3 of current-biasing CS-CG LNTA versus g_{mcs} for various α

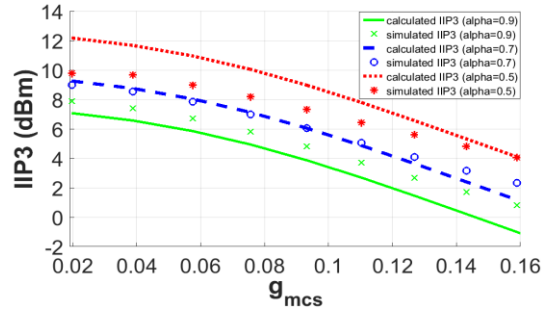

Figure 11. IIP3 of resistor-biasing CS-CG LNTA versus g_{mcs} for various α

5. DESIGN PROCEDURE OF THE CS-CG LNTA

To design of a CS-CG LNTA, a 20 mS transconductance stage (we call it to reference transconductance stage) should be designed at first. Then, some parameters of the gm transconductor including the output resistance (R_{or}), gate-source capacitance of the M_{ncs} and M_{pcs} (C_{gsr}), and output resistance of the M_{ncs} or M_{pcs} (r_{ob}) should be calculated by simulation. The width of the transistors can be set N times of the width of the transistors of the reference transconductance stage to achieve the desired gm stage ($N \times 20mS$) for CS stage. Moreover, the first-order and second-order non- linearity can be plotted versus g_m (Figure 12). The plotted curves can write as a function of g_m. Next, using Equation (6) (or Equation (4) for current-biasing version) and Equation (11), we can plot the NF and IIP3 by varying g_{mcs} and α same as Figures 13 and 14.

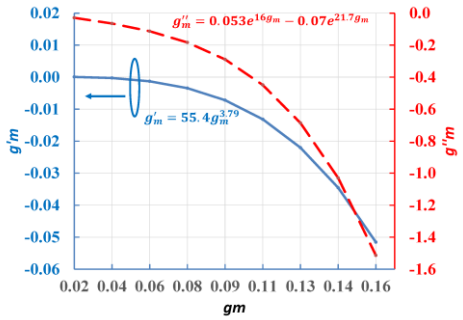

Figure 12. First-order and second-order transconductance nonlinearity of the CS stage versus g_{mcs}

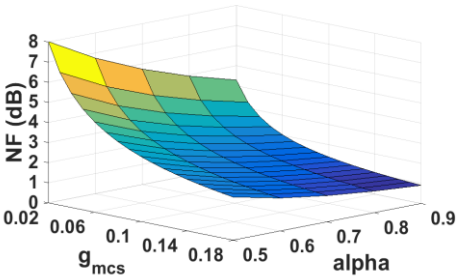

Figure 13. Estimated NF of resistor-biasing CS-CG LNTA versus g_{mcs} and α

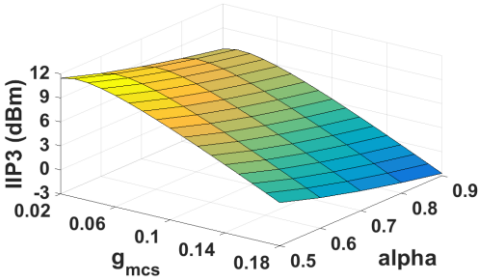

Figure 14. Estimated IIP3 of resistor-biasing CS-CG LNTA versus gmcs and α

After choosing the g_{mcs} and α from these figures to have the desired NF and IIP3, we can obtain other values for the elements that is utilized in the receiver.

C_{gs} of the designed CS stage is $N \times C_{gsr}$ while the R_{ocs} is R_{or}/N. By these values and a reasonable value for $R_{mixer,}$ we can calculate $\alpha_{cg \text{ and }} \alpha_{cs}$. Besides, C_{bcs} can be calculated by Equation (2). For the desired value for a voltage gain of the receiver, R_{cg} can be computed from Equation (10). R_{cg} demonstrates the equivalent gain of the mixer and the TIA in the main path. So, the R_1 (feedback resistor of the TIA in the main path (Figure 2)) is calculated as:

$$R_1 = \frac{\pi}{2} R_{cg} \tag{12}$$

Also, R_{cs} can be computed by Equation (3). So, the R_2 is $\frac{\pi}{2} R_{cs}$.

6. CONCLUSION

The low output impedance of the transistors in CS-CG LNTA is considered and new situation to cancel out the noise of the CG transistor is obtained. Analyses show that the noise of the current source transistor limits the NF in current-biasing CS-CG LNTA. So, it is better to use a resistor instead of the current source transistor to bias the CG transistor. Using the small biasing resistor increase the NF while high biasing resistor limits the operational frequency. For the first time, a closed-form equation is obtained to calculate the IIP3 of the CS-CG LNTA. Totally a design procedure to design the CS-CG LNTA is illustrated.

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8. APPENDIX: TAYLOR SERIES ANALYSIS

Tylor expansion of the I_{cs} and I_{cg} and V_i are defined in (A.1)-(A.3), respectively. I_{cs} and I_{cg} are output current of the CS and CG transconductance stage. V_i is the input voltage of the LNTA.

$$I_{cs} = A_1 V_s + A_2 V_s^2 + A_3 V_s^3 \tag{A.1}$$

$$I_{cg} = B_1 V_s + B_2 V_s^2 + B_3 V_s^3 \tag{A.2}$$

$$V_i = D_1 V_s + D_2 V_s^2 + D_3 V_s^3 \tag{A.3}$$

on the other hand, the I_{cs} and I_{cg} can be introduced by (A.4) and (A.5), respectively.

$$I_{cs} = \alpha g_{mcs} V_i + \alpha^2 g_{mcs}^{'} V_i^2 + \alpha^3 g_{mcs}^{''} V_i^3 \tag{A.4}$$

$$I_{cg} = -g_{mcg} V_i + g_{mcg}^{'} V_i^2 - g_{mcg}^{''} V_i^3 \tag{A.5}$$

The relationship between the coefficients of the CS with coefficients of the V_i is demonstrated in (A.6)-(A.8).

$$A_1 = \alpha g_{mcs} D_1 \quad \text{(A.6)}$$

$$A_2 = \alpha g_{mcs} D_2 + \alpha^2 g'_{mcs} D_1^2 \quad \text{(A.7)}$$

$$A_3 = \alpha g_{mcs} D_3 + 2\alpha^2 g'_{mcs} D_1 D_2 + \alpha^3 g''_{mcs} D_1^3 \quad \text{(A.8)}$$

Taylor series coefficients of the I_{cg} are as follows:

$$B_1 = -g_{mcg} D_1 \quad \text{(A.9)}$$

$$B_2 = -g_{mcg} D_2 + g'_{mcg} D_1^2 \quad \text{(A.10)}$$

$$B_3 = -g_{mcg} D_3 - 2g'_{mcg} D_1 D_2 - g''_{mcg} D_1^3 \quad \text{(A.11)}$$

By a node analysis at the input node, (A.12) can be obtained.

$$I_{cg} = \frac{V_i - V_s}{R_s} + \frac{V_i}{r_{ob}} \quad \text{(A.12)}$$

The coefficients of the V_i is determined by (A.13)-(A.15).

$$D_1 = \frac{1}{R_s\left(R_s^{-1} + r_{ob}^{-1} + g_{mcg}\right)} = 0.5 \quad \text{(A.13)}$$

$$D_2 = \frac{R_s}{8} g'_{mcg} \quad \text{(A.14)}$$

$$D_3 = -\frac{R_s^2}{8} g'^2_{mcg} - \frac{R_s}{8} g''_{mcg} \quad \text{(A.15)}$$

By calculating D_1–D_3, other variable coefficients can be calculated such as A_1-A_3 and B_1-B_3. Finally, Taylor coefficients of the Vout can be calculated by using (A.16).

$$V_{out} = \alpha_{cg} R_{cg} I_{cg} - \alpha_{cs} R_{cs} I_{cs} \quad (16)$$

A Modified Noise Analysis of a Common Source − Common Gate Low Noise Transconductance Amplifier for Sub-micron Technologies

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چکیده

در این مقاله یک تقویت‌کننده ترارسانای کم نویز که از تکنیک حذف نویز و ناخطینگی استفاده می‌کند مورد بررسی قرار گرفته است. روابط متداول با توجه به در نظر گرفتن امپدانس خروجی و خازن پارازتیک بین سورس و گیت ترانزیستورهای زیر میکرون اصلاح شده‌اند. روابط محاسبه شده از روابط دیگر اثبات شده در سایر کارها دقیق‌تر و ساده‌تر هستند. همچنین آنالیزها نشان می‌دهند که نویز ترانزیستور بایاس‌کننده ترانزیستور گیت مشترک، فواید تکنیک حذف نویز را محدود می‌کند. بنابراین ترانزیستور گیت مشترک با یک مقاومت بایاس شده است. این کار سبب بهبود معناداری در میزان نویز شده است. همچنین برای محاسبه خطسانی از سری تیلور استفاده شده است. در این مقاله برای اولین بار خطینگی این ساختار تحلیل شده و رابطه‌ای بسته ارائه گردیده است. سرانجام بر مبنای محاسبات انجام شده، یک رویه طراحی برای طراحان پیشنهاد شده است.

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