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A New Analog-based LO Harmonic Rejection Technique with Tunable Notch Frequency

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ABSTRACT

An effective technique for mixer LO harmonic rejection in a SAW-less wideband receiver front-end is proposed. The proposed technique provides a tunable notch that can be placed at any frequency like mixer LO harmonics, to avoid the aliasing in baseband after mixing. An analog LC notch is used in a cascode transconductor, and it can reject one of the 3rd or 5th harmonics. This notch frequency is tunable using the bond wire inductors or fixed Gyrator-C active inductor, and a capacitor array, without any significant Power/Area overhead on overall system. Since the accurate value of inductance is not clear, a calibration circuit is proposed to tune this LC notch. This tuning phase runs in forground, and consumes very low additional power. This technique is used in a wideband receiver front-end. Post-layout simulation in 130nm CMOS results in an average 3rd harmonic rejection ratio of 36 dB. The overall circuit consums 34mW power and a has a noise figure of 3.4dB at 1GHz frequency.

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1. INTRODUCTION

In the last years, demands for wireless connectivity that can support voice and data have increased. Lower cost solutions have been largely affected by the great advancements in wireless technology. With the progress of integrated circuits (ICs), the implementation of full transmitter/receivers is feasible in a chip, which reduces the total price of communication systems by eliminating the costly discrete components [1-3]. A wideband receiver commonly consists of a wide-band LNA, a mixer, an Analog to Digital Converter (ADC) and a Digital Signal Processor (DSP). In wideband receivers, all radio processes and functions are performed in the digital domain using a digital signal processor (DSP) that follows an analog-to-digital converter. Such a system provides the maximum reconfigurability, but implementation of a wide dynamic range ADC requires a high power budget, and remains impractical for battery-powered wireless devices. Hence, in recent years, other solutions have been proposed in order to realize a suitable SDR receiver. Discrete-time (DT) and mixed-signal solutions are more attractive, and usually include a mixing operation before the ADC. A power-scalable ADC having tunable resolution and bandwidth is usually utilized to save power. These techniques present flexibility and reconfigurability with a relatively low power consumption, appropriate for battery-powered wireless devices.

To realize a wideband receiver, there are several main issues: the out-of-band blockers, the LO harmonics mixing and the total noise figure (NF). The blockers can compress the receiver gain, while the LO harmonics lead to aliasing. The unwanted signals located at the LO harmonic frequencies are also folded to baseband (BB) or Intermediate Frequency (IF) and degrades the Signal-to-Noise Ratio (SNR). On the other hand, the high NF limits the sensitivity of the receiver. Several approaches are proposed to address the blockers problem [3-6] and the noise issue [7, 8].

To overcome the aliasing due to mixer LO harmonics, a harmonic rejection operation with a high Harmonic Rejection Ratio (HRR) in the single receiver is essential to satisfy the precise selectivity requirements. The classical HRMs proposed in [9-11]

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reject the 3rd and 5th harmonics theoretically, but suffer from gain and phase matching issues which limit the harmonic rejection performance to about 35dB. A two-stage approach is presented in [5] to achieve more harmonic rejection.

Passive mixers clocked by local oscillators (LO) translate baseband impedances to RF [12-15]. It has been reported in [10, 16, 17], the receiver front-end includes an LNA and a mixer, where amplifies and downconverts the RF signal to basenband (BB) in continuous-time domain. Several approaches use the RF sampling method [18-21], where the RF signal are sampled with a high rate. On the other hand, LNA-less receivers are proposed that can control the large blockers received from the input antenna [4, 6].

This work presents a wideband receiver front-end with harmonic rejection mixer to remove the most critical of LO harmonic, i.e., 3rd harmonic. The receiver front-end also tolerates the out-of-band blockers.The proposed technique provides a tunable notch that can be located at any desired frequency, e.g; mixer LO harmonics. This, avoid the aliasing in baseband after mixing. Section 2 introduces the main issues of wideband receivers (blockers and LO harmonics). Section 3 presents the proposed solution to harmonic rejection. The main contribution of proposed technique is the effective use of bondwire inductance to suppress a desired harmonic, without any significant Power/Area overhead on overall system. The tuning phase runs in forground, and consumes a very low additional power. On the other hand, the area overhead is negligible. Simulation results in 130nm CMOS are reported in section 4 and are compared with the classical harmonic rejection mixer.

2. WIDEBAND RECEIVERS ISSUES

A weak wanted signal is accompanied by large out-of-band blockers in a receiver. For narrowband receivers, an external SAW filter is commonly used after antenna to suppress the out-of-band blockers before making voltage gain. The SAW filters are expensive and large. Therefore, utilizing them is not practical to realize a multi-band receiver. Nowadays, the technology improvements increase the interests in designing SAW-less receivers, which eliminates the external components. Unlike active mixers, passive mixers have no reverse isolation. In the absence of reverse isolation, passive mixers clocked by local oscillators (LO) translate baseband impedances to RF. So, low-Q baseband impedances are converted to high-Q band-pass filters. Figure 1 shows general solution for a wideband receiver [3] that addresses both the blockers and LO harmonics issues.

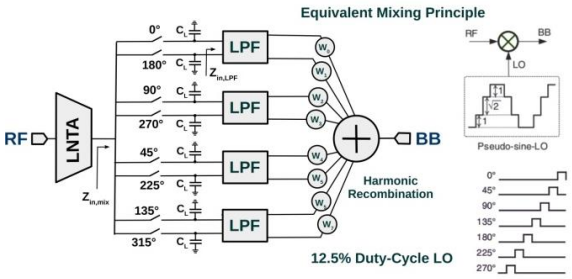

Figure 1. General N-path architecture to achieve both the blocker filtering and harmonic rejection [12]

In RF transceivers, switching mixers are commonly preferred to other topologies. These mixers multiply the signal in a square wave, and generate harmonics of the local oscillator frequency; therefore, a harmonic filtering is required. In the receiver, the resulting down-converted signal has relatively large images of the RF signal located at the odd multiples of the LO frequency. These images can be aliased with the wanted signal at the baseband. Alternatively, to reduce the strength of the 3rd and 5th LO harmonics, a harmonic rejection mixer can be used. The classical harmonic rejection mixer proposed in [9], three square-wave with phases of 0°, 45° and 90° weighted by "$1:\sqrt{2}:1$" are summed to generate a pseudo sine-wave to reject the 3rd and 5th LO harmonics. This technique is shown in Figure 2. The main drawback of this approach is that the irrational number $\sqrt{2}$ is difficult to be accurately implemented in the layout [12]. On the other hand, the harmonic rejection ratio (HRR) is sensitive to both gain and phase mismatches, and limits the HRR to around 35 dB.

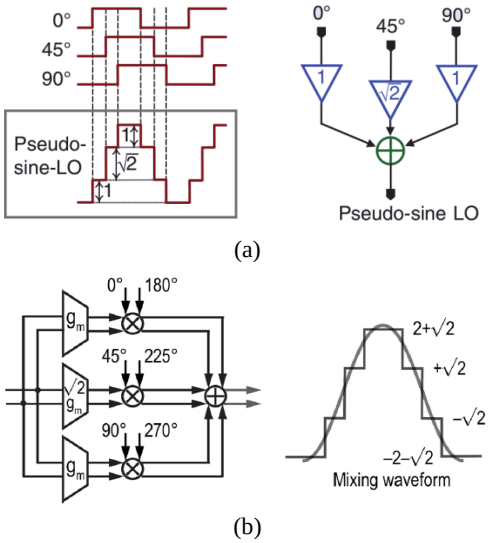

Figure 2. (a) Approximation of a pseudo-sine LO [12](b) Building pseudo-sine LO mixing waveform using three weighted G_m[10]

An automatic local oscillator phase-error detection and calibration circuitry is implemented for the mixers to achieve high HR ratio [22]. Another technique presented in [23], proposes a harmonic rejection mixer that utilizes a ratio of 1:1/3:1/5, as opposed to the irrational number $\sqrt{2}$. The harmonic suppression is controlled by a set of independent gain and phase tuning parameters. Recently, a new two-path time-based approach is published that works based on <50% clock duty cycle and deleyed clock in second path [24].

3. THE PROPOSED TECHNIQUE

3. 1. Principles and Circuit Implementation In order to improve the harmonic rejection, this paper proposes an analog technique that can be integrated with the already proposed receivers. Generally, to achieve a total low noise figure, an amplification is required at the first stage of receiver chain. The voltage gain in an LNA is realized in two steps: a V-I conversion (via trans conductance of a transistor) and an I-V conversion (via impedance or trans-impedance). The two functional blocks are separated by using a passive direct conversion mixer and a low-pass filter (LPF), as shown in Figure 3(a). A particular realization of the general concept is depicted in Figure 3(b) [5]. In this approach the voltage gain at RF is entirely removed. First, a Low Noise Transconductance Amplifier (LNTA) converts the RF voltage to current. Then this RF current is mixed by an LO waveform, and is pushed into a trans-impedance amplifiers (TIA) with a very low input impedance. In fact, the impedance in the output of LNTA is low, and there is no RF voltage gain therefore. The mixed current is filtered in the TIA using R and C to suppress the blockers. It is noticeable that the feedback loop gain has a roll-off at high frequencies, so the input impedance of the TIA is increased. To overcome this problem, a capacitor C_{VG} is used to reduce the impedance at high frequencies. The C_{VG} also contributes to determining the LPF cut-off frequency [5].

Figure 4 shows the block diagram of the proposed receiver front-end based on [5]. This technique is based on placing an analog LC notch in system, and, in theory, it can reject one of the 3rdor 5th harmonics completely.

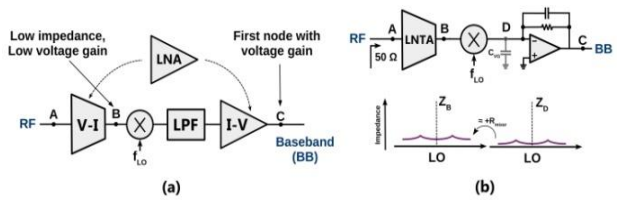

Figure 3. (a) The general concept of current-mode front-end (b) a specific realization [5]

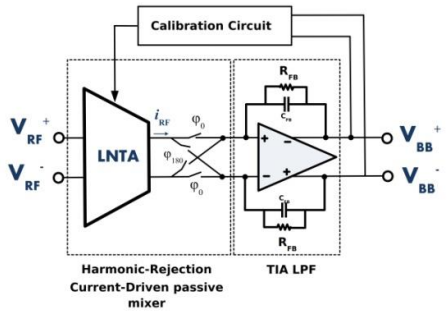

Figure 4. The proposed frond-end with harmonic rejection

This notch is tunable by using a fixed Gyrator-C active inductor and a capacitor array. Moreover, it is possible to use a bond wire inductor, without any extra power consumption. Since the accurate value of inductance is not clear, a digital foreground calibration is proposed to tune the LC notch. To realize this idea, a cascode transconductor architecture is used. Figure 5 shows the cascode transconductor architecture designed in this work and the general concept of proposed harmonic rejection method. Cascode transconductor results in a constant trans conductance within a wideband frequency range from 500 MHz to 5 GHz. The sizes of G_m-cell transistors are listed in Table 1.

3. 2. Calibration System for Tuning Since the accurate value of inductance is not clear (its approximate value is known), the value of capacitance must be set to tune the notch at a desired frequency of $1/\sqrt{LC}$.

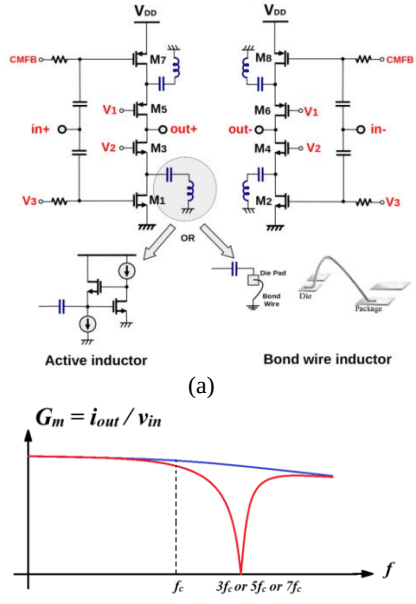

Figure 5. (a) The proposed cascade transconductor with embedded LC filter (b) The wideband frequency range of G_m

TABLE 1. The sizes of G_m-cell transistors

Transitor/capacitor/resistor	Size/value
M1,M2	60/0.130
M3,M4	35/0.130
M5,M6	32/0.130
M7,M8	50/0.130
$\mathbf{R_F}$	2.5kΩ
$\mathbf{C_F}$	1pF

Therefore, a capacitor array with selector switches is required to set the capacitance properly. Figure 6 shows this concept. Typically, a bond wire inductor has an inductance of 1-2 nH. To show the operation of the system, a 1.5nH inductor is considered. If the receiver is tunable for 0.9-5 GHz, a capacitor bank including **M**×100fF MIM-caps can be used to cover the frequencies between 2.7GHz (3rd harmonic of 900MHz) and 5GHz, where **M** is the number of capacitors. To achieve a better resolution, unit capacitance can be reduced; consequently, the number of capacitor increases. The model of bond wire inductor including parasitic capacitor is shown in Figure 6.

A digital foreground calibration set the LC filter capacitance by controlling the switches. A monotone signal with relatively large amplitude at required notch frequency is applied as the input, and a simple closed loop mechanism controls the switches by integrating the output and converting the result to the digital format. A low-power low-bandwidth 5-bit flash ADC (with simple logical operations on its thermometer output) is suitable because the output is in baseband. A 5-Bit ADC can support about 30 capacitors in array (2^5=32). Figure 7 shows the calibration setup. Figure 8 shows the 5-bit flash ADC used in calibration loop.

Foreground calibration operates in offline mode. It can tune the receiver to reject a harmonic interference before the ordinary operation of the receiver. It is easily possible with an RF monotone signal test. The loop of calibration converges rapidly. No extra power dissipation is expected. Moreover, the flash ADC consumes very low power. After tuning, the ADC will be off and the receiver will be ready to work. Figure 8 shows the OTA used in the TIA filter and the integrator and comparator used in the flash ADC.

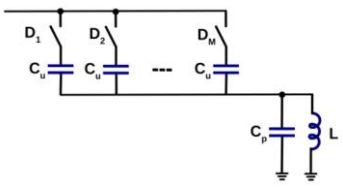

Figure 6. Tuning the LC notch

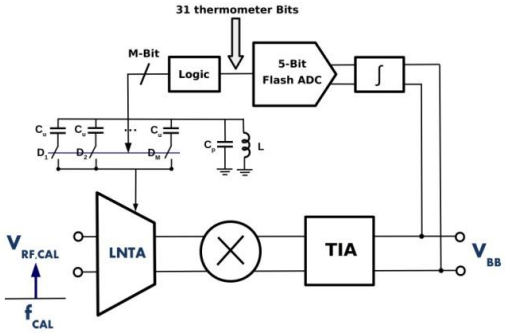

Figure 7. The circuit in calibration phase

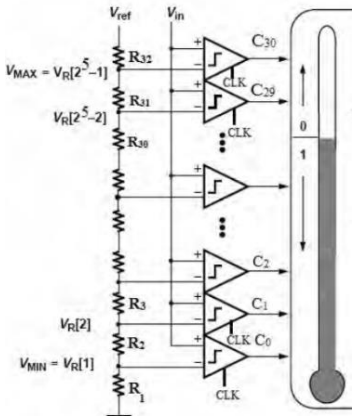

Figure 8. 5-bit Flash ADC (without Thermometer to binary encoder)

The OTA shown in Figure 9(a) is a simple two-stage fully-differential with common-mode feedback for each stage. This amplifier must have a bandwidth depending on the bandwidth of a wanted channel. In this work, the unity-gain bandwidth of the OTA is about 120MHz, which is suitable for the operation of a maximum 20MHz bandwidth in baseband. On the other hand, the OTA used in the integrator has a very low bandwidth, because the output response to calibration signal is a low-frequency one. Figure 9(b) shows the dynamic comparator used in the flash ADC. 31 comparators are needed for a 5-bit Flash ADC. The speed of ADC can be very low.

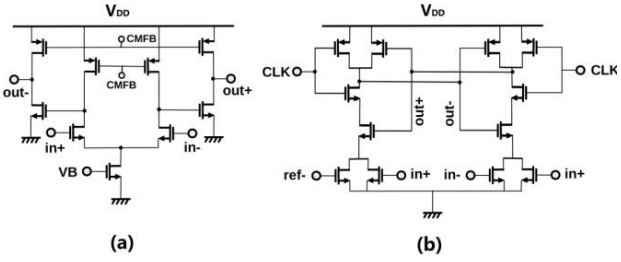

Figure 9. (a) The OTA used in TIA and (b) the comparator used in ADC

3. 3. Gyrator-C Active Inductor considerations A gyrator includes two coupled transconductors. The gyrator-C networks consist of a gyrator and a capacitor connected to one port of the gyrators. If the input and output impedances of the transconductors are infinite and the trans conductance are fixed, the gyrator-C network is lossless. The schematic of a basic gyrator-C active inductor is shown in Figure 10(a). Common-drain and common-source configurations give a positive and negative trans conductance, respectively. An important benefit of this kind of inductor is that all transistors are NMOS, making it attractive for high-frequency applications. The parameters of the equivalent network of the active inductor are given by Equation (1) [25].

$$C_p = C_{gs1}, R_p = \frac{1}{g_{m1}}, L = \frac{C_{gs2}}{g_{m1}g_{m2}}, R_s = \frac{g_{o1}}{g_{m1}g_{m2}} \quad (1)$$

In Equation (1) the parasitic resistance R_p limits the quality factor (Q) of the active inductor. Moreover, the parasitic series resistance R_s decreases the quality factor. In this equation, g_{o1} denotes the output conductance of the M1 in small-signal model, equal to $1/r_{o1}$. To evaluate the quality factor of the active inductor shown in Figure 10(a), the effect of the parasitic series resistance R_s is often negligible, while the effect of R_p is considered resulting in Equation (2) [25].

$$Q \approx \frac{R_p}{\omega L} = \frac{\omega_{t2}}{\omega} \quad (2)$$

Where, $\omega_{t2} = R_p/L$.

3. 4. Noise Figure The small signal analyses compute transfer function by using time-domain techniques. The small-signal noise factor of a differential cascode G_m cell shown in Figure 5 can be calculated by Equation (3).

$$NF = \frac{SNR_{\text{in}}}{SNR_{\text{out}}} = 1 + \frac{\gamma}{2\alpha^2 G_m R_S} \quad (3)$$

where, $\alpha = Z_{\text{in}}/(Z_{\text{in}} + R_S), G_m = 2(g_{m1} + g_{m4})$. In a 50Ω system, a transconductance of at least 10m℧ can guarantee an NF less than 3dB for this first gain stage without impedance matching (α=1). With impedance matching, a greater trans conductance is required. With a 25m℧ trans conductance, the NF will be less than 4dB.

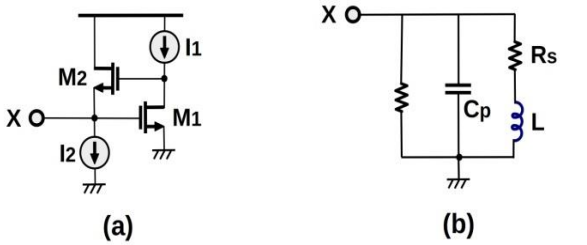

Figure 10(a). The simplified schematic of basic gyrator-C active inductor and (b) The equivalent circuit [25]

4. SIMULATION AND RESULTS

4. 1. The G_m, without LC Filtering The circuit is designed in 130nm with V_{DD}=1.5V, in normal mode, and bias voltages V_{B2} and V_{B3} are DC values equal to 800mV and 350mV, respectively. These values resulted in a trans conductance of about 20 m℧ which is constant in time and in a wideband frequency range. Figure 11 shows this frequency response from 900 MHz to 5 GHz.

4. 2. The G_m, with Proposed LC Filtering To demonstrate the good operation of the proposed harmonic rejection technique, an array consisting of 14 capacitors and switches are used. The capacitance of a unit capacitor is equal to 200fF. It is assumed that the bond wire inductor value is equal to 1.5 nH with a parasitic capacitance of 20fF. Figure 12(a) shows the G_m versus frequency when capacitors are added to circuit from 0 (without any filtering) to 14 with ideal switches. As it can be seen, the notch is variable from 2.5 to 5.5GHz with a good depth, i.e., less than -45dB. It is notable that the G_m at the wanted frequency also reduces slightly, about 1-4 dB. Figure 12(b) shows the curves with MOS switches. It is clear that the depth of the notch is reduced, because the resistance of switches is in the ON state. This problem can be improved by enlarging the size of MOS switches. Figure 12 shows the curves with MOS switches and an active inductor with 0.5 mA currents. Figure 13 shows that by using active inductor, lower notch depth is achieved because the quality factor of active inductor is much lower than the bond wire due to parasitic elements. Moreover, its power consumption is relatively high. Therefore, at high frequencies, using bond wires as inductors help achieve a high performance and a low power idea.

4. 3. Calibration Loop and Convergence To show the operation of the circuit in calibration phase, a monotone 3GHz signal with amplitude of 300mV is applied as input.

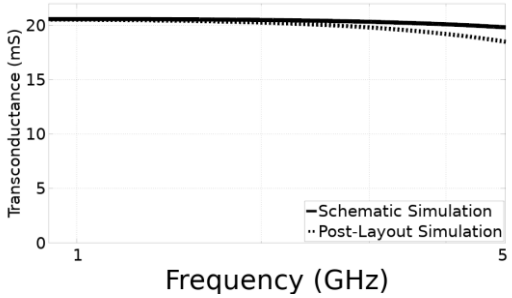

Figure 11. Frequency response of G_m simulated in 130nm CMOS technology. In post-layout simulation, due to parasitic capacitors the G_m slightly drops

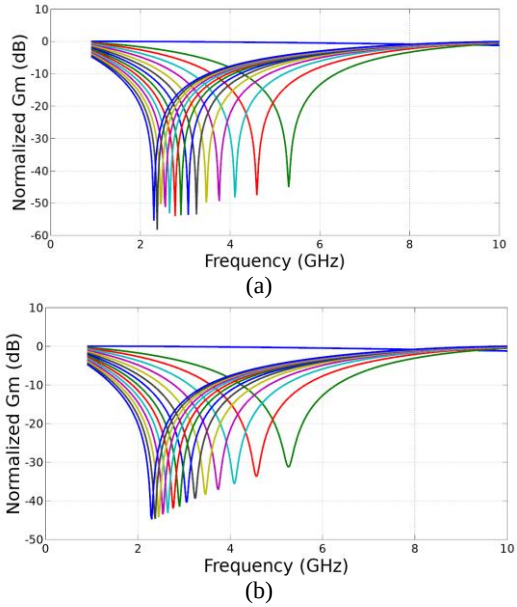

Figure 12. The frequency response of the G_m, with the proposed LC filtering, post-simulated in 130nm CMOS technology with a 1.5nH bond wire inductance (a) with ideal switches and (b) MOS switches

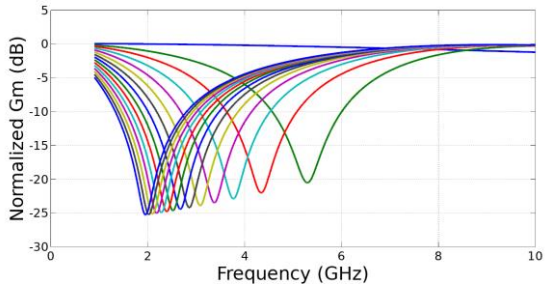

Figure 13. The frequency response of the G_m, with the proposed LC filtering, post-simulated in a 130nm CMOS technology with ≈2nH active inductance and MOS switches

A 1.5nH inductor with a parallel capacitance of 30 fF is used in this simulation as a model for bond wire. Figure 14(a) shows the TIA output voltage over time. The output is degrading along the convergence. The digital control code is shown in Figure 14(b), which in fact is the number of capacitors that are placed in the LC network.

For this case, nine 1.8pF capacitors result in a minimum output value for 3GHz. This values results in $1/\sqrt{LC} = 3.06$ GHz theoretically, which verify the operation of system. In order to decrease the simulation time, calibration clock frequency is set to 20MHz. In practice, the lower frequencies order) are possible to use. By using 20MHz clock, after about 6μs the loop is converged.

To prove the stability of calibration loop, the simplified equivalent model shown in Figure 15 is used.

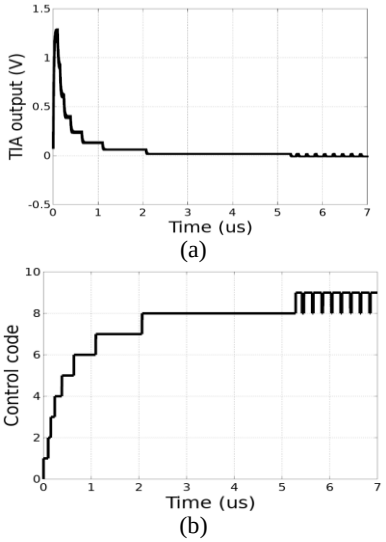

Figure 14 (a). The TIA output voltage over time during calibration phase (b) The digital control code (post-simulation results)

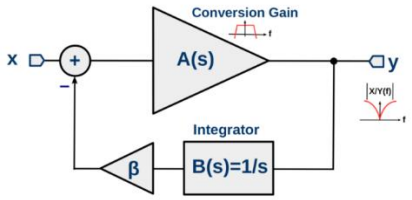

Figure 15. Simplified equivalent model of thecalibration loop

It is noticeable that this is a mixed-signal loop including a nonlinear mixing operation, and its accurate analysis is very complicated and is not helpful. Hence, an equivalent analog loop is used to investigate the stability. The G_m-cell and sampling mixer are modeled by a "conversion gain" block in baseband with a single pole and a gain of $A_0/3$, where A_0 denotes the gain at the fundamental. The feedback signal is subtracted from calibration input signal to minimize the output. In this simplified model, the LC tuning mechanism is modeled by only a gain factor in feedback path.

The transfer function of forward and feedback paths is given by Equation (4).

$$A(s) = \frac{A_0/3}{1+\frac{s}{\omega_p}} \ , B(s) = \frac{\beta}{s} \tag{4}$$

where ω_p, denotes the pole of forward amplifier (translateded gain from around 3rd harmonic to dc), and ω_{RC}=1/RC denotes the RC LPF pole in feedback network. Therefore, the overall transfer function is achieved by Equation (5).

$$H(s) = \frac{A(s)}{1+\beta A(s)B(s)} = \frac{\frac{A_0/3}{1+\frac{s}{\omega_p}}}{1+\left(\frac{A_0/3}{1+\frac{s}{\omega_p}}\times\frac{\beta}{s}\right)} = \frac{\frac{A_0\beta}{3}\,s}{\frac{s^2}{\omega_p}+s+\frac{A_0\beta}{3}} \tag{5}$$

The H(s) has two poles in new places and a zero at s = 0. This means that there is a notch at DC in the overall conversion gain transfer function from 3rd harmonic to baseband. The loop gain transfer function has two poles as shown in Equation (6).

$$T(s) = \beta A(s)B(s) = \frac{A_0/3}{1+\frac{s}{\omega_p}} \times \frac{\beta}{s} \quad (6)$$

In theory, such a system is always stable, but with a good phase margin consideration, the loop convergence response can be without ringing. Figure 16 shows the bode diagram of open-loop system with A_0=50, ω_p = 10MHz. As shown, the unity-gain bandwidth (ω_u) is about 150KHz, and a phase margin of about 90° guarantees the stability of the loop.

4. 4. Harmonic Rejection It is shown that the LC filtering places a notch in frequency response. As mentioned before, it is notable that the G_m at the wanted frequency also reduces slightly, about 1-4 dB. Figure 17 shows the 3rd harmonic rejection ratio versus input frequency from 900MHz to 1.5GHz.

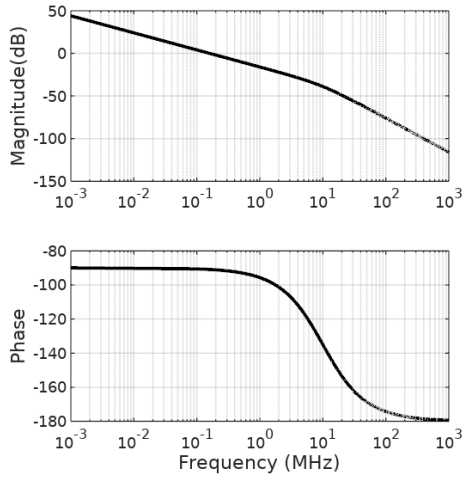

Figure 16. The bode diagram of open loop system

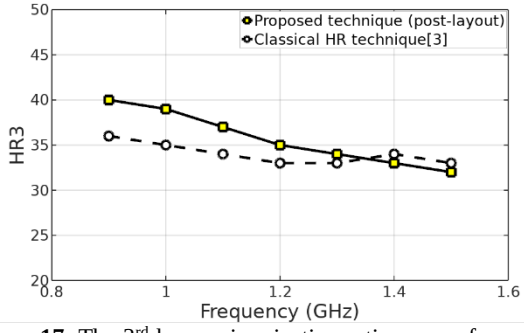

Figure 17. The 3rd harmonic rejection ratio versus frequency, and a comparison with the classical technique [9] (without the calibration of gain and phase mismatches)

The results are compared with the classical harmonic rejection technique [9]. It is mentioned in section 2 that this technique is very sensitive to mismatches, where the HRR is limited to around 35dB. The proposed technique presents a more rejection.

In order to fully consider the mismatches between different devices and their effect on the realized raised cosine modulation, a Monte-Carlo simulation on the full receiver is performed. This Monte-Carlo simulation considers both of the mismatches between devices and different process corner models for the devices. Figure 18 shows the histogram of the HRR values for the 3rd (HRR3) harmonics with a 1 GHz input signal. As shown, the average HRR3 is about 36dB and 95% of the samples have greater than 32 dB.

4. 5. Noise Figure and Power Consumption Figure 19 shows the simulated noise figure of the G_m cell versus frequency. The result is compared with the theoretical Equation (3). The cascode transconductors have a static current of about 2.5mA which results in a static power consumption of 3.75mW (with V_{DD}=1.5V). Cascode architecture has not any extra power consumption as compared to simple inverter-based G_m cell. In comparison with [9], the proposed harmonic rejection mixer uses only one G_m cell, resulting in less power dissipation. The calibration system consumes a total 1.5mW. It is notable that the calibration block operates only at the start of the system operation and it is off after tuning. Therefore, its power consumption is negligible.

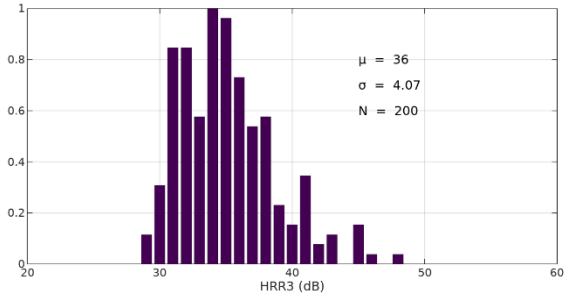

Figure 18. Monte-Carlo simulation results (normalized) of the receiver for 200 runs

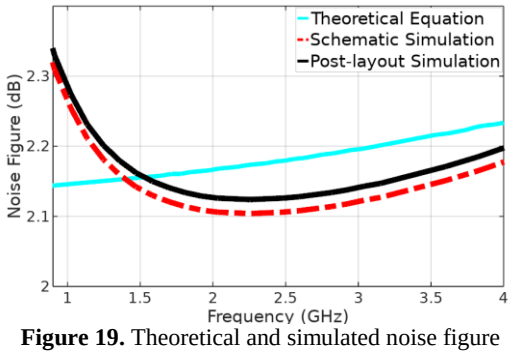

Figure 19. Theoretical and simulated noise figure

Table 2 summarize the specifications of the proposed receiver front-end and compare it to the published state-of-the-art SDR receivers. Several works reported a better harmonic rejection, but the main idea is based on conventional technique [9]: reconstructing a pseudo-sine mixing waveform with "$1:\sqrt{2}:1$" levels. In fact, these works proposed a calibration method to correct the gain and phase mismatches, resulting in a high harmonic rejection ratio. But, in this work, a completely new concept with a few hardware requirements is introduced. The proposed work, simulated in 130 nm CMOS, exhibits a performance that compares well to SDR receivers implemented in more advanced technologies, outlining the potential of the proposed architecture.

The receiver front-end including G_m cell, passive mixer and sampling capacitances are laid out in 130nm CMOS technology as shown in Figure 20.

TABLE 2. The performance summary and comparison(1) Without baseband processing.(2) Without synthesizer

	This work	Andrews [ISSCC'10]	Murphy [JSSC'12]	Ru [JSSC'09]	Bagheri [JSSC'06]	Chen [JSSC'14]
CMOS Technology	130 nm	65 nm	40 nm	65 nm	90 nm	65 nm
Supply Voltage (V)	1.5	1.2 / 2.5	1.3	1.2	1 / 2.5	1.2
Frequency (GHz)	0.8 ~ 4	0.4 ~ 6	0.08 ~ 2.7	0.4 ~ 0.9	0.8 ~ 5	0.5 ~ 3
NF (dB)	3.3 @ 1GHz (1)	5.5	1.5 ~ 2.5	4	5 ~ 5.5	5.5 ~ 7.8
HRR3 (dB)	35 (average) 40 @ 1 GHz input	35	41	> 60	38	> 45
Power Consumption (mW)	34 (1)	37 ~ 70 (2)	35 ~ 78 (2)	60 (1)	>100 (2)	250 ~ 600
Area (mm^2)	≈0.1 (1)	2 (2)	2 (2)	1 (2)	3.8	5.9

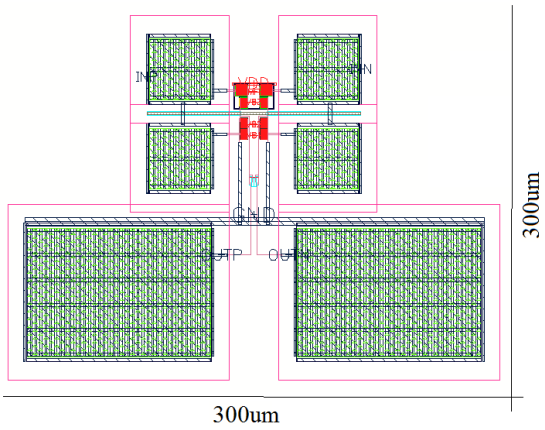

Figure 20. Layout of the receiver front-end in 130nm CMOS without calibration circuit

5. CONCLUSION

In this paper, an effective technique for mixer LO harmonic rejection in a SAW-less wideband receiver front-end is presented. The proposed technique provides a tunable notch which can be located at any desired frequency, e.g., at mixer LO harmonics. An analog LC notch is used in a cascode transconductor, and it can reject one of the 3rdor 5th harmonics. This notch frequency is tunable by using a fixed Gyrator-C active inductor, or bond wire inductor, and a capacitor array. Since the accurate value of inductance is not clear, a digital foreground calibration is proposed to tune this LC notch. The main contribution of proposed technique is the effective use of bondwire inductance to suppress a desired harmonic, without any significant Power/Area overhead on overall system. The tuning phase runs in forground, and consumes a verylow additional power. The area overhead is limited to capacitor bank and calibration loop, that are negligible. Post-layout simulation results of the 130nm CMOS operating at a 1.5-V supply and consuming 34 mW show that, for a 1 GHz RF input, the receiver has a harmonic rejection of 40 dB for the 3rd harmonic. A 200-runs Monte carlo simulation with a 1 GHz input signal results in an average HRR3 of about 36dB.

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A New Analog-based LO Harmonic Rejection Technique with Tunable Notch Frequency

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چکیده

در این مقاله تکنیکی موثر برای حذف هارمونیک محلی مخلوط کننده در گیرنده‌های پهن باندی که دارای فیلتر موج اکوستیکی سطحی نیستند پیشنهاد شده است.تکنیک پیشنهادی یک ناچ قابل تنظیم ایجاد می‌کند که قادر است در هرفرکانسیمانند هارمونیک‌های محلی مخلوط کننده قرار گیرد واز تداخل در باند پایه بعد از عمل مخلوط شوندگی جلوگیری نماید. در این تکنیک یک ناچ سلف–خازنی آنالوگ در مدار هدایت انتقالی آبشاری استفاده شده است و قادر است یکی از هارمونیک‌های سوم یا پنجم را حذف نماید.ناچ فرکانسی مورد نظر با استفاده از سلف ناشی از سیم اتصال دهنده پد به پایه تراشه ویا یک سلف فعال ژیراتور–خازنی به همراه رشته خازنی قایل تنظیم است، بدون اینکه سربار توان/مساحت زیادی روی کل سیستم داشته باشد.از آنجایی که مقدار دقیق سلف نامشخص است یک کالیبراسیون برای تنظیم نمودن ناچ سلف–خازنی مورد نظر استفاده شده است.این کالیبراسیون به صورت پیش‌زمینه‌ای انجام می‌شود و توان بسیار کمی مصرف می‌کند. این تکنیک روی ورودی یک گیرنده باند پهن پیاده سازی شد و نتایج شبیه‌سازی بعد از جانمایی در تکنولوژی ۱۳۰ نانومتر CMOS نشان دادند که یک نسبت حذف هارمونیک میانگین ۳٦ دسی بل به دست آمد. توان مصرفی برابر ۳٤ میلی وات و عدد نویز در فرکانس ۱ گیگاهرتز برابر ۳/٤ دسی بل به دست آمده است.

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