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A High Gain and Forward Body Biastwo-stage Ultra-wideband Low Noise Amplifier with Inductive Feedback in 180 nm CMOS Process

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ABSTRACT

This paper presents a two-stage low-noise ultra-wideband amplifier to obtain the high and smooth gain in 180nm CMOS Technology. The proposed structure has two common source stages with inductive feedback. The first stage is designed for 3GHz frequency and the second stage is designed about 8GHz. In the simulation, symmetric inductors of TSMC 0.18um CMOS technology in ADS software is used. Simulation results show high and relatively smooth S21 equal to 18.674±1.38dB, the noise figure of less than 3.7dB, the power consumption of 14.6mW with 1.2V supply voltage and suitable matching at the input (S11<-10.8dB) in 3.1 to 10.6 GHz frequency range. Moreover, IIP3 of this circuit is -9.5dBm at the 7GHz frequency.

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1. INTRODUCTION

Ultra-Wideband (UWB) is a radio technology used for wireless data transmission with higher speed at low energy levels [1]. UWB is suitable for short range applications. In amplitude and frequency modulation, message signal requires a carrier for transmission; thus, an oscillator or mixer is required; but, in UWB technology, the carrier wave is not used. In UWB technology, short time pulses with ultra-low power are used instead of the carrier wave and this increases data transmission rate, accuracy and reduces the cost of manufacturing transmitter and receiver [1].

Ultra-wideband low noise amplifier is the main block in communication receiver [2] after receiving the signal via the antenna. Since the received signal level is very low, noise is one of the main parameters in designs. In addition, smooth and proper gain, input matching [3] and low power consumption are other features of low noise amplifiers. Different topologies are used in designing low noise amplifiers where each one has its own advantages and disadvantages. Common-gate amplifiers which have an input resistance of 1⁄gm might be suitable option for a low-noise amplifier [4], on the other hand, they produce more noise compared to common-source amplifiers. In order to reduce the noise of common-gate amplifier, noise cancellation techniques are used [5]. A common gate structure with a negative feedback has been proposed [6]. This circuit has low power consumption, but this power reduction has caused to increase the noise figure. Also, a common gate structure has been used at the first stage due to smaller input resistance [7]. Comparing with other works, the technique introduced in this apper presents smoother gain. Common-source configuration cannot establish matching conditions alone; thus, it is used along with resistive feedback [8]. It has been reported in literature [9], a common source structure with resistive feedback has been used along with noise cancelling technique. This amplifier has been designed in proper power situations and its noise figure is almost acceptable considering the consumption power level but its gain is not flat. Using resistive feedback and the inductance at the gate, 50-ohm input matching is established, but inductance of gate degrades noise figure significantly due to a limited quality factor of the inductance and its value cannot be more than 0.5nH. In

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order to solve this problem, this paper has employed a two-stage amplifier to which an inductive feedback obtain a smooth and high gain.

This paper is organized as follows: The second section investigates the performance of the circuit. Section 3 presents simulation results and section 4 concludes the paper.

2. PROPOSED UWB LNA

The proposed structure is shown in Figure 1 and Table 1. Since achieving a suitable flat gain in 3.1 to 10.6 GHz using one stage is difficult, this circuit is comprised of two common-source stages. First stage which includes transistors M_1 and M_2 which is designed about 3 GHz and the second stage includes transistors M_3 and M_4 also designed about 8 GHz so that the resulting configuration gives a smooth gain throughout the whole frequency interval. Gain diagram of each stages and gain of the resulting configuration are shown in Figure 2. Moreover, since the noise of the first stage plays the main role in noise figure, it has been tried to design the first stage as low noise as possible and the second stage gives more freedom to smooth the gain. Figure 3 shows noise of each stage and resulting noise of two stages. As can be seen in Figure 3, total noise of the circuit is equal to the noise of the first stage and the second stage does not affect much noise. The inductors L_{G1} and L_{G2} can increase bandwidth by changing resonance frequency. What should be noted is that L_{G1} and L_{G2} have a series resistance equal to LW/Q. This series resistance significantly degrades noise figure of the circuit. Figures 4 and 5 show noise figure of the circuit in terms of L_{G1} and L_{G2} at 10.6 GHz. It can be seen that for values higher than 0.5nH, noise figure increases with a high slope. In this paper, feedback inductances are used to smooth the gain. Inductances in feedback create less noise at the output compared to those at the gate. Therefore, these inductances can be selected for smoothing gain with more freedom (L_{F1} and L_{F2}). Equation (1) shows the input impedance of the first transistor (M1). Equations (2) and (3) calculate the gain of each stages. Equation (4) represents total gain. It can be seen that feedback inductances L_{F1} and L_{F2} significantly affect the gain of stages which can be adjusted to obtain a smooth gain in the whole frequency range. Figures 6 and 7 show S21 parameter for different values of L_{F2} and L_{F1}. It can be seen that smooth gain is obtained between 3.1GHz to 10.6GHz for L_{F1}=0.8469 nH and L_{F2}=1.0 nH.

$$Z_1 = Z_{F1} \| \left(\frac{1}{C_{gs1} S} + L_{S1} S + \frac{g_{m1} L_{S1}}{C_{GS1}} \right) \quad (1)$$

$$A_{V1} = \frac{g_{m2} Z_{D1}}{(1+g_{m2} Z_{F1})} \frac{-Z_{F1} g_{m1} Z_1}{(1+L_{S1} g_{m1} + L_{S1} S C_{GS1})(Z_1 + R_S + L_{G1} S + \frac{1}{C_1 S}) + g_{m1} R_S Z_1} \quad (2)$$

$$A_{V2} = \frac{g_{m3} Z_{D2}}{(1+g_{m3} Z_{F2})} \frac{-Z_{F2}^2 g_{m4}}{Z_{F2}(1+g_{m4} R_{o1}) + R_{o1} + \frac{1}{C_2 S} + L_{G2} S} \quad (3)$$

$$A_V = A_{V1} A_{V2} \quad (4)$$

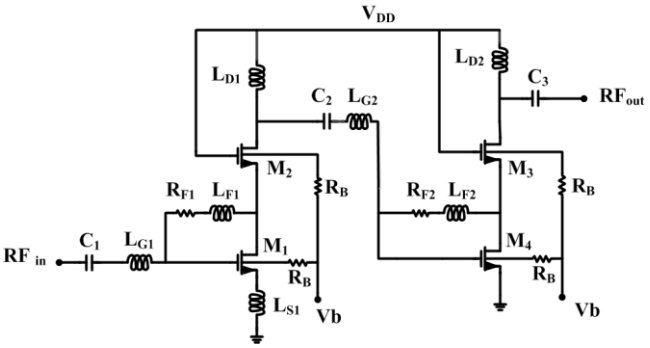

Figure 1. Shematic of proposed uwb LNA

TABLE 1. Design values of proposed LNA

M_1	(5.7µm/0.18 µm)×64	C_2	1pF	RB	5k Ω
M_2	(3.7µm/0.18 µm)×40	C_3	1pF	L_{s1}	0.11 nH
M_3	(2.3µm/0.18 µm)×60	L_{G2}	0.585 nH	L_{D1}	1.1 nH
M_4	(4.0µm/0.18 µm)×40	R_{F2}	209 Ω	L_{G1}	0.333 nH
R_{F1}	171 Ω	L_{D2}	0.8nH	L_{F2}	1.0nH
V_{DD}	1.2 v	Vb	0.6 v		
C_1	5.7pF	L_{F1}	0.869 nH		

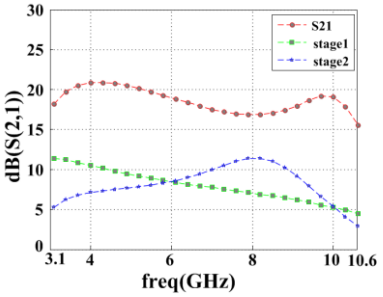

Figure 2. Simulated S21 parameter of 2-stages and total S21

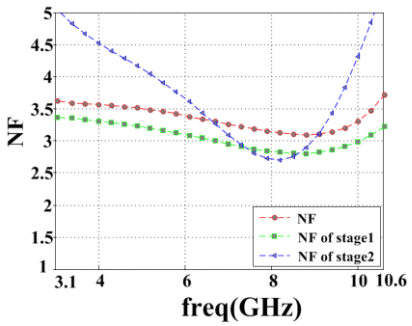

Figure 3. Simulated frequency responses of stages NF and total NF of 2 stages

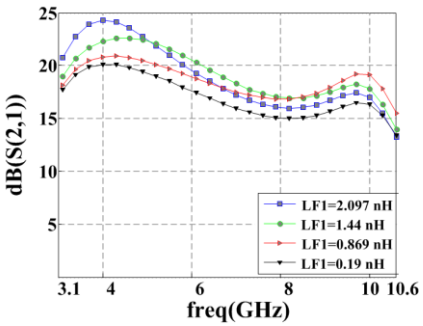

Figure 7. Simulated S21 of the circuit for different values of L_{F1}

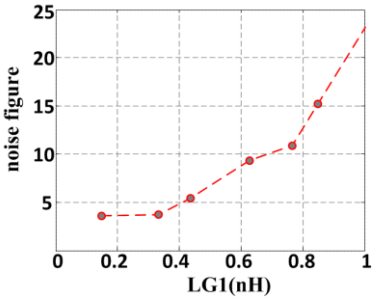

Figure 4. Simulated noise figure of the circuit in terms of L_{G1}at 10.6 GHz frequency

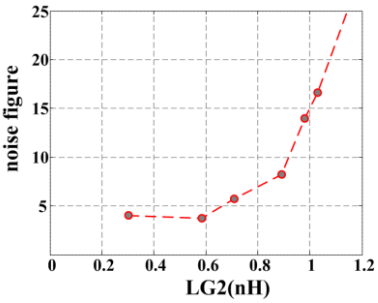

Figure 5. Simulated noise figure of the circuit in terms of L_{G2} at 10.6 GHz frequency

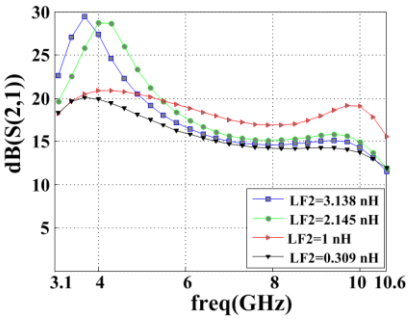

Figure 6. Simulated S21 of the circuit for different values of L_{F2}

In this paper, Forward body bias technique is used. Threshold voltage for NMOS transistors can be changed by the following equation:

$$V_{th}=V_{th0}+\gamma(\sqrt{2\Phi_F+V_{SB}}-\sqrt{2\Phi_F}) \quad (5)$$

where, Φ_F and V_{th0} are the surface Fermi potential and threshold voltage for zero substrate bias voltage (V_{SB} = 0V) and γ is the body effect parameter [10]. Based on Equation (5), while V_{SB} can be reduced, V_{th} will reduce. By reducing V_{th}, transistors require a lower bias voltage and as a result, the supply voltage can be designed to lower voltage level. 50-ohm input impedance matching is created using an inductance at source (L_{S1}) and inductive feedback. Figure 8 shows circuit model of the input impedance. In addition, Equation (6) gives the relationship of the input impedance.

$$Z_{in}=R_S+\frac{1}{C_1S}+L_GS+\left[\left(Z_{F1}\frac{1+g_{m1}L_{S1}S}{1+g_{m1}L_{S1}S+\frac{g_{m1}}{g_{m2}}}\right)\|\left(\frac{1}{C_{GS1}S}+L_{S1}S+\frac{g_{m1}L_S}{C_{GS1}}\right)\right] \quad (6)$$

A parameter which can be used for stability characteristic is Stern stability coefficient and can be defined as Equation (7). Equation 8 has defined Δ. If K>1 and Δ<1, the circuit is absolutely stable. That is, it does not oscillate with any combination of source impedances and load [8]. Figures 9 and 10 show that the designed circuit is absolutely stable.

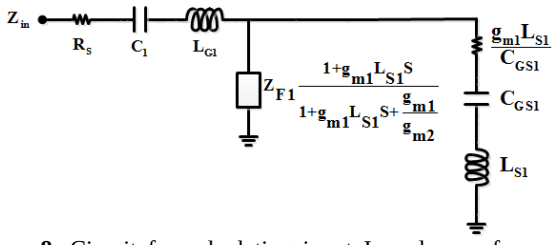

Figure 8. Circuit for calculating input Impedance of proposed UWB LNA

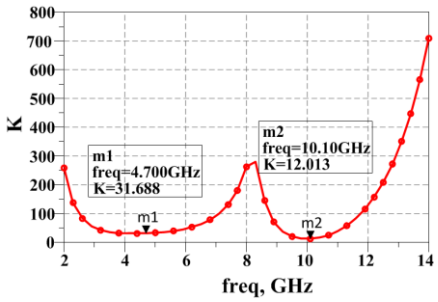

Figure 9. stability factor k

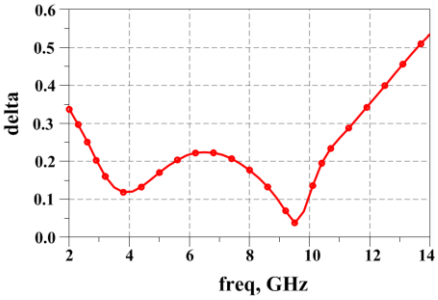

Figure 10. Δ of the proposed uwb LNA

$$K=\frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \quad (7)$$

$$\Delta=S_{11}S_{22}-S_{12}S_{21} \quad (8)$$

3. SIMULATION AND RESULTS

In designing of the proposed UWB low-noise amplifier, TSMC 0.18µmRFCMOS Technology is used for all transistors, Inductors, Resistors, and Capacitors of the circuit. Also, the inductors of the INDS2_SYM model is used. The total power consumption of the circuit is 14.6mW. Noise figure, input matching, and circuit gain are simulated using ADS Software at -40 to 85 degrees centigrade at different process corner. Figure 11 shows noise figure of proposed LNA. At TT process corner and at 27ºC, circuit noise figure is obtained between 3.1dB and 3.7dB. At SS process corner and at 85ºC, circuit noise figure is obtained between 3.8dB and 4.4 dB. Moreover, at FF process corner and at -40 degrees of centigrade, noise figure is reduced and varies between 2.2 to 3.3 dB. As can be clearly seen in the Figure 12, the input impedance matching (S11) versus frequency is fairly preserved with respect to the PVT variation. Figure 13 shows S21 of the circuit using L_{F1}=0.869nH and L_{F2}=1nH which has a proper gain in the whole frequency interval. In addition, simulation results for IIP3 are shown in Figure 14 which are obtained using two tones with 10MHz spacing at 7GHz. Input power is swept from -70 dBm to 10 dBm and IIP3 at 7GHz is -9.5dBm. Additionally, Table 2 compares the structure with other UWB low noise amplifier circuits.

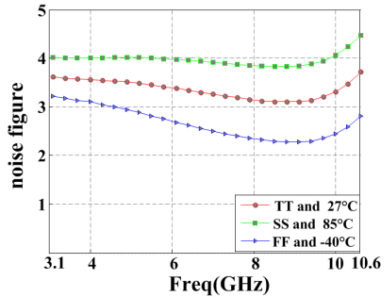

Figure 11. Simulation result of noise figure

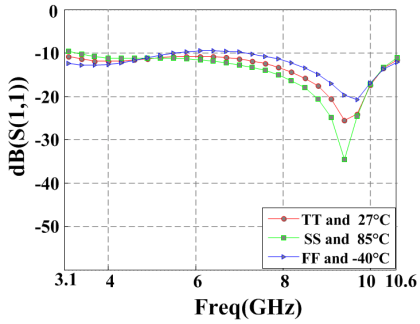

Figure 12. Simulation result of S11 parameter

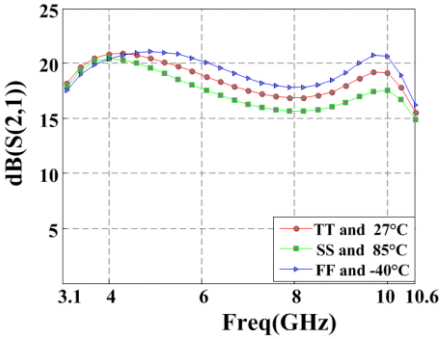

Figure 13. Simulation result of S21 parameter

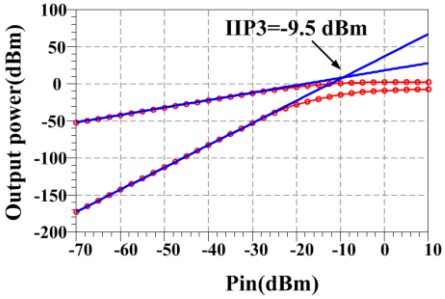

Figure 14. Simulation result of IIP3 at 7 GHz

TABLE 2. Comparison of the proposed LNA with recently simulated UWB LNAs

Process [nm]	BW [GHz]	S21 [dB]	S11 [dB]	NF [dB]	IIP3 [dBm]	Power [mw]	FOM	Reference
180	3.1-10.6	18.67 ± 1.38	<-10.8	3.1-3.7	-9.5	14.6	10.305	This work
130	2.35-9.37	10.3 [c]	<-8	3.68 [d]	-4	9.97	5.43	[11][a]
90	2.5 – 10.9	10.3	< -11	2.6	10.4	15.6	6.76	[12][b]
180	3.1-10.6	11.5 ± 1.1	< -10	2.9-5.4	-4.6	15.2	6.54	[13]
180	2-6.5	11	< -10	2.7	4.4	7.6	7.55	[14]
130	4.7-11.7	12.4	< -11.9	2.9	-3	13.5	6.76	[15]
130	2.6-10.7	13.5	< -11	2.7	5	13.5	9.39	[16]
180	3-5	22	< -13.5	4.5	-2	10	2.41	[17][b]

This table employs FOM (defined in literature [11]) measures to compare the performance of the proposed low noise amplifier with other UWB low noise amplifier circuits.

$$FOM = \frac{S_{21}(\text{dB}) \times BW(\text{GHz})}{(F-1) \times P_{DC}(\text{mw})} \quad (9)$$

In Equation (9), S_{21} is absolute maximum voltage gain, P_{DC} show power consumption is in mW, BW show bandwidth in GHz and F is minimum noise factor of LNA.

4. CONCLUSIONS

In designing the proposed UWB low noise amplifier, TSMC 0.18um CMOS Technology is used. In this structure, inductances are used in the feedback network to control the gain of stages which can be adjusted to obtain a proper gain in the whole frequency range between 3.1 to 10.6 GHz. In addition, the proposed amplifier performs well between -40º to 85ºC and different process corners. The noise figure of this circuit is less than 3.7dB and its power consumption is 14.6mW, the voltage gain of LNA is 18.674±1.38dB and good input matching S11<-10.8 is obtained between 3.1 to 10.6 GHz. Moreover, IIP3 of the proposed amplifier is -9.5 dBm at 7GHz frequency.

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چکیده

در این مقاله یک تقویت‌کننده کم‌نویز فوق پهن‌باند دو طبقه برای دستیابی به گین بالا و هموار در تکنولوژی ۱۸۰ نانومتر معرفی شده است. ساختار پیشنهادی دارای دو طبقه تقویت‌کننده سورس‌مشترک همراه با فیدبک سلفی می‌باشد. طبقه اول حول فرکانس ۳ GHz و طبقه دوم حول فرکانس ۸ GHz طراحی شده است. درشبیه‌سازی از سلف‌های متقارن تکنولوژی TSMC 0.18um CMOS در نرم‌افزار ADS استفاده شده است. نتایج شبیه‌سازی S21 بالا و نسبتاً هموار dB ۱۸/۱±٦٧٤/۳۸، عدد نویز کمتر از ۳/۷ dB، توان مصرفی ١٤/٦ میلی وات با ولتاژ تغذیه ۱/۲ ولت و تطبیق مناسب در ورودی (S11<-10 dB) را در گستره فرکانسی ۳/۱ تا ١٠/٦ گیگاهرتز نشان می‌دهد. همچنین این مدار دارای IIP3 برابر ۹/۵- dBm در فرکانس ۷ گیگاهرتز می‌باشد.

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