International Journal of Engineering

Journal Homepage: www.ije.ir

Low Dropout Based Noise Minimization of Active Mode Power Gated Circuit

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P A P E R I N F O

Paper history:
Received 14 August 2016
Received in revised form 02 December 2017
Accepted 04 February 2018

Keywords:
Architecture
Power-gating
Data-retention
Leakage
Noise
Low-dropout Voltage

A B S T R A C T

The presence of package inductance induces large voltage fluctuation (bounce noise) on the power rail during power down to power up transition in the power gating circuit that may cause unwanted transitions in neighboring circuits. In this work, a power gating architecture is developed for minimizing power in active mode. Noise for the architecture has also been analyzed. The effect of various noise minimization approaches for reducing power supply noise have been evaluated in power gating architecture. A new concept of noise minimization technique using Low Dropout Voltage Regulator has been proposed in this paper. The amount of charge in the internal nodes that passes through the sleep transistor during the wake-up transition has been controlled by the proposed noise minimization techniques. The Low Dropout Voltage Regulator is designed with a target of reducing bounce noise by minimizing voltage fluctuations on the power rail. Low noise active mode power gating architectures have been designed in Synopsys Custom Designer tool at iPDK 90nm technology. Saving of noise at the power supply rail has been observed up to 99%.

***doi**: 10.5829/ije.2018.31.09c.10*

1. INTRODUCTION

Low power VLSI devices and circuits have been a subject of keen research interest in today's era of deep submicron technologies. Suppression of the sub-threshold leakage current and control of transistor count per chip, is highly desirable to extend the battery lifetime of high-performance portable applications with long idle periods. For reducing leakage power, different power gating (PG) structures with high performance in the active mode and short wake-up time during standby mode have been proposed in literature [1-3]. During active mode, runtime leakage is also minimized using PG techniques [4, 5]. But many negative circuit level aspects of PG, such as power supply noise, large instantaneous current through sleep transistor (ST) etc. necessitate a careful understanding of its impact on the behavior of circuits. These aspects can be controlled by controlling the current through the sleep transistor during sleep to active mode transition. Previously different strategies has been developed in order to minimize this kind of noise. Some of the literatures related to this noise in the PG circuit are described next, in this section.

1. 1. Step-wise Turn-on Approach Kim et al. [6] have reported the ground bounce noise is reduced by turning the sleep transistors ON in a non-uniform stepwise manner. Based on literatures [7, 8], a three-step turn-ON strategy is presented to suppress this bounce noise. Kumar et al. [9] stated that delay and bounce noise are controlled in four steps by turning ON the parallelly connected ST gradually.

1. 2. Two-step Turn-on Approach In, tri-mode PG structure ground bounce noise is suppressed with a two-step transition in the park mode during the sleep to active mode [10]. A dual-switch circuit technique is described in literature [11] with a ground bounce noise suppression methodology. A tri-transistor controlled circuit technique is presented in literature [12] to suppress the ground bounce noise in gated-VDD and ground MTCMOS circuits. A tri-mode PG structure [10] is also proposed in literature [13] for the reduction of noise in sequential MTCMOS circuit.

1. 3. Stacking PG Approach According to Saxena et al. [14], high performance stacking PG structure is implemented to reduce ground bounce noise and leakage

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Please cite this article as: D. Nath, S. N. Pradhan, Low Dropout Based Noise Minimization of Active Mode Power Gated Circuit, International Journal of Engineering (IJE), IJE TRANSACTIONS C: Aspects Vol. 31, No. 9, (September 2018) 1546-1552

current. Sreenivasulu and Rao [15] reported that transistor sizing techniques are adopted to reduce ground bounce noise. Based on literature [16], low leakage multiplier circuit is designed to control ground bounce noise using a stacked sleep transistor with a delayed select signal. Kumar et al. [17] stated that multi-VDD level converter is used in PG technique to reduce the leakage current and ground bounce.

1. 4. Low Dropout Voltage Regulator (LDO) The fluctuations in the power supply and the ground line also can be minimized by LDO. Over the past years, number of LDOs have been designed having certain advantages as well as shortcomings, one over the other. Wu et al. [18] proposed LDO shows a reduction in the load regulation and dropout voltage with a low PSRR (44dB). A CMOS LDO of 0.4V dropout voltage is designed by Hicham and Qjidaa [19] using wideband and low-current circuit technique. Kugelstadt [20] has introduced a relatively less efficient LDO which is designed with a 1nF internal capacitor. Based on Giustolisi et al. [21], a robust compensation technique is applied in LDO regulators to reduce the compensation capacitor. A capacitor less LDO regulator architecture was presented by Torres et al. [22].

1. 5. PG Circuit and Bounce Nois A new design of PG approach (active power gated (APG) circuit) in active mode has been developed. In this work, effect of ground bounce noise of poposed active power gated (APG) circuit is analyzed using various ground bounce noise minimization approaches [12, 13] under SOC configuration.

LDO regulator has been designed with the target of reducing power supply noise. LDO regulator has been implemented in the proposed PG architecture in order to reduce more noise on the power over other noise minimization technique.

2. PROPOSED ACTIVE POWER GATING ARCHITECTURE

Architecture of new Active Power Gating (APG) approach is shown in Figure 1. This architecture differs from literature [5] in sequential part and data retention part of the design. In this design, both the combinational and sequential blocks are power gated by ST at the positive edge of the clock cycle, whereas reported in literatures [4, 5], only combinational part is power gated. PG of Retention logic is not done for retaining states. Here, PG is applied in the active mode within the clock cycle to minimize the runtime leakage if idle time is present. Three retention logics are used, two of them ('retention logic 1 negedgeclk' (RL1), 'retention logic 2 negedgeclk' (RL2)) are controlled by the negative edge of the clock cycle and another one ('retention logic 3 posedgeclk (RL3)') is controlled by the positive edge of the clock cycle.

The complete timing diagram of the proposed architecture is shown in Figure 2. During the hold time (T_{hold}) RL1 and RL2 separate the combinational logic from the sequential logic while RL3 passes all the previous states of combinational logic. These states are propagated through the sequential logic and RL1. After hold time, combinational logic and sequential logic are power gated at the remaining part of the positive clock cycle (T_{PGoff}) to reduce leakage power during which no intermediate nodes are passed. At the negative edge of clock cycle ($T_{PGstart}$), combinational block becomes active and RL3 is turned-OFF. During the evaluation time (T_{eval}), circuit blocks evaluate its state (T_{eval}). After evaluation, RL2 allows the data for evaluation at this stage. Then, the states propagate through the sequential logic and pass through the RL1. During the setup time (T_{setup}) inputs change its states. This process is repeated at the next positive edge.

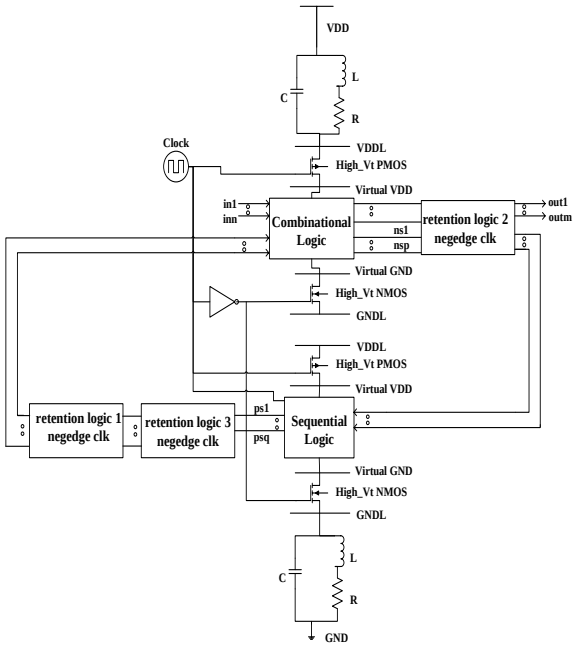

Figure 1. Proposed architecture of APG

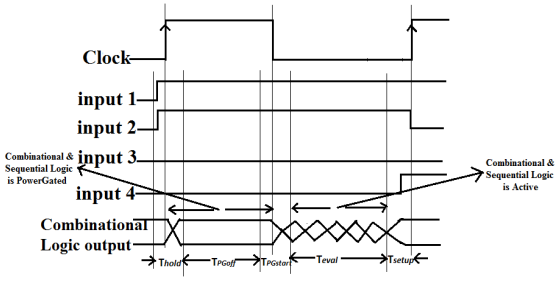

Figure 2. Timing diagram of APG architecture

3. NOISE MINIMIZATION APPROACHES

Here, parasitic components: resistance, inductance, and capacitance of the 40-pin Dual In-line Package (DIP-40) [23] assumed in the proposed APG design are 0.217Ω, 8.18nH and 5.32pF respectively for capturing more accurate behavior of the circuit which is not considered in litretures [4, 5]. In this paper, Tri-Mode PG (ckt1), Dual-Switch PG (ckt2), 3-Transistor Controlled PG high V_T (ckt3), 3-Transistor Controlled PG low V_T (ckt4) approaches are implemented in APG architecture to show the effect of noise on the proposed architecture. A benchmark circuit s27 [24] is taken to implement these architectures. Noise immune designs are simulated and noise results are reported.

4. PROPOSED LOW DROPOUT VOLTAGE REGULATOR (LDO)

The basic LDO circuit [20] consists of a pass device (PD), 'voltage reference' circuit (VR) and error amplifier (EA) with loop control logic. In this work, PD (Figure 3) is implemented with four PNP transistors in Darlington pattern which is quite different from other works. This type of configuration is adopted to generate constant load voltage at high load current with low dropout voltage and low quiescent current for high efficiency. Figure 6 shows the optimized LDO architecture with proposed pass device circuitry that generate desired stable output voltage.

A feedback type bandgap reference circuit (Figure 4) is designed according to the specifications for producing a fixed voltage irrespective of power supply variations, temperature changes and loading on the device. Bandgap circuit produces a fixed voltage by adding a voltage that increases with temperature to a voltage that decreases with temperature. These types of voltage can be generated by tapping the base-emitter voltage (V_{BE}) and using difference in V_{BE} of bipolar junction transistors. In this bandgap circuit, two current components (I_1, I_2) are generated which are proportional to V_{EB1} and V_{EB2}. Current mirror by shorting the gates of M_1 and M_2, is used to force currents into a pair of bipolar transistors whose base emitter voltage difference is used to establish ΔV_{BE}. To create ΔV_{BE} drop at R_3, V_1 and V_2 should be equal. The OPAMP is so designed that the two node voltages V_1 and V_2 are always equal. Normally for ideal OPAMP, V_1 and V_2 are always equal as no current flows into the inputs. To make node voltage V_1 and V_2 equal, the currents I_1, I_2 and resistors R_1, R_2 are fixed at an equal value. R_3 value should be smaller than R_1, R_2 to create ΔV_{BE} and temperature incisive of V_{REF}. The current equations of M_1 & M_2 are:

$$I_1 = k_1 \times (V_{GS1} - V_{T1})^2 \times (1 + \lambda_1 \times V_{DS1}) \quad (1)$$

$$I_2 = k_2 \times (V_{GS2} - V_{T2})^2 \times (1 + \lambda_2 \times V_{DS2}) \quad (2)$$

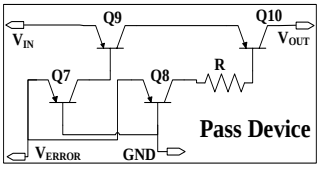

Figure 3. Pass Device

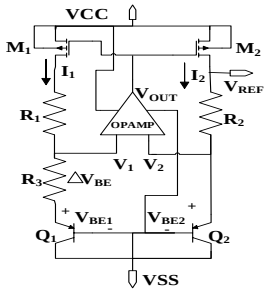

Figure 4. Bandgap reference circuit

where, V_{GS}, V_{DS}, V_T and λ are gate to source voltage, drain to source voltage, threshold voltage and channel length modulation parameter respectively. From these two equations of I_1 and I_2, it is found that:

$$\frac{I_2}{I_1} = \frac{k_2 \times (1+\lambda_2 \times V_{DS2})}{k_1 \times (1+\lambda_1 \times V_{DS1})} \quad (3)$$

Here, $\lambda \times V_{DS} \ll 1$.
So, we can neglect λV_{DS} from the above equation and the new equation will form in the following manner,

$$\frac{I_2}{I_1} = \frac{K_2}{K_1} \quad (4)$$

where, k_1 and k_2 are aspect ratio. The transistors have been chosen as identical, so the W/L ratio (k) of these two transistors are same, i.e. $I_1=I_2$. Current flow through Q_1 and Q_2 are:

$$I_1 = I_{s1} e^{\frac{V_{BE1}}{V_{TV}}} \quad (5)$$

$$V_{BE1} = V_{TV} \ln \frac{I_1}{I_{s1}} \quad (6)$$

$$I_2 = I_{s2} e^{\frac{V_{BE2}}{V_{TV}}} \quad (7)$$

$$V_{BE2} = V_{TV} \ln \frac{I_2}{I_{s2}} \quad (8)$$

since $V_1=V_2=V_{BE2}$, if we apply KVL between two transistors Q_1 and Q_2, the equation will become:

$$V_{BE2} - I_1 \times R_3 - V_{BE1} = 0 \Rightarrow I_1 = \frac{V_{BE2}-V_{BE1}}{R_3} = \frac{\Delta V_{BE}}{R_3} \quad (9)$$

where, $\Delta V_{BE} = V_{TV} \ln \frac{I_2 \times I_{S1}}{I_1 \times I_{S2}}$, V_{TV}=Thermal voltage $V_1 = I_1R_1$, $V_2=I_2R_2$, since, $V_1=V_2 \Rightarrow I_1R_1=I_2R_2$.
Now, apply KVL from V_{REF} node to ground along R_3 and Q_2 to determine V_{REF}.

$$V_{REF} = V_2 + I_2R_2 \quad (10)$$

$$V_{REF} = V_{BE2} + I_1R_1 \quad (11)$$

$$V_{REF} = V_{BE2} + \frac{\Delta V_{BE}}{R_3} R_2 \quad (12)$$

Hence, the reference circuit produces a temperature incisive voltage as V_{BE2} decreases and V increases with temperature.

A differential amplifier is used as an EA (Figure 5) to compare the scaled-down version (V_{SO}) of the output (produced by resistors using voltage divider rule) with the fixed reference voltage (V_{REF}). As, proposed PD should be optimized, hence, to drive this device, amplifier is also optimized accordingly. This amplifier is designed using current mirror topology. Current through both the transistors are equal. Sizes of parallel transistors are set as identical (M_1=M_0, M_2=M_3, M_4=M_5) to generate equal amount of current.

The output voltage is maintained by proper design of pass device (PD) and adjusting the ratio of two resistors (R_3, R_2). The PD must be large enough to guarantee the minimum dropout voltage while providing the maximum load current. The output of the differential amplifier (V_{ERROR}) drives the emitter terminal of the two PNP transistors (Q_7, Q_8). To boost up the current at maximum level, collector terminals of Q_7 & Q_8 are connected to the base terminals of other two transistors (Q_9, Q_{10}) acting as a Darlington pair. Lowest voltage drop is achieved by the voltage across the transistors (Q_9, Q_{10}) which is the minimum input-output differential. Here, very low load resistance (R_4) is used at the output end. Dropout voltage of the LDO circuit is given by:

$V_{DO} = V_{IN} - V_{OUT}$

$V_{DO} = 2V_{CE}$ ($\approx$ 250mV for this proposed LDO)

By setting the resistor value (R_3, R_2), the 'scaled down voltage (V_{SO})' is set and is compared with the fixed reference voltage (V_{REF}). This difference voltage (V_{ERROR} = V_{SO}-V_{REF}) drives the PD. When the base-emitter voltage of PNP transistors exceeds 0.6 volts, then base current starts to flow to turn-ON the PD. Output current and the output voltage increases. Again, this output voltage is scaled down and is compared with the reference voltage. Difference of this voltage runs the transistors to increase the output current. After a particular time (V_{ERROR} = 0), it enters into the saturation region and constant output current flows, then the output voltage is also fixed.

$$V_{SO} = V_{OUT} \times \frac{R_1}{R_1+R_2}, \quad (13)$$

when, $V_{ERROR} = V_{SO} - V_{REF} = 0$, then, $V_{SO} = V_{REF}$:

$$V_{OUT} = (1 + \frac{R_2}{R_1}) \times V_{REF} \quad (14)$$

Equation (14) is true when V_{IN} is sufficiently high to keep differential amplifier and pass device in saturation region. In this region, V_{OUT} becomes constant which set V_{DO} to very low voltage.

As part of its regulation, differential amplifier and bandgap reference circuit of LDO can attenuate any spikes in the input voltage which have some deviation from the internal reference.

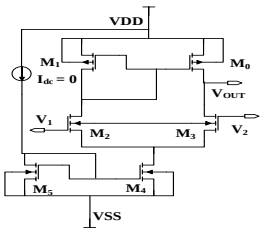

Figure 5. Error amplifier (EA) circuit

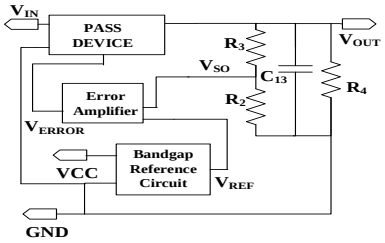

Figure 6. Proposed LDO architecture

High PSRR LDO can be generated by minimizing dropout voltage. So, spikes on power rail can be suppressed by using the high PSRR LDO in the circuit. If LDO regulator is used in the power line of PG architecture, then only this device can regulate fluctuated supply voltage during PG mode. It can also help the neighboring circuits to function correctly while sharing the same power line.

5. PROPOSED NOISE MINIMIZATION SCHEME USING LDO IN APG ARCHITECTURE

In this paper, this architecture implemented considering package inductance is termed as ckt5 (Figure 7). The proposed LDO regulator is attached between the high_V_T transistor (ST) and the power rail (V_{DDL}) in APG architecture.

Noise on power rail can be defined by:

$$\Delta V = (V_{DD} - V_{DDL}) \cong L\frac{d}{dt} I(\xi, t), \quad (15)$$

where,ξ=(V_{DD}-V_{DDL}), V_{DD} = supply voltage, V_{DDL}= voltage drop at power rail.

During mode transition of PG circuit, voltage drops on power rail due to the flow of high current leads to increase in noise ($\Delta V = V_{DD} - V_{DDL}$). To overcome this problem, high PSRR with low dropout LDO regulator is proposed and implemented in the PG circuit that can reject spikes on the power rail (V_{DDL}) using its internal differential amplifier, bandgap reference circuit and pass device. LDO reduces variation on the power rail (V_{DDL}) by regulating the voltage of V_{DDL} node. This in turn increases the value of V_{DDL} node near to VDD. Hence, noise (ΔV=V_{DD} - V_{DDL}) on the power rail reduces which leads to decrease in the rate of change of current ($\frac{d}{dt} I(\xi, t)$) flow through the power rail. There is no contribution of noise due to current drawn by the LDO circuit as on chip VDD drives LDO.

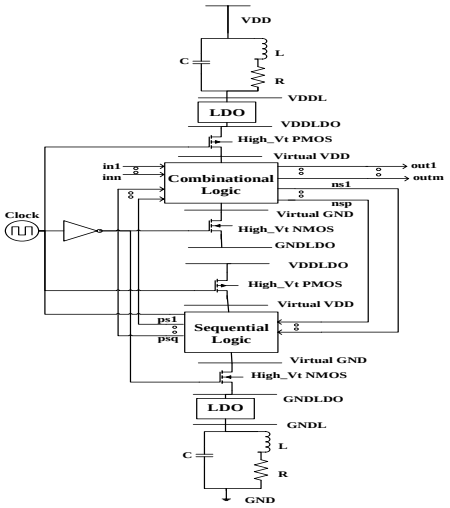

Figure 7. A scheme of using LDO regulator in APG (ckt5)

6. SIMULATION RESULT

The designs of proposed modified APG and ckt1, ckt2, ckt3, ckt4, ckt5 and LDO are implemented taking benchmark circuit- s27. It is observed from Table 1, that with the reduction of the frequency of operation as idle time increases, APG design becomes more efficient to reduce leakage. Power saving results of this APG design outperforms the results of the previous PG works [3, 4, 25-27]. Memory access PG reduces the wasted core leakage power by 38.04% [26]. For 16-bit multiplier design at frequency 1MHz, power saving is 29% compared to PG design [4]. Data-Retained PG (DRPG) [27] used to reduce active mode leakage achieves up to 25.7% saving over conventional designs.

At 2.5V input voltage, output and dropout voltage of the proposed LDO is 2.00253V and 247.47mV respectively. This regulator produces load current of 50.3343mA and the quiescent current of 117.79μA. The measured PSRR is as high as 73.97dB with an efficiency of 88.79%.

LDO maintains around 250mV dropout voltage in between 2-3V input voltage and plot of line regulation is shown in Figure 8.

It is also seen that LDO maintains output voltage of about 2.3V with the variation of input voltage from 2.25 – 2.75V (Figure 9).

TABLE 1. Percentage saving of power over no PG

Frequency (MHz)	%Saving in Average Power of APG over no PG	%Saving in Leakage of APG over no PG
f=1.25	54.78	86.83
f=1.67	17.81	68.33
f=2.50	10.63	47.33

The variation of output voltage with the changes of load current from 30 to 50mA is shown in Figure 10. The load regulation of the proposed LDO is observed to be 2.28%.

This proposed LDO provides output voltage of about 2V by varying the load resistance (R_4) from 30Ω to 100Ω. It is shown that, output voltage is almost constant at higher load resistance (5 - 10KΩ) as shown in Figure 11.

The variation in output voltage with respect to temperature is also observed for the proposed LDO circuit (Figure 12). From the Figure 12, it is seen that output voltage becomes constant after room temperature attainment for the proposed LDO circuit. Then, bounce noise produced by the ckt1, ckt2, ckt3, ckt4, ckt5 in PG circuit during sleep to active mode is discussed.

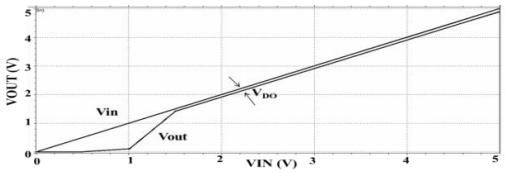

Figure 8. Output voltage Vs input voltage

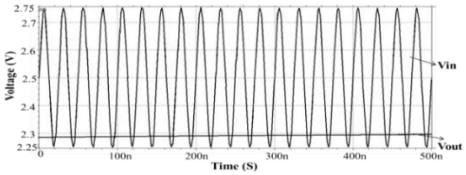

Figure 9. Transient response of voltage

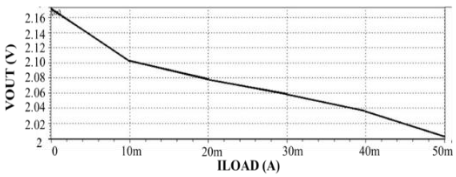

Figure 10. Output voltage Vs load current

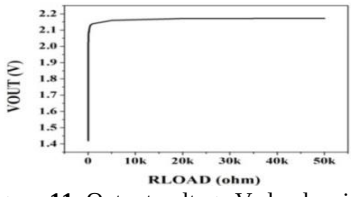

Figure 11. Output voltage Vs load resistance

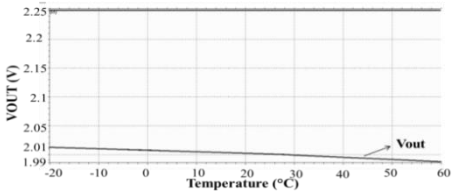

Figure 12. Output voltage vs temperature

From Table 2, it is observed that noise on the power supply (0.06mV) in ckt5 is lower than the ckt1, ckt2, ckt3, ckt4 over APG. There is a large deviation in the voltage level of power supply with package inductance in APG. Whereas, there is less peak to peak variation in power rail with the noise reduction logic of the PG circuits. Percentage saving of noise (peak to peak variation) over APG is also shown in Figure 13.

Percentage saving of noise on the power rail in ckt5 is 98% compared to the ckt1, ckt2, ckt3, ckt4. Transient analysis of peak to peak noise produced on the power rail using LDO regulator for ckt5 is shown in Figure 14. From Table 3, it is found that, proposed noise reduction approach gives better result compared to other previous works. Using proposed concept voltage fluctuation reduces significantly, but power and area occupancy increases due to the extra circuit component of LDO.

TABLE 2. Peak to Peak Noise on Power Rail over APG

Peak to Peak Noise on Power Rail (mV)					
APG	**Ckt1**	**Ckt2**	**Ckt3**	**Ckt4**	**Ckt5**
2.69	2.23	1.5	2.4	1	0.06

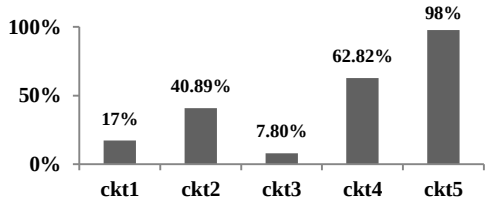

Figure 13. Saving of Noise on Power Rail over APG

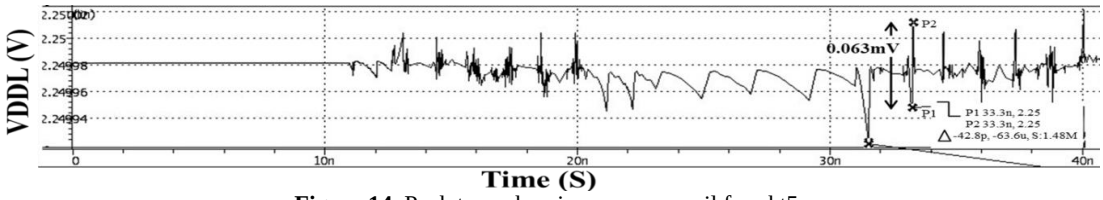

Figure 14. Peak to peak noise on power rail for ckt5

TABLE 3. Noise reduction comparison with previous work

	[7]	**[12]**	**[13]**	**[15]**	**Proposed Work**
Noise reduction (%)	30-74	63.93	94.16	76.28	99

7. CONCLUSION

In this paper, a new PG architecture is proposed for minimization of noise and power. PG is applied for both the combinational and sequential block in active mode. But, PG circuit also suffers from noise on the power rail during sleep to active mode. Effectiveness of different noise reduction approaches in this proposed architecture have also been analyzed in this paper. All the circuits - APG, ckt1, ckt2, ckt3, ckt4, ckt5 have been designed for reduction of noise on the power supply. Peak to peak voltage fluctuation is reduced more in this scheme of using low dropout voltage regulator in PG architecture compared to the other approaches.

8. ACKNOWLEDGEMENT

This work is supported by SMDP-C2SD project, sponsored by MeitY, Govt. of India.

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Low Dropout Based Noise Minimization of Active Mode Power Gated Circuit

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P A P E R I N F O

Paper history:
Received 14 August 2016
Received in revised form 02 December 2017
Accepted 04 February 2018

Keywords:
Architecture
Power-gating
Data-retention
Leakage Noise
Low-dropout Voltage

چکیده

حضور بسته القایی باعث ایجاد نوسان ولتاژ بالا (بانس نویز) در طی انتقال توان بالا به پایین بر روی ریل قدرت در مدار گیت قدرت می‌شود که ممکن است تغییرات ناخواسته را در مدارهای مجاور ایجاد کند. در این کار یک طراحی گیت قدرت برای کاهش توان در حالت فعال توسعه داده شده است. نویز نیز برای این طراحی تحلیل شده است. تأثیر روش‌های مختلف کاهش نویز برای کاهش نویز منبع تغذیه در طراحی گیت قدرت ارزیابی شده است. در این مقاله، یک مفهوم جدید از روش کمینه‌سازی نویز با استفاده از رگولاتور ولتاژ خروجی پایین پیشنهاد شده است. مقدار شارژ در گره‌های داخلی که از طریق ترانزیستور خواب در طول گذر از بیداری عبور می‌کند، توسط تکنیک‌های کمینه‌سازی نویز پیشنهاد شده کنترل شده است. رگولاتور ولتاژ پایین خروجی با هدف کاهش نویز گشتاور از طریق به حداقل رساندن نوسانات ولتاژ بر روی ریل قدرت طراحی شده است. طراحی‌های گیت قدرت در حالت فعال و نویز کم توسط ابزار Synopsys Custom Designer در تکنولوژی 90 nm iPDK طراحی شده‌اند. صرفه‌جویی در نویز در ریل منبع تغذیه تا ۹۹٪ مشاهده شده است.

***doi**: 10.5829/ije.2018.31.09c.10*