International Journal of Engineering

Two Novel Flip Flop with Level Triggered Reset in Quantum Dot Cellular Automata

S. Zoka[a], M. Gholami[*b]

[a] Department of Electrical and Computer Engineering, University College of Rouzbahan, Sari, Iran.
[b] Department of Engineering and Technology, University of Mazandaran, Babolsar, Iran

A B S T R A C T

Quantum dot cellular automata (QCA) introduces a pioneer technology in nano scale computer architectures. Employing this technology is one of the solutions to decrease the size of circuits and reduce power dissipation. In this paper, two new optimized FlipFlops with reset input are proposed in quantum dot cellular automata technology. In addition, comparison with related works is performed. The reset pin in the proposed circuits is level triggered. Simulation results demonstrate that both proposed desgins have efficient structures in terms of area, delay and complexity. The proposed structures are simulated using the QCA designer and validated. Simulations of the first proposed level triggered reset D-Flip Flop showed that this circuit has 82 quantum cells and required only two clock cycle for valid operation. In addition, the second proposed architecture for level triggered reset D-Flip Flop has only 85 quantum cells and it needs only one clock cycle for proper operation.

doi: 10.5829/ije.2018.31.03c.03

1. INTRODUCTION

Quantum Cellular Automata (QCA) is a new electronic paradigm for information and communication process. This is considered as a revolutionary nano-scale computational method. An important advantage of QCA over other nano-electronic architectures is that similar cells used to create logic gates can be utilized to construct wires that carry logical signals [1]. QCA allows operating frequency in terahertz range and also it permits element occupancy rate to be 900 times more than the end of CMOS scale unit that is not feasible in current CMOS technology [1]. The advantages of QCA technology have made this technology a good alternative to CMOS in future.

Due to the importance of this emerging technology as well as considering sequential circuits as an integral part of digital circuits, the design of sequential circuits like flip-flops, has been increasingly considered in QCA technology. One of the most common designs of D-type flip-flops is the combination of master and slave structures from two latches, which can be implemented in QCA and is discussed in literature [2]. This

arrangement clearly demonstrates the cascading latch one after the other. 133 cells are used to design this type of flip-flop in QCA; while the wasted area contains about 600 cells. This design needs more than eight clocking zones from input to output; hence the input-output delay is two clocking periods. But most of the memory vectors presented in scientific assemblies are based on D-latch and sequential circuits are level triggered functionally. However, an efficient flip-flop should designed edge triggered. Huang and Lombardi [3] proposed the first design. The relative simplicity of a D-Latch indicates that the sequential design of the QCA can easily be achieved within the Cartesian arrangement. This implementation requires 69 cells and a surface area of 686.93 square nm. It should be noted that due to the need of various digital circuits, including selective counters and frequency dividers to reset-Pin flip-flops, the need for circuits such as QCA technology is strongly felt. In the circuits that was designed so far, the reset pin is not considered in designing circuits. In this paper, we have tried to design optimal D flip-flops for a D-type riser flip-flop with a reset pin to be used in these circuits.

Next section introduces the proposed flip-flops with reset pin. Then, the occupied space and the delay in the

Corresponding Author's Email:m.gholami@umz.ac.ir (M. Gholami)

propagation of the proposed structures will be compared and their simulation and operation will be examined.

2. QCA PRELIMINARIES

QCA cell is the basic unit in QCA circuits, and they consist of four quantum dots that are arranged in a square model. This is shown in Figure 1. Zhang et al. [4]stated that the cell was charged with two additional electrons, which could allow tunneling between different quantum points through clocking mechanism. These electrons tend to occupy opposite locations as a result of their bilateral electrostatic repulsion.

2.1. Basic Structures In QCA design, cells are systematically built to implement the desired gate and connector structures. QCA design is precisely analyzed by cell interactions. The specified framework around each cell is only intended to differentiate a cell from other cells and they do not show any physical system because electrons are quantum mechanical particles.The electrons are able to tunnel between the points of a cell. The electrons adjacent to each other in the cell will interact with each other; hence the polarity of a cell is directly affected by the polarity of its neighboring cells.

This wire is a horizontal row of QCA cells and emits a binary signal from the input to the output due to electrostatic interactions between adjacent cells [5]. If the cell is charged with two additional electrons, the electrons would be arranged in a diagonal way.This type of placement is due to the Coulomb's repulsive forces that do not allow them to be arranged in any other order. When an electron is placed in a cell in a special diameter (logic 1), this polarity consists of electrons located in the vicinity of the QCA with the same polarity. As shown in Figures 2 and 3, wires are made using two types of cells such as ordinary cells and rotated cells. In a 45 degree wire, the propagation of a binary signal between two polarities is alternated [6].

Coulomb interaction between adjacent cells allows logic circuits to be implemented with a simple change in placement of cells in the design.
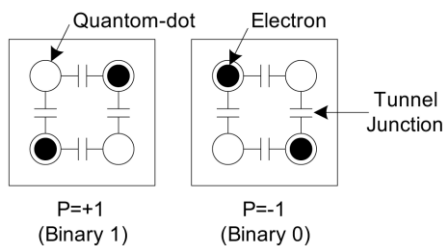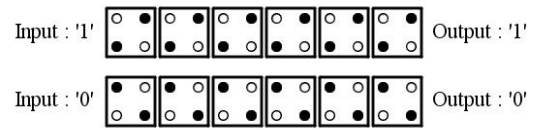

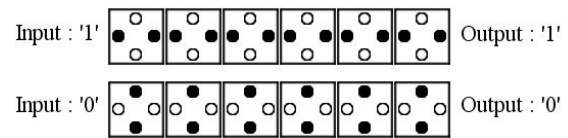**Figure 2.** Wire in QCA technology (90 degree)

Figure 3. Wire in QCA technology (45 degree)

As shown in Figure 4, it is understood that cell placement only takes place by touching their corners, and the inverse electrostatic interaction is created in this manor. Because, the quantum dots associated with different polarities do not match the cells. The binary information is saved in cell 1 and transmitted to cells 2 to 6. The electron pair in the cell 7 reacts to its neighbor, namely, cells 5 and 6, to increase polarity, which is accompanied by a change to opposite polarity.

Inversion in QCA can be implemented in two ways: positioning and rotation. Figure 4 shows an implementation method for positioning which shows the logic input level as inverted in the output. This inverter is known as fork inverter. The output cell is affected by both end and fork cells to ensure that the operation is reliable. In the inverter, the 45-degree displacement in two lines of cellular integration produces the complementary action of the input signal. Contrary to what is common in CMOS as the simplest gate, the inverter occupies a significant area in the QCA.

2.2. Clocking Previously, clocking was not defined in the circuit designed with QCA technology. Therefore, information is transferable without clocking via the wire. To have a fully synchronized circuit using QCA technology, clocking is also used to control the flow of data and the application of pipelines to wires. Another point to note is that the clock cannot be considered as an input for the circuit.
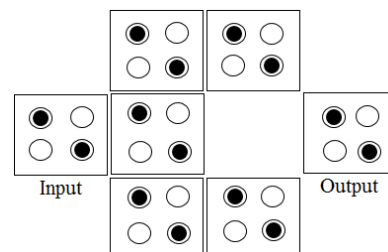

Figure 1. Basic Cell in QCA

Figure 4. Fork inverter in QCA.

By adding this capability, the cells remain in the clocking region with a certain polarity.

The four stages of switching, holding, releasing and relaxing compose a clocking cycle [5]. As shown in Figure 5, each stage has 90 degrees phase difference over the previous stage [5].

- In the switching stage, the energy boundary of elevated electrons inside the cell rises to a point where cell polarity is affected by adjacent cells, and the cell reaches its ultimate binary value [7].
- In the holding phase, the energy of the inner points rises to a point where electrons do not affect the electrons of the adjacent cells, they do not switch, and the cell retains its polarity [8].
- At the releasing stage, the energy of the inner points of the cell decreases to a point where cell loses its polarity [8].
- At the last stage, there is no inner point and the cell has no effect on its adjacent cells [8].

Figure 6 shows clocking stages.

In the QCA Designer software which is used to simulate QCA circuits, each step of the clock is shown in a different color [9]. The green color for the switching stage, the purple for the holding stage, the blue for releasing stage and the white color for the relaxation phase.

Due to the delay in propagation between adjacent cells and energy levels, the number of cells in each hour is limited. A maximum of 28 and a minimum of 2 cells are defined for the permitted number of cells in each stage of the clock. Simulations indicate that the numbers less than 2 cells in an hour may result in signal distortion which leads to poor functioning of the circuit.

3. THE PROPOSED CIRCUITS

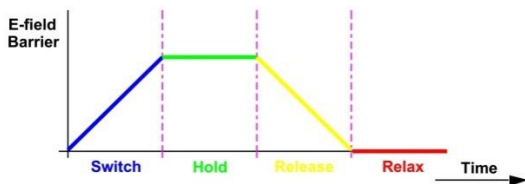The basic design of a D-FF circuit with reset pin is shown in Figure 7.

Figure 5. QCA clock phase

Figure 6. Clocking stage in QCA Designer

Given the shape by setting the value 1 to the reset pin of AND gate, the output value would always be equal to the output of the flip-flop [10]. When the reset value is changed to 0, the output value has to be set to 0 by assuming different values in the flip-flop output. One advantage of designing this type of flip-flop with a reset pin is that the output would change based on the reset pin level. Considering the structure of figure 7, we can provide a D flip-flop with a reset pin. Next, two new structures for D flip-flop with reset pin are provided in QCA technology which are usable in important digital circuits.

Figure 8 shows the original structure as a D flip-flop with reset pin in QCA technology which is based on D flip-flops with optimizing master and slave flip-flops [10]. This includes a D-latch and an edge-to-level converter. The converter section uses the clocking capability of QCA. An AND operator is used between input clock and inverted byte. When the input clock is transmitted from the zero level to the high level (+1), it would increase after clocking four regions. At the end of this flip-flop, the AND gate is used as the reset section, and when it is low, output is reduced to zero. The truth table for the edge-to-level converter is shown in Table 1. As shown in the table, the reset pin acts as an asynchronous flip-flop and does not depend on the clock circuit. Also, returning the value of this base to a logical state, the flip-flop status will return to the previous state.

Regarding the implementation of the first structure provided for the D flip-flop with reset pin (Figure 8), it can be seen that the number of cells in this implementation is about 82 cells and the area lost is about 180 cells. Exactly as usual, delaying the application of the first CLK entry in order to prepare valid output is eight clocking area (or two clocking interval). In the second structure, an optimal D flip-flop with a reset pin is provided.
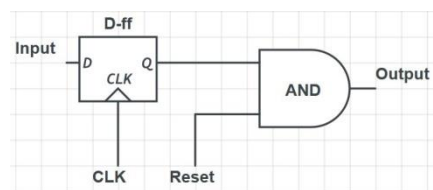
Figure 7. Basic D-ff circuit with reset pin

TABLE 1. The Converter Truth Table[10]

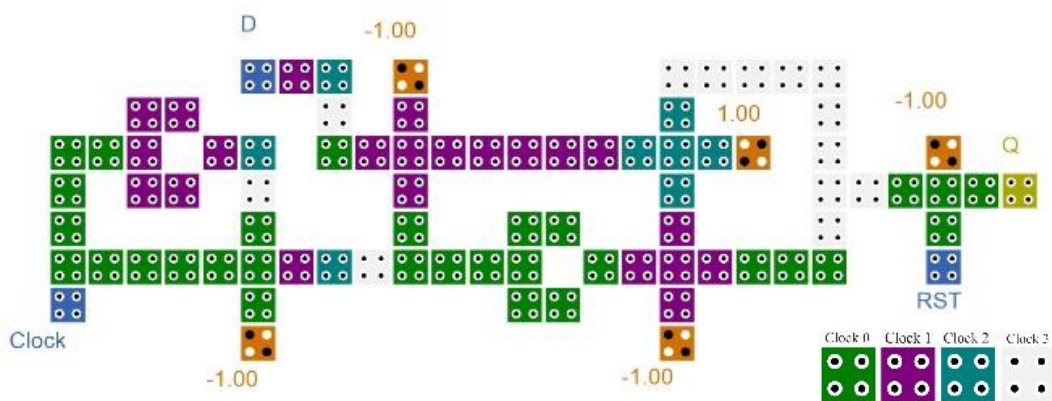| Clock State	CLKNew	$\overline{CLK_{old}}$	OutPut
1	1	-1	-1
-1	-1	1	-1
-1 to 1 Transition	1	1	1
1 to -1 Transition	-1	-1	-1

Figure 8. First proposed circuits with Reset pin

This structure consists of four major gates and one inverter. Delay units are not more than four additional clocking sections on the CLK route. There are four distinct modes that are as follows:

(A) When the CLK remain in + 1:

- The M1 majority gate entries are + 1, Q, + 1 in Figures 9, so the output of q1 is +1.
- In the M2 gates, the values of a and b are both -1, and the output of q2 is-1.
- The majority gate input of M3 is -1, Q, and +1, and the output of this gate equals Q.
- As above, if +1, -1 and Q are the gate inputs of M4 majority gate, their output is Q (which means Q remains in the previous state).

  (B) When the CLK remain in -1:

- The inputs of M1 majority gate are +1, Q, and -1, so its output equals Q.
- In M2 majority gate, a and b values are both +1, and the output of q2 equals +1.
- M3 gate maximum inputs are -1, Q, and -1, and q3 equals -1.
- As above, if Q, +1, and -1 are the inputs of M4 majority gate, the output will equal Q (Q remains in its previous state).

  (C) When the CLK falling from +1 to -1:

- M1 majority gate inputs are +1, Q, and -1 and the output (q1) equals Q.
- In M2 majority gate, a is +1 and b is -1, hence outputs of M2 are +1, input, and -1, and the output results of q2 equals input.
- CLK_{Old} equals +1 in M3, hence the inputs of M3 majority gate are -1, Q, and +1, and the output results of this gate equals q3.
- If Q is the input of M4 majority gate, its output equals Q (Q remains in its previous state).

  (D) When CLK is rising from -1 to +1 (rising edge):

- The inputs of M1 majority gate are +1, Q, and +1, hence the output of q1 remains in +1.

- In M2 majority gate, a is -1 and b is +1, hence the inputs of M2 majority gate are actually -1, +1, and input, and the result of q2 input equals Input.
- In M2 gate, CLK_{Old} value equals -1, hence the inputs of M3 majority gates are -1, Q, and -1, and the result of inputs of this gate (q3) equals -1.
- If +1, Input, and -1 are the inputs of M4 majority gate, its output equals input (Q turns to input value in this condition).

In the second structure for D flip-flop with reset pin which is shown in Figure 10, the number of used cells is 85 and the lost area is approximately 168 cells.

4. SIMULATION AND RESULTS

The simulation results of the first proposed circuit which follows a D type master/slave flip-flop is shown in Figure 11. As it can be seen, changing Reset pin falling to zero will change the output of the flip-flop to zero.
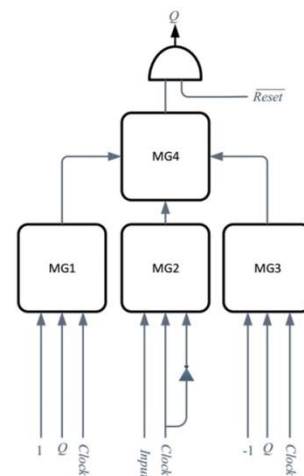

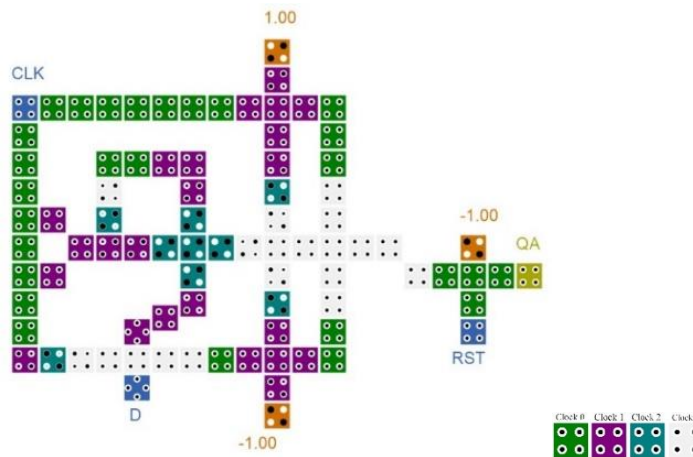**Figure 9.** schematic of proposed Flip-flop

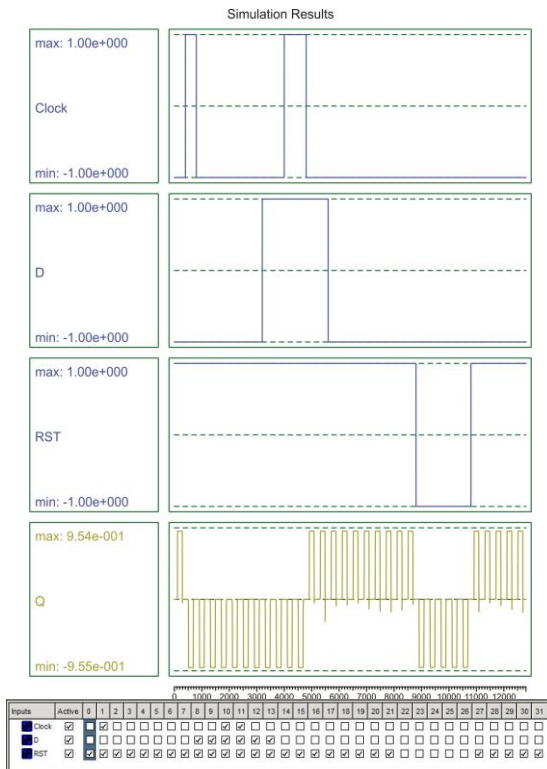**Figure 10.**Implementation of proposed circuit

Figure 11. Simulation result of the first proposedcircuit and the vector table that assign for this simulating

This situation continues until the upper edge of the reset pin is reached. In this flip-flop, 82 quantum cells have been used. Also, the space occupied by this flip-flop is 11.0 square micrometers. Initial clocking at the beginning of this simulation is due to ensuring zero output.

As shown in Figure 12, the results of the proposed second circuit simulation are the same as the proposed circuit, but the delay of the second propagation circuit is

1.25 cycles, and in the first circuit, the propagation delay is 2 cycles. It should also be noted that the occupied space in the second circuit has dropped from 180 cells to approximately 168 cells. In addition to all of these, the results are noticeable after eight clocking in the first circuit. However, in the second circuit, this amount is reduced to four clocking. Table 2 shows the comparison of performance of the two proposed structures.

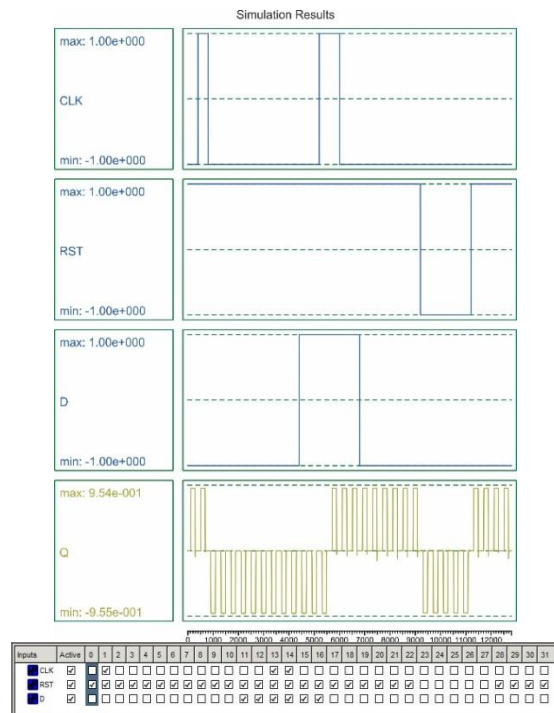Figures 13and 14 presented behavior of proposed flipflops without considering the reset module of there.

Figure 12. Simulation result of the second proposed circuit and relevant vector table
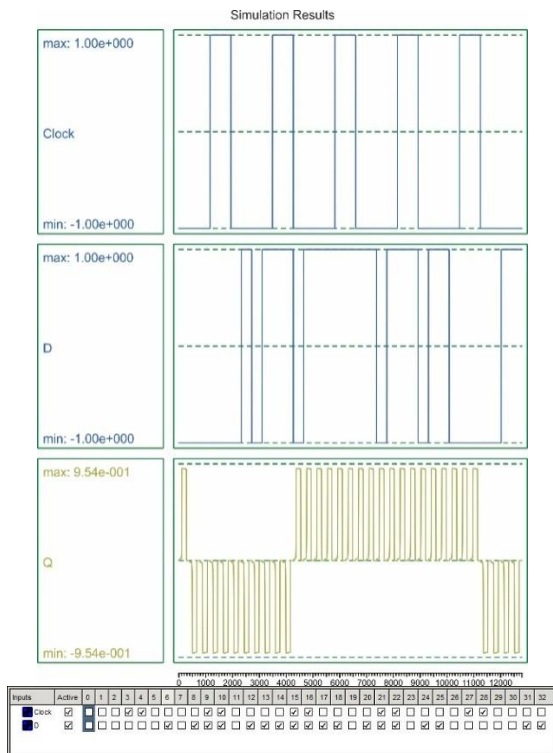
Figure 13. Simulation result of the D-flipflop behavior without reset module for first proposed circuit and relevant vector table
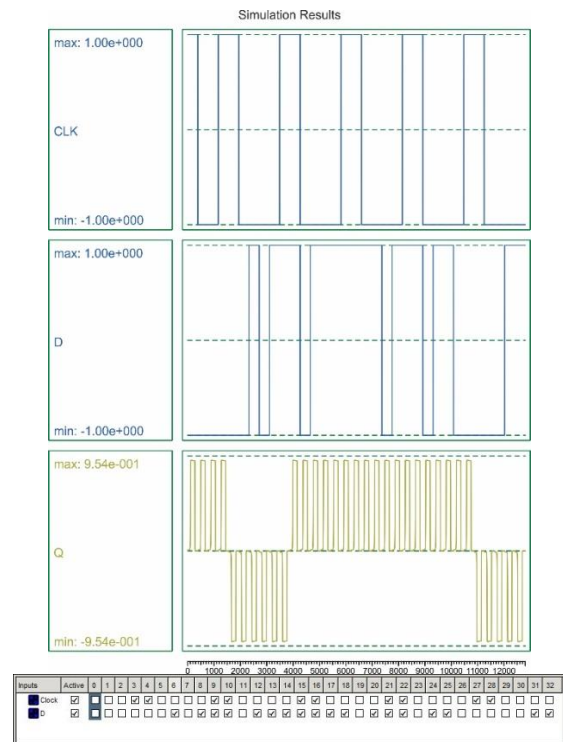

Figure 14. Simulation result of the D-flipflop Behavior without reset module for first proposed circuit

As it can be seen, due to the *Vector Tabel's* for this circuits. Both flipflop designed rising edge triggered and while the rising edge do not injected to clock pin of flipflop, the output remain in preveios state.

5. CUNCLUSIONS

Quantum dot cellular automata (QCA) introduces a pioneer technology in nano scale computer architectures.

In this paper, two new optimized FlipFlops with reset input are proposed in quantum dot cellular automata technology. In addition, comparison with related works is performed. The reset pin in the proposed circuits is level triggered. Simulation results demonstrate that the both proposed desgins have efficient structures in terms of area, delay and complexity. Simulations of the first proposed level triggered reset D-Flip Flop show that this circuit has 82 quantum cells and needs only two clock cycle for valid operation. In addition the second proposed architecture for level triggered reset D-Flip Flop has only 85 quantum cells and it needs only one clock cycle for proper operation.

TABLE 2. Comparison of the proposed QCA circuits

Designs	Complexity(cell count)	Area (um^2)	Area dissipation(cell count)	Delay(clock cycle)	Reset ability	Type of wiring
First Proposed D-flipflop with Reset pin	82	0.11	180	2	Yes	**Coplanar**
Second Proposed D-flipflop with Reset pin	85	0.14	168	1	Yes	**Coplanar**
S.Hashemi D-FlipFlop Without Reset[11]	84	0.09	-	2.75	NO	**Coplanar**
S.Hashemi Dual edge Triggered D-FlipFlop Without Reset [11]	120	0.14	-	3.25	NO	**Coplanar**
A. Vetteth et al Level Triggered D-FlipFlop [12]	68	0.08	-	1.5	NO	**Coplanar**

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S. Zoka[a], M. Gholami[b]

a Department of Electrical and Computer Engineering, University College of Rouzbahan, Sari, Iran.
b Department of Engineering and Technology, University of Mazandaran, Babolsar, Iran

P A P E R I N F O	چکیده

آتوماتای سلولی کوانتومی (QCA) یک فناوری پیشتاز در مقیاس نانو برای طراحی معماری‌های کامپیوتری است. استفاده از این فناوری یکی از راه حل های موجود برای کاهش اندازه مدارهای دیجیتال و کاهش توان مصرفی آنها است. در این مقاله دو فلیپ فلاپ D با ورودی بازنشانی در تکنولوژی آتوماتای کوانتومی سلولی ارائه شده است، به علاوه مقایسه آن با کارهای مرتبط نشان داده شده است. پایه بازنشانی در مدار ارایه شده حساس به سطح است. نتایج شبیه سازی نشان میدهد که هر دو طراحی حاضر ساختارهای موثری از لحاظ فضا و تاخیر و پیچیدگی هستند. ساختارهای ارایه شده توسط نرم افزار QCADesigner شبیه سازی شده اند که صحت انجام آنها را تایید میکند. شبیه سازی اولین فلیپ فلاپ D حساس به لبه ارایه شده نشان میدهد که این مدار ۸۲ سلول کوانتومی دارد و فقط به دو دوره کلاک برای عملکرد صحیح نیاز دارد. به علاوه معماری دوم ارایه شده برای فلیپ فلاپ D حساس به سطح با ورودی بازنشانی ارایه شده تنها به ۸۵ سلول کوانتومی نیاز دارد و در یک دوره ساعت عملکرد مناسب خواهد داشت.

doi: 10.5829/ije.2018.31.03c.03