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RESEARCH NOTE

A Novel Generalized Topology for Multi-level Inverter with Switched Series-parallel DC Sources

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A B S T R A C T

This paper presents a novel topology of single-phase multilevel inverter for low and high power applications. It consists of polarity (Level) generation circuit and H Bridge. The proposed topology can produce higher output voltage levels by connecting DC voltage sources in series and parallel. The proposed topology utilizes minimum number of power electronic devices which helps in reduction of the cost, size, and weight. The proposed topology consumes low power therefore improves the efficiency of the converter. Switching pulses are generated using Phase disposition (PD) pulse width modulation technique. Finally the effectiveness of the proposed topology is verified using MATLAB/SIMULINK software tool. 7level asymmetrical multilevel inverter prototype hardware is prepared to support the proposed topology to verify the effectiveness and its validity.

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NOMENCLATURE

Vo	Output Voltage	$V_{dcm,i}$	i^{th} cell m^{th} DC voltage source
V_{dc1}, V_{dc2}	Voltage connected to each cell	N_{level}	Number of output voltage levels
V_{dcn}	Voltage connected to n^{th} cell	N_{IGBT}	Total number of IGBTS
m	Number of separate DC voltage source	V_{omax}	Maximum output voltage
N_{step}	Number of output voltage steps		

1. INTRODUCTION

Introduction of the multilevel inverters was done in 1975 and initiated with three level inverter [1]. Many sources of DC voltage are synthesized to obtain a staircase identical to sinusoidal output voltage waveform. In recent years MLI is gaining much fame in the field of DC/AC conversion due to less THD, better power quality and good electromagnetic compatibility.

Even after having many merits MLI has few demerits that is to maximize output voltage levels semiconductor switch requirements with peripheral devices like protection circuits, gate driver circuits used extensively. Due to more device count the overall system becomes expensive, stupendous and complicated and minimizes the quality and competency of the converter [2].

MLI are grouped into Cascaded H Bridge, Flying capacitor and Neutral point Clamped traditionally. Cascaded H Bridge is popular due its coherence and easy operation but the limitation of the topology is requirement of isolated DC power supplies [3]. CHB is arranged as asymmetric and symmetric configuration based on magnitude of the DC voltage sources if $V_{dc1} \neq V_{dc2} \neq V_{dc3}$ is asymmetric vice versa. For the same number of power switches the asymmetric configuration of CHB generates more number of voltage levels as compared with symmetric configuration.

The requirement of large number of bidirectional switches is a major issue in asymmetrical topologies. An effort has been attempted to reduce bidirectional

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switches in asymmetrical topology by proposing a new topology in this paper.

The possibility of connecting two or more sources in series and parallel gives enough flexibility for meeting voltage/power requirements in the vehicle drive systems [4].

In this paper the concept of series/parallel connected DC voltage sources based on the basic topology presented in reference [5] is extended. The proposed topology requires only one bidirectional switch.

Batteries, capacitors and isolated DC voltage supplies can be used as DC voltage sources in the proposed topology [6]. When ac voltage sources are available using rectifiers and isolated transformers multiple DC voltage sources can be produced [7]. The problem of voltage balancing is eliminated by employing fixed DC voltage source [8].

2. CASCADE H BRIDGE MULTI-LEVEL INVERTER TOPOLOGY

In the family of Multi level inverter conventional cascaded multi-level inverter is the most influencing topology [9]. The cascade H bridge topology allows several DC voltage sources to synthesize a desired output voltage, it requires least number of components as compared to diode clamped and flying capacitor multi level inverters and no specially designed transformer is needed as compared to multi pulse inverter [10]. A cascade multi level inverter consists of number of H bridge inverter units with separate DC voltage sources for each unit. The full bridge topology shown in Figure 1 is used to synthesize ac output voltage of three unique voltages ($+V_{dc}$, $-V_{dc}$ and zero) by connecting DC voltage source by different combinations of the four switches S_{11}, S_{12}, S_{13} and S_{14}. The overall output voltage is given by:

$$V_0 = V_{dc1} + V_{dc2} + \ldots\ldots + V_{dcn} \quad (1)$$

In Figure 1 if all the voltage sources are equal then the inverter is referred as symmetrical ($V_{dc1} = V_{dc2} = V_{dcn}$) otherwise known as asymmetrical ($V_{dc1} \neq V_{dc2} \neq V_{dcn}$) cascaded multi-level inverter.

2. 1. Symmetrical Cascaded Multi-level Inverter

The number of output voltage steps (Nsteps) for "m" number of separate DC voltage sources (batteries or PV cells) in symmetrical cascaded MLI is given as:

$$Nstep = 2 \times m + 1 \quad (2)$$

For m = 1; 3steps , m = 2; 5steps. The maximum output voltage produced with 'm' number of DC voltage sources in symmetrical cascaded multi level inverter is equal to $m*V_{dc}$.

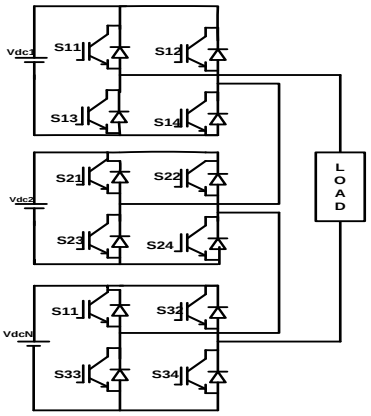


Figure 1. Conventional cascaded multi-level inverter

2. 2. Asymmetric Cascaded Multi level Inverter

For asymmetric cascaded MLI, the magnitudes of the DC voltage sources of different cells are not equal. Asymmetrical cascaded H Bridge MLI produces more output voltage levels than it's symmetric with equal number of cells.

If the separate DC voltage sources shown in Figure 1 are chosen according to a geometric progression with the factor of 2 or 3.

For "n" cascaded H Bridge MLI the number of voltage steps in asymmetrical cascaded H Bridge MLI is given as:

$$Nstep = 2^{m+1} - 1 \quad if\ Vj = 2^{j-1}Vdc \quad for\ j = 1,2,...m \quad (3)$$

$$Nstep = 3^{m+1} - 1 \quad if\ Vj = 3^{j-1}Vdc \quad for\ j = 1,2,...m \quad (4)$$

The maximum output voltages of these 'm' cascaded multi-level inverters are:

$$Vo\max = (2^m - 1)Vdc \quad if\ Vj = 2^{j-1}Vdc\ for\ j = 1,2,3..m \quad (5)$$

$$Vo\max = \left(\frac{3^m - 1}{2}\right)Vdc\ if\ Vj = 3^{j-1}Vdc\ for\ j = 1,2,3..m \quad (6)$$

Comparing Equations (2)–(6) it can be observed that asymmetrical cascaded H Bridge multi level inverters can produce more output voltage steps and higher maximum output voltage with the same number of bridges.

3. BASIC TOPOLOGY

The recommended basic structure in reference [11] shown in Figure 2 consists of three power switches Sa1, Sb1, Sc1 and two DC voltage sources and every switch is composed with an IGBT with anti parallel diode. When switch sc1 is ON the output voltageV0=V1, when switch Sb1 is ON the output voltage V0=V2, when Sa1

is ON the output voltage Vo=V1+V2 and when Sb1 and Sc1 is ON, V1 and V2 are connected in parallel, therefore the output voltage Vo=V1-V2. If V1≠V2 due to short circuit of DC voltage sources, huge amounts of circulating current will be circulated. To avoid this, the DC voltage sources magnitudes should be identical (V1=V2). Care must be taken when sa1 is conducting Sb1 or Sc1 should not turn ON vice versa.

In Figure 3, the switching devices should be selected carefully since the voltage across each switch is selected differently. The voltages across switches Sa1-San-1, Sb1- Sbn-1 and Scn-Scn-1 during their OFF state are VSa1-VSan-1, VSbn-VSbn-1 and VSc1-VScn-1 respectively, which satisfy:

VSa1 =VSa2=……VSan-1
VSb1 =VSb2=……VSbn-1
VSc1 =VSc2=……VScn-1

These switches voltages will come to lesser and lesser comparing with the output voltage when number of steps are increased. The IGBTs and MOSFETs are sufficient for these switches because these switches are operated at twice the frequency of the reference waveform.

The Voltages of the switches in H Bridge during OFF state are Vs1-Vs4 which satisfy:

$$VS1 = VS2 = VS3 = VS4 = \sum_{k=1}^{m} Vk \quad (7)$$

The voltage of the above switches becomes approximately equal to the output voltage therefore, the switching frequency of these switches becomes equal with the reference waveform. Therefore, insulated Gate Bipolar transistors (IGBT) can be preferred for these switches.

4. PROPOSED TOPOLOGY

The basic cell of proposed topology [11] is modified to generate more output voltage steps with minimum switches, a new topology is proposed in this paper and is verified by implementing prototype hardware 7level asymmetrical topology. The proposed topology is shown in Figure 4. The topology is composed of two DC voltage sources V1 and V2 along with level generation circuit. Level generation circuit consists of high frequency switches and should withstand high switching frequency to produce required voltage levels. The H Bridge circuit, is responsible for the conversion of the polarity of the output voltage and is low frequency part operating at line frequency. Using basic cell positive voltages are generated shown in Figure 5 (a). S1, S2, S3 and S4 forms the H Bridge which gives both positive and negative pulses shown in Figure 5 (b).The proposed topology can be easily extended by connecting basic cells in series and connected across the H Bridge. A 16 level asymmetrical cascaded H Bridge is shown in Figure 6(a) of the proposed topology. A generalized topology is shown in Figure 6(b).

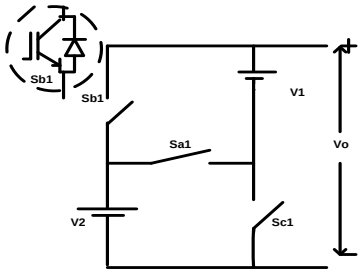


Figure 2. Basic Cell proposed in reference [11]

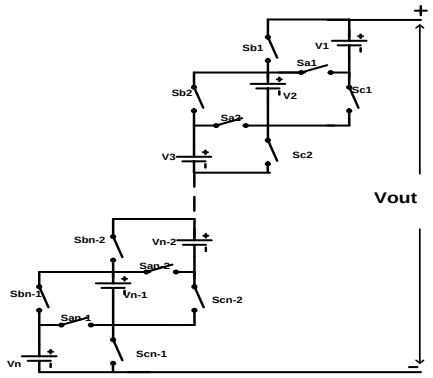


Figure 3. Extended Unit proposed in reference [11]

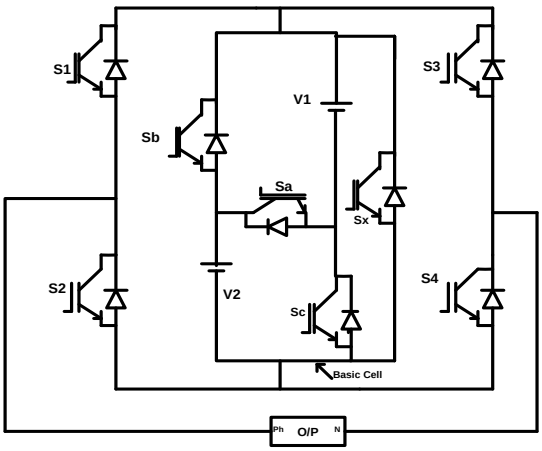


Figure 4. Proposed Topology

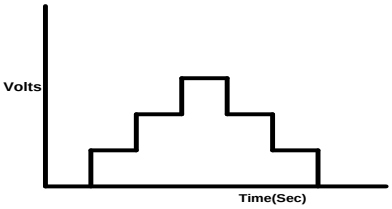


Figure 5(a). Basic Cell Output

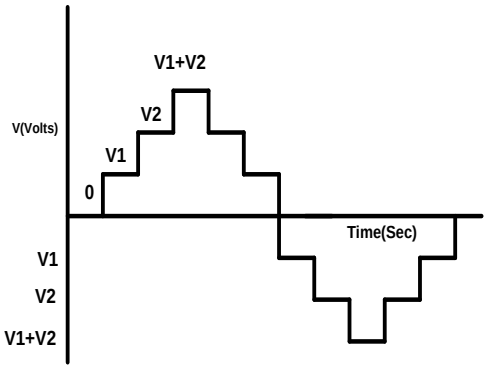


Figure 5(b). Output voltage waveform

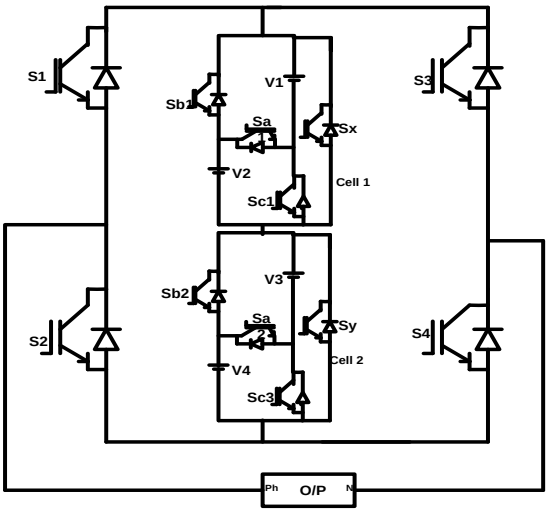


Figure 6(a). Proposed 16Level Asymmetrical Cascaded H Bridge MLI Topology

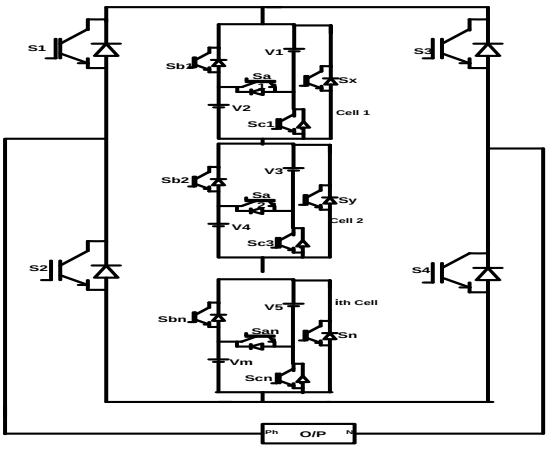


Figure 6(b). Generalized Topology of the proposed Cascaded Bridge MLI Topology

The values of the dc voltage sources employed in the asymmetrical MLI are assumed unequal in different cells such that maximum output voltage levels can be produced using less switching devices.

i). The magnitude of the DC voltage sources can be selected using the following equation, for the i_{th} cell, the value of the m_{th} DC voltage source:

$$Vdc\,m,i = 2^{(m-1)}Vdc \quad (8)$$

For cell 1 consisting of two voltage sources V_{dc1}&V_{dc2}:
ie i=1, m=1 ; $V_{dc1},1 = V_{dc}$
For i=1, m=2 ; $V_{dc2},1 = 2V_{dc}$
For cell 2contains V_{dc3} &$_{Vdc4}$
For i=2 , m=3 $V_{dc3},2= 2^2V_{dc}= 4V_{dc}$
For i=2 , m=4, $V_{dc4}= 2^3V_{dc}= 8V_{dc}$..

ii). For the i^{th} cell the output voltage levels (N_{level})can be determined by the following equation:

$$N\,level = 2^{2i} \quad ; \quad where'i'\ is\ \ cell\ \ number \quad (9)$$

For i=1 ; 2^2 =4 levels
i=2 ; 2^4=16 levels
i=3 ; 2^6=64 levels..

iii). The total number of IGBTs (N_{IGBT}) required is calculated using the following equation:

$$N_{IGBT} = 4i + 4; \quad (10)$$

For i=1; 4+4=8 IGBTs
i=2; 4*2+4=12
i=3; 4*3+4=16,

iv). The maximum output voltage is obtained by the i^{th} cell of the proposed topology and can be determined as follows;

$$The\ \ Maxmum\ \ Output\ \ Voltage\ \ Vo\max = (2^{2i} - 1)Vdc \quad (11)$$

For cell 1 i.e. i=1; 3Vdc
i=2; 15Vdc
i=3; 63Vdc.

Switching states of the proposed 7 level asymmetrical cascaded MLI is shown in Table 1.

5. MODULATION METHODS

Many modulation strategies are possible for multi-level inverters. Phase disposition (PD) PWM technique is employed for generating switching pulses. This technique is derived from the triangular carrier that has individually the lowest switching frequency among the multi-level PWM method and it provides low harmonic distortion and can be easily extended to any level.

TABLE 1. Output Voltages and Switching Sequence of the Proposed 7 Level Inverter

Level	0	1	2	3
Switching sequence	Sx	Sc	Sb	Sa
Output Voltage	0	V1	V2	V1+V3

5. 1. Phase Disposition (PD) PWM Method To generate switching pulses Phase Disposition PWM technique is used and developed Simulink model by incorporating topologies with reduced device count techniques.

In phase disposition (PD) pulse width modulation technique all carriers are arranged in phase. Figure 8 illustrates reference and carrier wave forms for the 7 level asymmetrical cascaded H bridge of the proposed topology. Phase disposition modulation has lowest line to line harmonic voltages [12]. Phase disposition modulation places significant harmonic energy into a carrier component in each phase leg and then relies on common mode cancellations between the phase legs to eliminate this harmonics from the line to line output voltage. Figure 8 shows carrier and reference wave arrangements in PD modulation technique. Switching pulses generated using Simulink is shown in Figure 9.

6. COMPARISON OF OTHER TOPOLOGIES WITH THE PROPOSED TOPOLOGIES

To investigate the performance analysis, it is also compared with other different multi-level inverter topologies compared in reference [10] and shown in Figure 7. The number of switches used in generating voltage levels plays a vital role in determining the complexity, cost of the multi-level inverter, and efficiency. A comparison is made on the basis of number of switches used against output voltage levels produced.

It is shown in Figure 10 that the topologies compared in reference [10] have almost equal number of switches but they produce unequal number of voltage steps. This is due to their arrangement of dc voltage sources and are considered only in series. However, in some topologies both series and parallel connections are also considered. In the proposed generalized topology the basic cell is connected to generate more output voltage levels by connecting DC voltage sources in series with all its possible combinations.

7. SIMULATION RESULTS

To conform and validate the effectiveness of the proposed topology, simulation has been carried out using matlab/simulink. Phase disposition (PD) Pulse width modulation techniques is employed for switching pulse generations with carrier frequency of 5KHz and 10KHz, where as reference, signal frequency is kept at 50Hz. The proposed topology is simulated using matlab/simulink by constructing 7-level asymmetrical topology. The simulated output voltage and current waveforms are shown in Figures 11 and 12. Fast Fourier Transform (FFT) analysis of the voltage and current waveforms of the proposed topology are shown in Figures 11(a) and 12(a). It was observed that the total harmonic distortion for the voltage is 21% and for the current waveform is 3.41%.

8. EXPERIMENTAL RESULTS

To approve and ensure the concept and feasibility of the proposed topology an experimental setup has been

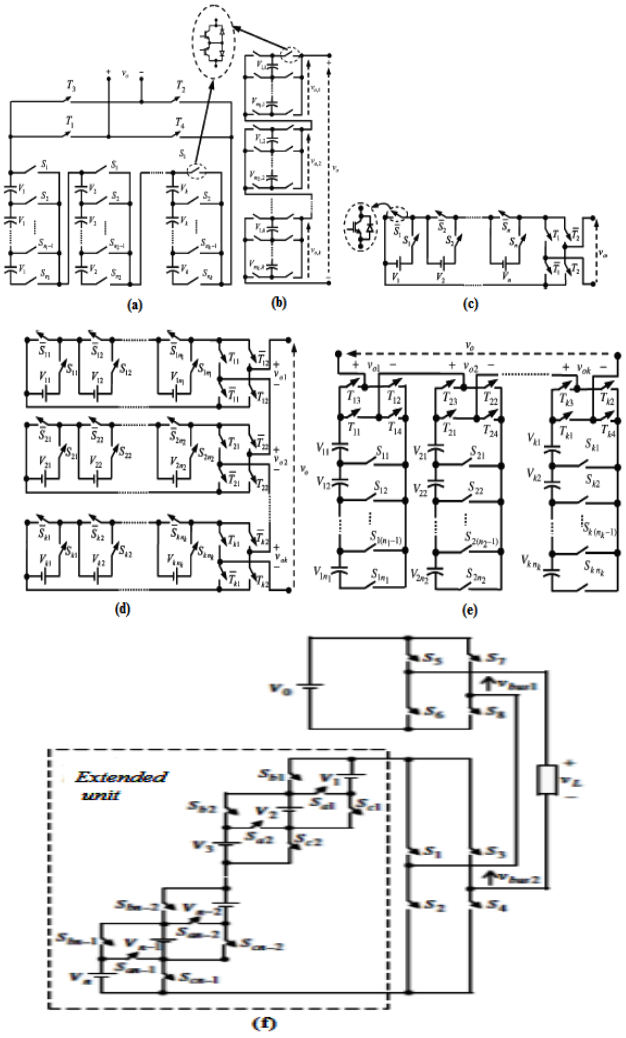


Figure 7. Various Topologies Compared in reference [10].

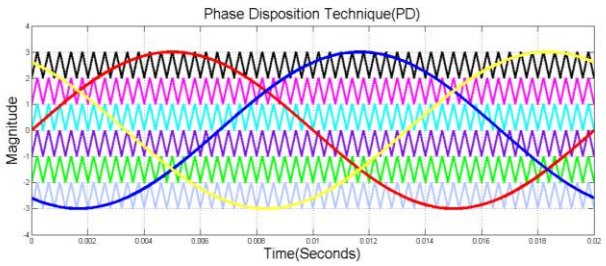


Figure 8. Carriers arrangement in phase Disposition PWM

prepared for 7-levels of output voltage and validated experimentally with R-L load (R=50Ω and L=55mH) shown in Figure 13. Switching pulses for H Bridge (S1 & S4) are shown in Figure 14. For high frequency switches (Sa, Sb, Sc &Sx) they are generated using Phase Disposition (PD) and are shown in Figure 15.

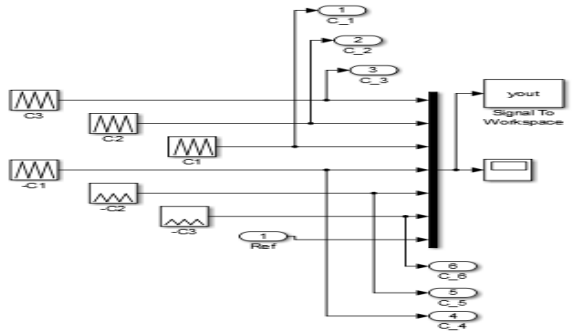


Figure 9. Simulation circuit for generating Switching pulses

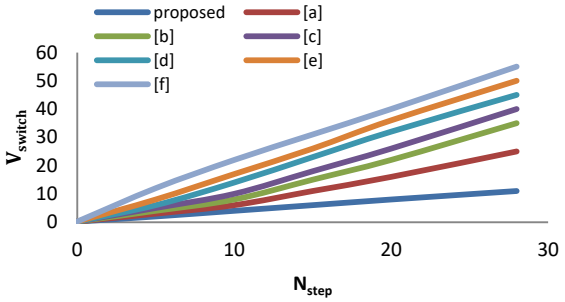


Figure 10. Copmarision of Switches against output voltage steps of proposed topology with topologies compared in reference [10] and shown in Figure 7

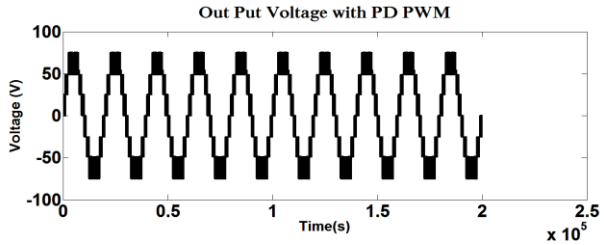


Figure 11. Output voltage with PD PWM

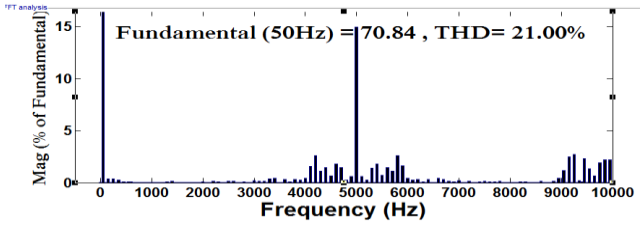


Figure 11(a). Voltage Total Harmonic Distortion (THD) with PDPWM

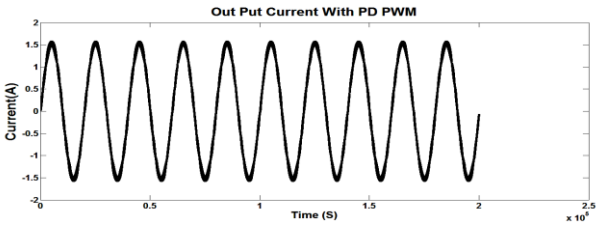


Figure 12. Output Current with PDPWM

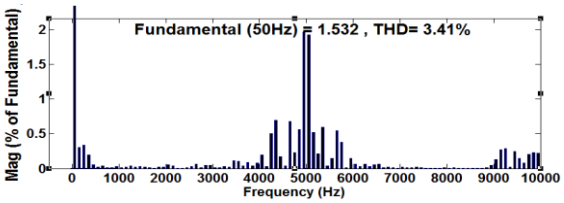
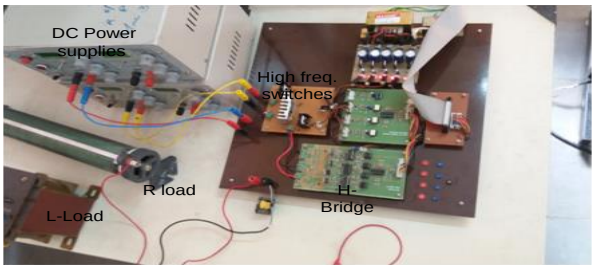


Figure 12(a). Current Total Harmonic Distortion with PD PWM



Hardware implementation of proposed 7level asymmetric MLI

Figure 13. Experimental setup for the 7level asymmetrical Cascaded H Bridge MLI of the proposed topology

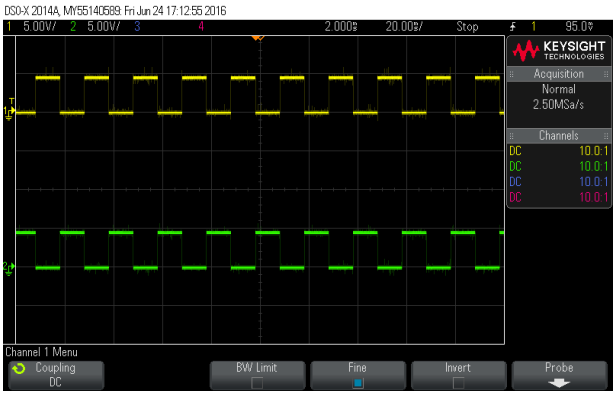


Figure 14. Switching Pulses for S1 and S4

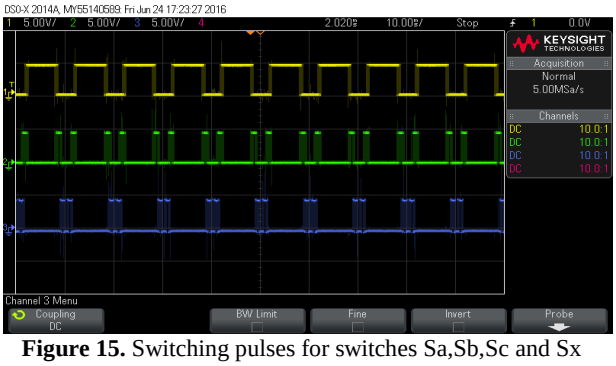


Figure 15. Switching pulses for switches Sa,Sb,Sc and Sx

An IRF840 MOSFETS, FIO5012 Bidirectional IGBT is used for high frequency switching, IRF840 MOSFETS for H-Bridge is used for low frequency switching, IR2110 ICs are used in Driver circuit, 4584 ICs for NOT gates and 4081 ICs for AND gates are used for Boolean operations, 6N137,TLP250 Opto isolators are used .7815, 7805 regulator ICs are used for 15Volts and 5Volts supply, SPARTRAN 3A DSP trainer is used for driving the gate signals.

The experimentally obtained voltage and current waveforms for the proposed 7-level asymmetrical topology using PD modulation, are shown in Figures 16, 17 and 18. It was observed that simulated and experimentally obtained results are matching with each other. Both simulation and experimental total harmonic distortion (THD) of the propposed topology are shown in Table 2. The adavantages and limitations of the proposed topology is also listed in Table 3.

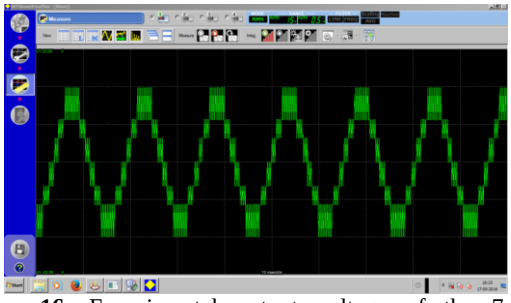


Figure 16. Experimental output voltage of the 7-level cascaded H Bridge MLI of proposed topology

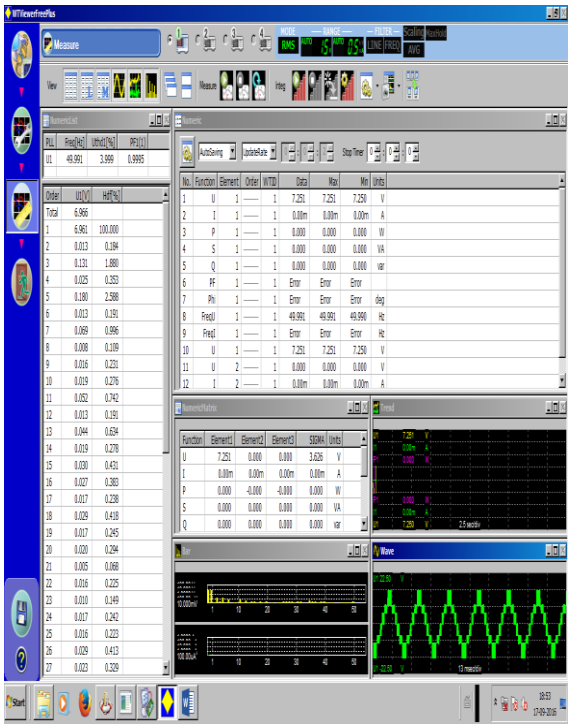


Figure 17. Experimental output voltage of the 7-level cascaded H Bridge MLI of proposed topology THD

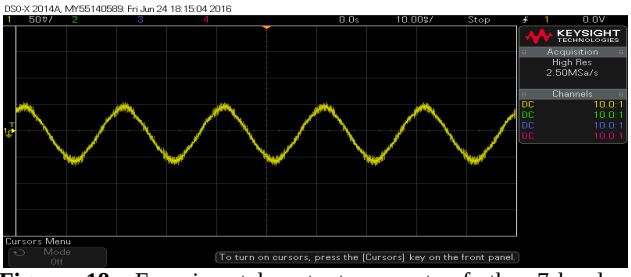


Figure 18. Experimental output current of the 7-level cascaded H Bridge MLI of proposed topology

TABLE 2. Comparison of Total Harmonic Distortion

	SIMULATION	EXPERIMENT
Voltage THD	21%	3.99%
Current THD	3.41%	4.2%

TABLE 3. Advantages and Limitations of the proposed Topology

Advantages	Limitations
1.Input dc voltage sources can be connected in either series or parallel	At fundamental switching frequency high voltage rated switches cannot be operated.
2.Equal load sharing is possible among all input dc voltage sources	Trinary source configuration is not possible
3.Use of binary source configuration is possible	

9. CONCLUSION

In this paper a new structure for the improvement of the cascaded H bridge multilevel inverter presented, that operates on the basis of the series and parallel connections of the dc voltage sources was presented. In the proposed topology the series connection of the basic cell and capability of the series connection of the dc voltage sources increases the number of voltage levels. The ability of the proposed topology was tested by simulation and experimental work of a 7level inverter based on the proposed topology.

10. ACKNOWLEDGMENTS

We thank the University Grants Commission (UGC), New Delhi for providing the Major Research Project to Dr. P. Satishkumar to carry out the research in the area of Cascaded multi-level inverters. We also thank the Principal and Head of the department, University College of Engineering, Osmania University for their encouragement and support and permitted us to utilize equipment.

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A Novel Generalized Topology for Multi-level Inverter with Switched Series-parallel DC Sources

RESEARCH NOTE

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چکیده

این مقاله توپولوژی نوینی از یک اینورتر چند طبقه تک فاز برای کاربرد های توان کم و زیاد را ارائه می دهد که از یک مدار تولید کننده پلاریته و پل H تشکیل شده است. توپولوژی ارائه شده می تواند با اتصال سری و موازی منابع ولتاژ DC سطوح ولتاژ بالاترا ایجاد کند. این توپولوژی کمترین تعداد افزاره های الکترونیک قدرت را بکار می گیرد که به کاهش هزینه، اندازه و وزن کمک می کند، توان کمی مصرف می کند و بنابراین راندمان مبدل را بهبود می بخشد. پالس های سوئیچینگ با استفاده از روش مدوله سازی پهنای پالس PD ایجاد می شود. سر انجام موثر بودن توپولوژی ارائه شده با ابزار نرم افزار MATLAB/SIMULINK درستی سنجی شده است.نمونه سخت افزاری اینورتر۷طبقهنا متقارن آماده شده تاتائیر و اعتبار توپولوژی ارائه شده را پشتیبانی کند.

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