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Improving Linearity of CMOS Variable-gain Amplifier Using Third-order Intermodulation Cancellation Mechanism and Intermodulation Distortion Sinking Techniques

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A B S T R A C T

This paper presents an improved linearity variable-gain amplifier (VGA) in 0.18-µm CMOS technology. The linearity improvement is resulted from employing a new combinational technique, which utilizes third-order-intermodulation (IM3) cancellation mechanism using second-order-intermodulation (IM2) injection, and intermodulation distortion (IMD) sinking techniques. The proposed VGA gain cell consists of a variable-gain attenuator followed by a differential cascode amplifier as a fixed-gain stage. The continuous gain control mechanism in the first stage occurs by varying the gate voltage of an nMOS transistor. Our proposed linearization technique is applied to the fixed gain cascode amplifier of the second stage. To examine the linearity of the proposed circuit, a nonlinear analysis of the cascode amplifier based on Taylor series has been performed. The simulation results show that after linearization, the third-order input intercept point (IIP_3) of the whole VGA has been improved about +18 dB at the gain of 15.4 dB. The VGA has a voltage gain varying from -7.5 to 19.5 dB and a bandwidth of 830 MHz to 845 MHz. Morever, the circuit dissipates 4.65 mW to 9.35 mW from a 1.8 V single supply over the entire gain range.

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1. INTRODUCTION

Variable-gain amplifier (VGA) is an essential sub-system in receivers which maximizes the whole dynamic range and is used in many applications such as disk drives [1] and wireless communication links [2]. In a modern communication receiver, a VGA usually precedes an analog-to-digital converter (ADC) to adapt the loss variation of the transmission channel and in turn ease the dynamic range requirement of the ADC [2].

A VGA must keep two main characteristics simultaneously; a controllable gain and a good linearity. However, many of recently reported VGAs have poor linearity. In a high-speed programmable gain amplifier (PGA) designed using variable MOS transconductors in disk drive applications, the linearity is limited by nonlinear characteristics of the transconductors [1, 3]. One of the main challenges of a g_m-ratioed VGA which its gain is controlled by the g_m ratio of the input to load stages, comes from the load stage distortion which significantly affects output linearity over the entire gain range [4, 5]. The linearization in resistive source degeneration technique improves the system linearity, however, increases noise and power dissipation [6]. Also, VGAs with poor linearity can be seen in other works [7-9].

Using cascode amplifier topology in VGAs, due to its advantageous properties over the common-source amplifier, results better high-frequency operation and wider dynamic range [10-13]. Elwan et al. [14] have used a cascode structure in a VGA and reported its superiorities over common-source amplifier but the linearity is still unpleasant.

Recently, Yeh et al. [15] has proposed an improved linearity cascode VGA. In this paper, we are going to propose a VGA based on the cascode topology with a

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larger voltage-gain and a much better linearity. The proposed VGA consists of a variable-gain attenuator followed by a fixed gain cascode amplifier. The gain variation mechanism is realized via controlling the gate bias voltage of the nMOS transistor in the first stage. In order to improve the VGA's linearity, we have combined two techniques simultaneously: one is injecting an IM2 signal to the common-source node [16] of the cascode amplifier and second is sinking the same amplifier's output current [17]. By tuning some parameters, our novel technique has significantly lowered the IM3 component of the output current which leads to increasing the IIP_3 of the whole VGA. Furthermore, to examine the performance of the circuit, a nonlinear analysis based on Taylor series has been conducted on the cascode amplifier. Simulations verify excellent linearity improvement and larger gain dynamic range. Because of the superior linearity, the proposed VGA best suits the applications requiring high linearity such as direct conversion receiver (DCR). The rest of the paper is organized as follows. Section 2, provides the proposed linearized VGA (L-VGA) design and analysis. Section 3, shows the simulation results and finally, conclusions are presented in Section 4.

2. PROPOSED LINEARIZED VGA DESIGN AND ANALYSIS

This section presents the proposed linearized VGA structure consisted of an attenuator stage followed by a fixed-gain stage, separately. Then, to investigate how the cancellation mechanism works, a nonlinear analysis of the circuit based on Taylor series theory is introduced.

2. 1. Attenuator Stage Circuit Design Figure 1 depicts the variable gain attenuator structure of the first stage. The attenuator topology is a source follower (M1, M2) with active load nMOS (M3, M4) biased in triode region. Simply, from the small signal low-frequency model of a source follower (neglecting body effect), the voltage gain of the circuit is given by [18]:

$$G_1 = \frac{\mu_n C_{ox}(\frac{W}{L})_{1,2}\left(V_{cont} - (V_o + V_{Th})\right)}{\mu_n C_{ox}(\frac{W}{L})_{1,2}\left(V_{cont} - (V_o + V_{Th})\right) + \frac{1}{r_{o1,2}} + \frac{1}{r_{o3,4}}} \quad (1)$$

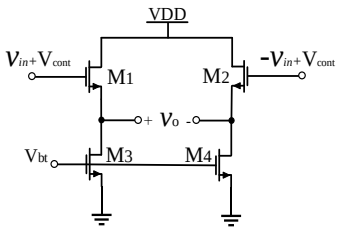

Figure 1. Schematic of the attenuator stage as a variable-gain cell

Equation (1) shows that the voltage gain of the attenuator can be varied by the control voltage V_{cont}.

2. 2. Fixed-gain Stage Circuit Design Figure 2 shows the fixed-gain differential cascode amplifier of the second stage. M1 and M2 are the input transconductor and M4 and M5 are the common-gate stages. M6 and M7 are pMOS active load current sources and M3 acts as the tail current source. In order to set a proper common-mode output voltage VCM, a DC level sensing pair along with a common-mode feedback (CMFB) circuit is used.

Considering the input-stage differential pair of the cascode amplifier shown in Figure 2, the time-varying drain current I_1 can be expressed as a function of the small-signal gate-source voltage (v_{gs}) around its bias point, appropriately chosen on the I-V charecteristics of device M1, using Taylor series expansion as:

$$i_{d1} = g_1\left(v_g - v_s\right) + g_1^{'}\left(v_g - v_s\right)^2 + g_1^{''}\left(v_g - v_s\right)^3 + \ldots \quad (2)$$

where g_1, $g_1^{'}$ and $g_1^{''}$ are the jth-order, (j = 1,2,3), transcenductance coefficients of input device respectively, given by [16]:

The third-order term in Equation (2) is the main contribution of IM3 components in the transconductor -stage. However, the multiplying term $-2g'_m v_g v_s$ in g'_m ($v_g - v_s$) also contributes to IM3 because v_s contains intrinsic IM_2 components [16]. Therefore, the linearization of the cascode amplifier is a significant consideration.

2. 3. Distortion Analysis of the VGA Topology With the Proposed Linearization Technique The complete linearized VGA structure is shown in Figure 3. The IM2 generator composed of M12 and M13, generates the IM2 current (i_x) which is then converted to the IM2 voltage (v_{IM2}) through resistor R_1. Here, M3 converts v_{IM2} to the current i_{IM2} and inject it to the v_s node.

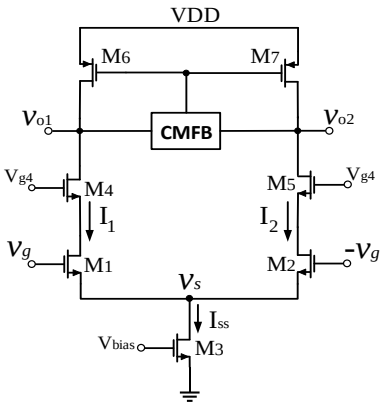

Figure 2. Schematic of the cascode amplifier of the second stage

An AC coupling network, formed by C and R_b, is inserted between the bias transistor and the squaring circuit to facilitate the DC bias of M3. The i_{IM2}, i_{d1} and i_{d2} come together which results in lower output IM3 cpmponents [16].

For further suppression of the output IM3 component in current i_o, we have used an additional diode-connected nMOS transistor Ma (as i_a injected into the v_1 node in Figure 3), as an IMD sinker [17].

Here, the source follower of the first stage is considered to be linear because of its low intermodulation distortion [19]. Thus, our analysis is focused on the cascode amplifier of Figure 3.

At the beginning, we define i_{IM2} as $2X \times v_{in}^2$ and $v_g = G_1.v_{in}$. The relation between differential output current i_o and input voltage v_{in}, in Figure 3, is a nonlinear differential equation which can be described as a Taylor series expansion as below:

$$i_o = C_1 v_{in} + C_3 v_{in}^3 + C_5 v_{in}^5 + \ldots \tag{4}$$

Differential circuits exhibit an odd-symmetric input/o-output characteristic [9]. It indicates that a differential circuit driven by a differential signal produces no even-order harmonics as expressed in Equation (4). In the equation above, C_1 is the first-order term of the output current that refers to the small signal gain. C_3 and C_5 are the third and fifth-order nonlinearity coefficients, respectively. For analyzing IM3 and IIP_3, our analysis is focused on C_3. Thus, the above polynominal is limited to the third-order term. By solving KCL equations (neglecting second order effects), the expression for i_{d1} is obtained as below [16]:

$$i_{d1} = \underbrace{(g_1 G_1)}_{A_1} v_{in} + \underbrace{(g_1' G_1^2 + X)}_{A_2} v_{in}^2 + \underbrace{\left((g_1'' - 2\frac{g_1'^2}{g_1})G_1^3 + 2XG_1\frac{g_1'}{g_1}\right)}_{A_3} v_{in}^3 \tag{5}$$

In Equation (5), A_1 is the small signal gain of the transconductor stage and A_2, A_3 are the nonlinear components in i_{d1}. The first terms in A_2 and A_3 are the intrinsic nonlinearities and the second ones are introduced by the new linearization technique.

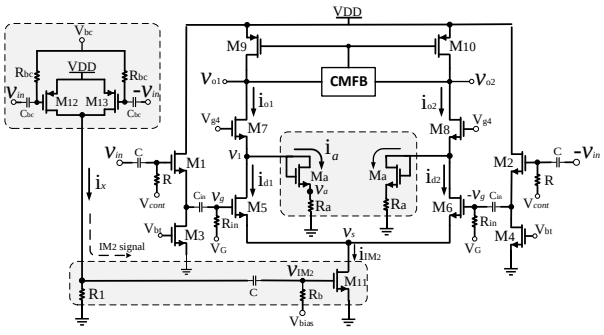

Figure 3. Circuit schematic of the proposed linearizaed VGA

$$g_1 = \frac{\partial I_{DS}}{\partial V_{GS}}\ ,\ g_1' = \frac{1}{2!}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2}\ ,\ g_1'' = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3} \tag{3}$$

To find i_a, we first approximate v_a with respect to v_1 with Taylor series expansion as follows [20]:

$$v_a \approx g_{1a} v_1 + g_{2a} v_1^2 + g_{3a} v_1^3 \tag{6}$$

Therefore, i_a is obtained through v_a / R_a:

$$i_a = \frac{v_a}{R_a} = \frac{g_{1a}}{R_a} v_1 + \frac{g_{2a}}{R_a} v_1^2 + \frac{g_{3a}}{R_a} v_1^3 \tag{7}$$

To have i_a as a function of v_{in}, we write $v_1 = Z_1 \times i_{d1}$ in which, Z_1 is the equivalent resistance of parallel paths diode-connection and common-gate. So, i_a would be given as:

$$\begin{aligned} i_a = &\underbrace{-\left(Z_1 A_1 \frac{g_{1a}}{R_a}\right)}_{\beta_1} v_{in} + \underbrace{\left(Z_1^2 A_1^2 \frac{g_{2a}}{R_a} - Z_1 \frac{g_{1a}}{R_a} A_2\right)}_{\beta_2} v_{in}^2 \\ &+ \underbrace{\left(2Z_1^2 A_1 A_2 \frac{g_{2a}}{R_a} - Z_1 A_3 \frac{g_{1a}}{R_a} - Z_1^3 A_1^3 \frac{g_{3a}}{R_a}\right)}_{\beta_3} v_{in}^3 \end{aligned} \tag{8}$$

As known, the sum of i_a and i_{d1} would be i_{o1} as follows:

$$i_{o1} = i_{d1} + i_a = (A_1 + \beta_1) v_{in} + (A_2 + \beta_2) v_{in}^2 + (A_3 + \beta_3) v_{in}^3 \tag{9}$$

i_{o2} would be the same as i_{o1} if v_{in} is replaced by $-v_{in}$. The injected IM2 current from M3, i_{IM2}, is found by [16]:

$$i_{IM2} = 2X \times v_{in}^2 = -2g_{12}' g_{m3} R_1 v_{in}^2 \tag{10}$$

From $i_o = i_{o1} - i_{o2}$ and Equation (4), C_1 and C_3 can be concluded (on the next page).

From Equations (11.a) and (11.b), the third-order input intercept point for the nonlinear output current can be expressed as below [21]:

$$IIP_3(\text{dBm}) = 10 \log_{10}\left(\sqrt{\frac{4}{3}\left|\frac{C_1}{C_3}\right|}\right) + 10 \text{ dB} \tag{12}$$

An interesting observation on Equation (12) is that by setting C_3 to zero the linearity of the VGA can be maximized. In Equation (11.b), it is observed that the proposed linearization technique has introduced the degrees of freedom which is able to cancel the third-order distortion terms. Therefore, it is apparent from Equation (11.b) that an appropriate choice of resistor and transistor sizes, leads to a lower C_3 and results a better IIP_3.

In order to predict the IIP_3 behavior, the theoretical values for IIP_3 as a function of tunable parameters such as resistors R_1 and R_a calculated by Equation (12) have been plotted in Figure 4.

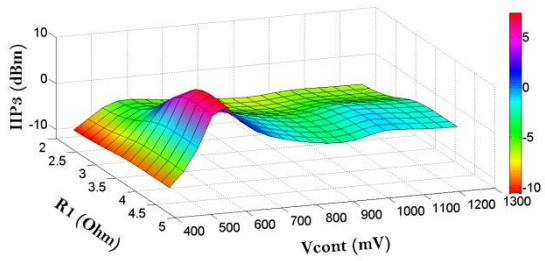

Figure 4. IIP_3 variations computed with Taylor series vs. V_{cont} and R_1

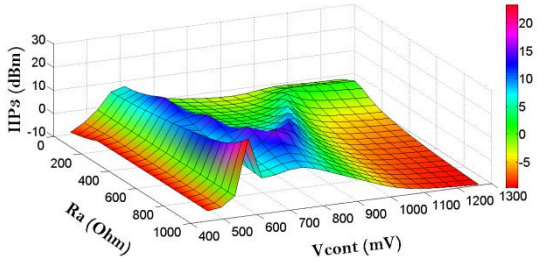

Figure 5. IIP_3 variations computed with Taylor series vs. V_{cont} and R_a

Figure 4(a) illustrates the IIP_3 behavior of the VGA as a function of control voltage and resistor R_1 for R_a = 0Ω. For different control voltages, The IIP_3 experiences its maximum values as R_1 increases. So, we choose R_1 = 4 KΩ as an optimal value.

The IIP_3 behavior of the VGA for R_1 = 4 KΩ as a function of control voltage and resistor R_a is shown in Figure 4(b). As R_a increases, the IIP_3 also increases at control voltages ranging from 600 to 900 mV, but it decreases at high gain modes (Vcont > 900mV). Here, we choose R_a = 200Ω as an optimal value by considering the low gain linearity importance and also drastic drop at high gain mode.

The theoretical values were obtained for a 100µm/0.18 µm aspect ratio for M4 and M5, 60µm/0.18 µm for M1 and M2 ,and 15µm/0.18 µm for the tail current source M3. The transistor sizing for the squaring circuit (or IM2 generator circuit) is chosen to be 9µm/0.18 µm. Finally, the size of Ma is considered to be 24µm/0.18µm.

3. SIMULATION RESULTS

Simulations using Advanced Design System (ADS) simulator was performed to validate the results of the Taylor analysis in Figure 4. The fully differential variable-gain amplifier, shown in Figure 3, has been simulated using 0.18µm CMOS TSMC model. The cascode biasing current was set to 1.94 mA, whereas the total current driven from the attenuator stage varied from 49 µA to 2.66 mA. The bias voltage for the squaring circuit, V_{bc}, and gate voltage of M1 and M2, V_{gate}, was set to 935 mV and 900 mV, respectively. The total current consumed by the squaring circuit is 456 µA. The IIP_3 variation as a function of control voltage considering the optimal values obtained from the theoretical calculations is illustrated in Figure 5.

The results were plotted before and after applying the linearization technique. As shown in Figure 5, before the linearization technique, the IIP_3 reaches its maximum value at the gain of 2.9 dB then decreases as control voltage increases.

In this case, the minimum and maximum values obtained for the IIP3 are -17.2 dBm and 4.4 dBm, respectively. The linearity of the VGA has improved using the proposed linearization technique as the IIP_3 curve shows one more peak at the gain of 14 dB, as shown in Figure 5. The second peak, produced by the linearizer circuit, prevents the IIP_3 to decrease as fast as non-linearized VGA (NL-VGA) does. Therefore, it can be observed from Figure 5 that the new cancellation technique works so good leading to a significant IIP_3 improvement of +18 dB at the gain of 15.4 dB. Thus, the minimum and maximum values obtained for the IIP_3 is - 9.3 dBm and 8.5 dBm, respectively. As can be seen from Figure 5, by applying the proposed technique,

$$C_1 = 2G_1\left(g_1 - Z_1 g_1 \frac{g_{1a}}{R_a}\right) \quad (11\text{ a})$$

$$C_3 = 2G_1\left[\begin{array}{l}\left(g_1'' - 2\frac{g_1'^2}{g_1}\right)G_1^2 - Z_1\frac{g_{1a}}{R_a}\left(g_1'' - 2\frac{g_1'^2}{g_1}\right)G_1^2 + \frac{2g_{12}' g_{m3}R_1}{g_1}\left(Z_1\frac{g_{1a}}{R_a} - 1\right)\\ +2Z_1^2 g_1\frac{g_{2a}}{R_a}\left(g_1' G_1^2 - g_{12}' g_{m3}R_1\right) - Z_1^3 g_1^3 G_1^2\frac{g_{3a}}{R_a}\end{array}\right] \quad (11\text{ b})$$

the results have been plotted before and after applying the linearization technique. As shown in Figure 6, before the linearization technique, the IIP_3 reaches its maximum value at the gain of 2.9 dB then decreases as control voltage increases.

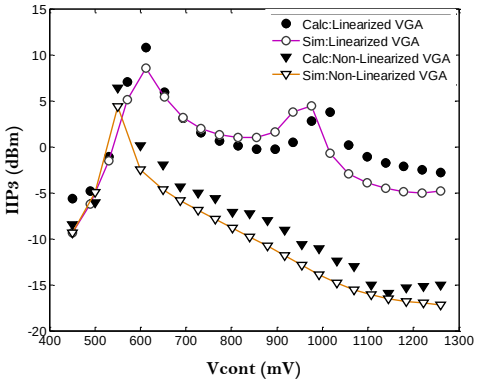

Figure 6. Comparison of calculated and simulated IIP3 before and after applying the linearization technique versus control voltage

In this case, the minimum and maximum values obtained for the IIP3 are -17.2 dBm and 4.4 dBm, respectively. The linearity of the VGA has improved using the proposed linearization technique as the IIP_3 curve shows one more peak at the gain of 15.4 dB, as shown in Figure 5. The second peak, produced by the linearizer circuit, prevents the IIP_3 to decrease as fast as non-linearized VGA (NL-VGA) does. Therefore, it is obvious from Figure 5 that the new cancellation technique worked so good leading to a significant IIP_3 improvement of +18 dB at the gain of 15.4 dB. Thus, the minimum and maximum values obtained for the IIP_3 is - 9.3 dBm and 8.5 dBm, respectively. As can be seen from Figure 5, by applying the proposed technique, input linearity of the VGA has improved very well and a good agreement with Figure 4(b) is also evident.

Figure 7 shows the frequency response obtained from the simulation with control voltage ranging from 0.45 V to 1.26 V. The upper 3-dB bandwidth is 830 MHz and 845 MHz at high gain and low gain modes, respectively. A high-pass filter with a low cut off frequency would be enough to block the DC offsets from preceding stages and provide a correct bias for the cascode stage. As it can be seen from Figure 6, there is a BW variations of about 15 MHz over the entire gain range.

Figure 8 illustrates the VGA voltage gain over different control voltages obtained from the simulation. By applying the linearization technique, the gain of the VGA does not change at all, therefore the dynamic range remains constant. The VGA achieves a gain range from -7.5 to 19.5 dB.

Figure 9 illustrates the total power dissipation of the VGA for different gain control voltages. The power dissipation of the linearized and non-linearized VGA are shown with solid and dashed lines, respectively. As it can be seen from Figure 8, there is a slight difference between these two curves which is about 0.15 mW.

To compare the VGA's efficiency before and after linearization, a figure of merit (FoM) based on linearity, bandwidth, voltage gain, noise and power consumption is defined as:

$$FOM = \frac{IIP_3(mW) \times gain \times BW\ (MHz)}{P_{dc}(mW) \times (F-1) \times 1(MHz)} \quad (13)$$

where, F is the noise factor of the VGA.

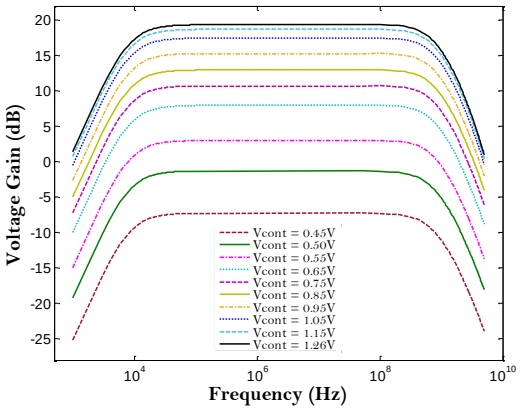

Figure 7. Simulated frequency response vs. various control voltages

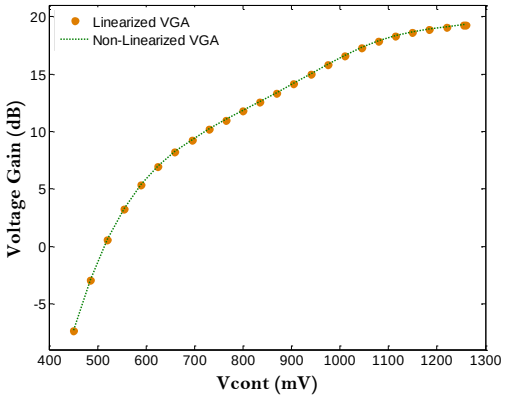

Figure 8. Simulated voltage gain over control voltage

TABLE 1. Performance summary and comparison

REF.	2009 [14]	2013 [15]	2011 [7]	2012 [8]	2013 [9]	2012 [5]	This work: NL-VGA	This work: L-VGA	Units
Process	65	90	180	180	180	180	**180**	**180**	**nm**
IIP3	-25*	-19~3	-4.5~0	-18*	-1.4~ -2.9#	N/A	**-17.2~4.4**	**-9.3~8.5**	**dBm**
BW	40	56~64**	1000~5000	0~5600	2~1900	76~809	**850~865**	**830~845**	**MHz**
Gain	-18~47	-18~22	-5~11	-16.5~6.5	-10.6~7.8	-37~28	**-7.5~19.5**	**-7.5~19.5**	**dB**
NF	N/A	4.8~18	3.2~7.2	16.5~27.1	21.4~27.1	22	**13~16**	**13~16**	**dB**
Power	2.23	26	10~19	7.9	12.2	3.1~5	**4.5~9.2**	**4.65~9.35**	**mW**
Supply	1.2	2	1.8	1.8	1.8	1.8	**1.8**	**1.8**	**V**
FOM_{max}	N/A	N/A	N/A	N/A	N/A	N/A	**1.1**^	**85**^	

* Reported values are for the maximum gain setting.
# Estimated from the input P1dB.
^ Values were calculated at 15.4 dB where the FOM is maximum.
** Reported value is in GHz.

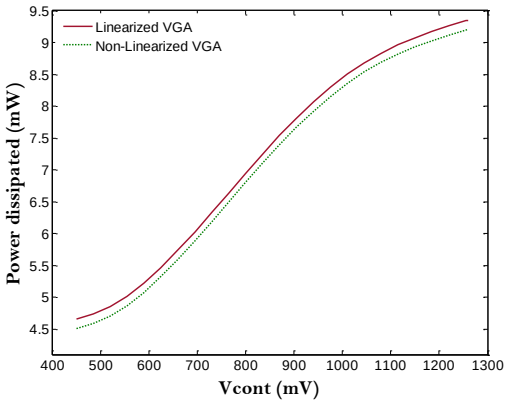

Figure 9. Total power dissipation across different control voltages

4. CONCLUSION

This paper developed a variable-gain amplifier with low IM3 components resulted from injecting low frequency IM2 and using the diode-connection transistors for sinking nonlinear components of output current. The proposed VGA was analyzed by Taylor series. Simulation results in 0.18µm TSMC CMOS technology demonstrated a maximum IIP_3 improvement of +18 dB at the gain of 15.4 dB. The excess power consumption is about 0.15 mW. The obtained bandwidth varies 15 MHz (830MHz to 845MHz) in the whole gain range. The achieved noise figure (NF) of the linearized VGA is between 13 to 16 dB at the entire gain range.

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Improving Linearity of CMOS Variable-gain Amplifier Using Third-order Intermodulation Cancellation Mechanism and Intermodulation Distortion Sinking Techniques

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چکیده

در این مقاله یک تقویت کننده‌ی بهره متغیر با خطسانی بهبود یافته در فناوری CMOS ۰/۱۸ میکرومتر ارائه شده است. بهبود خطسانی با ارائه یک شیوه ترکیبی جدید شامل تزریق مولفه مدولاسیون داخلی مرتبه دوم و جذب مولفه‌های مدولاسیون داخلی انجام گرفته است. سلول بهره در این تقویت کننده متشکل از یک طبقه تضعیف کننده ولتاژ با بهره متغیر و یک طبقه تقویت کننده کسکود تفاضلی با بهره ثابت می باشد. سازوکار کنترل پیوسته بهره در طبقه تضعیف کننده با تغییر ولتاژ گیت ترانزیستور n کانال ورودی صورت می پذیرد. در این مقاله، شیوه خطی‌سازی پیشنهادی جهت بهبود خطسانی مدار به تقویت کننده کسکود طبقه دوم اعمال شده است. جهت بررسی خطسانی و آزمون عملکرد مدار پیشنهادی، یک تحلیل غیرخطی بر اساس سری تیلور بر روی طبقه کسکود انجام گرفته است. نتایج حاصل از شبیه سازی این طرح نشان می‌دهد که پس از اعمال شیوه پیشنهادی به مدار، نقطه برخورد مرتبه سوم در ورودی تقویت کننده‌ی بهره متغیر به میزان ۱۸ دسیبل در بهره ولتاژ ۱۵/۴ دسیبل بهبود یافته است. بهره ولتاژ تقویت کننده از ۷/۵- تا ۱۹/۵ دسیبل با پهنای باند ۸۳۰ تا ۸۴۵ مگاهرتز بدست آمده است. همچنین، توان مصرفی کل مدار در حدود ۴,۵ تا ۹,۳۵ میلی وات از منبع تغذیه ۱/۸ ولتی می باشد.

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