International Journal of Engineering

Journal Homepage: www.ije.ir

# Phase Frequency Detector Using Transmission Gates for High Speed Applications

M. Gholami*

*Faculty of Engineering and Technology, University of Mazandaran, Babolsar, Iran*

*PAPER INFO*

*Paper history:*
Received 13 May 2016
Received in revised form 27 May 2016
Accepted 02 June 2016

*Keywords*:
Phase-frequency Detectors
Phase Detector
Delay Locked Loop
Phase locked Loop
Transmission Gate
Transceiver

*ABSTRACT*

In this paper a new phase-frequency detector is proposed using transmission gates which can detect phase difference less than 500ps. In other word, the proposed Phase-frequency Detector (PFD) can work in frequencies higher than 1.7 GHz, whereas a conventional PFD operates at frequencies less than 1.1 GHz. This new architecture is designed in TSMC 0.13um CMOS Technology. Also, the proposed PFD achieves a capture range approximately twice that of conventional PFDs. The simulation results support the theoretical predictions. To validate correct performance of this novel PFD, it is then used in a conventional delay locked loop structure.

***doi***: *10.5829/idosi.ije.2016.29.07a.05*

## 1. INTRODUCTION

The Delay Locked Loop (DLL) and Phase locked Loop (PLL) have become important components for valid data transmission in high-speed interface systems, frequency synthesizers [1, 2], clock and data recovery [3] and clock skewing circuits [4]. Hence, PLLs and DLLs are main blocks in transceivers architecture. As the speed of electrical systems is increasing, DLLs and PLLs with higher operating frequencies are needed. It is required in DLLs and PLLs to compare phase difference of input and output of DLLs or PLLs. Phase-Frequency Detectors (PFDs) are used to minimize this phase differences. Hence, one of the main building blocks in both PLLs and DLLs architecture is PFD [5].

There are some limitations in conventional PFDs which may result to lower speed, accuracy and frequency capture range of PLLs or DLLs [6, 7]. Therefore, designing a new PFD which can help to conquer these problems will be of high importance. Transmission gates (TG) have the ability to transfer the data with higher speed rather than conventional switches. Therefore, in this paper a new TG based PFD is deigned to conquer the limitation of detecting phase offset in high speed applications.

*Corresponding Author's Email: m.gholami@umz.ac.ir (M. Gholami)

## 2. CONVENTIONAL PHASE-FREQUENCY DETECTOR

Figure 1 shows the conventional PFD architecture which is widely used in PLLs and DLLs [8, 9]. As can be seen in Figure 1, conventional PFD has two D-flip flop and one NAND gate. The D-flip flops are triggered with two inputs of PFD. In the other words, two inputs that their phase differences to be determined are connected to the clock of D-flip flops. Up and DN signals are generated by these two D-flip flops. These two signals switch the current of charge pump. Both signals are initially low. In the first rising edge of inputs, the corresponding D-flip flop's output will be high. The state is held until the rising edge of the other input arrives. At this time, the reset pass will be activated and both UP and DN will be equal to zero. The related waveforms for conventional DLL are shown in Figure 2.

Also, the gate level implementation of this conventional PFD with NAND-based latches which is reported elsewhere [10] is shown in Figure 3. As can be

Please cite this article as: M. Gholami, Phase Frequency Detector Using Transmission Gates for High Speed Applications, International Journal of Engineering (IJE), TRANSACTIONS A: Basics Vol. 29, No. 7, (July 2016) 916-920

seen in this figure, the reset path contains 3 two inputs, one 3 inputs and one 4 inputs NAND gates.

To have higher speed PFD we need to minimize the reset path delay. In the other words, the number of gates should be decreased in reset path line. Another problem of this conventional PFD is its blind zone which increases the phase noise (in other words jitter) of DLLs or PLLs. Therefore, in this paper a new TG based PFD is deigned to conquer the limitation of detecting phase offset in high speed applications. Use of transmission gates will increase the speed of data transmission and also by decreasing reset path delay we can design higher speed PFD which will be introduced in next section.

## 3. PROPOSED TRANSMISSION GATE PHASE-FREQUENCY DETECTOR

The proposed transmission gate based PFD is shown in Figure 4. This circuit is divided into three sections. When A='0' in section I, the $TG_1$ is ON and $TG_2$ is OFF and $V_{DD}$ is transferred to $V_1$. In rising edge of A, $TG_1$ is OFF, $TG_2$ is ON and $V_1=V_{DD}$ will be kept in loop containing $TG_2$ and two inverters. Also, in the rising edge of A, $TG_3$ will be activated and $V_1=V_{DD}$ is transferred to UP. This means that section I is a circuit which can act as a D-flip flop with input of D='1'. This procedure similarly happens to Section II for input B.

Section III is a control circuit. This circuit will be activated when both UP and DN signals are high. When UP or DN signals or both of them are low, this circuit will connect X node to Z and Y node to W. Hence, in this case both of the circuits will act as a D-flip flop. When UP and DN signals are high, the control circuit (section III) will send zero to Z and W nodes (in other words the second loop in sections I and II will be opened). This results to UP='0' and DN='0'.

As the proposed circuit just contains three inverters and one two inputs NAND gate in the reset path, it has better speed rather than conventional PFD. Using delays in NAND gate in section III, result to lower reset path and higher speed of proposed PFD [6].

## 4. SIMULATIONS AND RESULTS

The proposed TG based PFD is designed in TSMC 0.13 um CMOS technology. The results for frequency of 1.7 GHz when phase difference is less than $\pi$ are shown in Figure 5, which proves the correct operation of the TG based PFD. Also, the results when the phase difference is more than $-\pi$ is shown in Figure 6. These figures prove that the capture range of the proposed TG based PFD is between $-2\pi$ and $2\pi$. In both of figures the proposed PFD calculates the phase differences of two inputs A and B. Depending on A leads B or B leads A, there will be pulses at outputs UP or DN. Also Figure 7 and Figure 8 show the reset time and blind zone time of proposed PFD which is acceptable in comparison with other works.

In addition, to validate the correct working of proposed PFD, it is used in DLL-based frequency synthesizer architecture. All building blocks of DLL is like what reported in the literature [2] except conventional PFD which is replaced with proposed TG based PFD. Figure 9 shows the locking process of DLL-based frequency synthesizer using proposed TG based PFD. This figure can show correct working of proposed PFD. It should be mentioned that this DLL is designed in CMOS Technology and for frequency of 400 MHz. A comparison between proposed architecture and some related works is shown in Table 1. In addition, Table 2 shows the variation of proposed phae frequency detector at different frequencies.

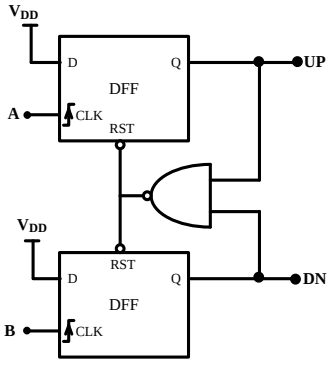


**Figure 1.** Conventional PFD [7]

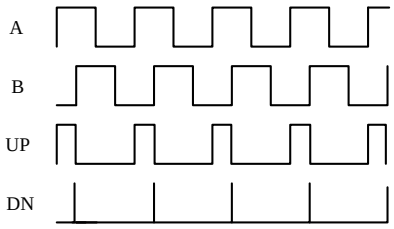


**Figure 2.** Waveforms related to conventional PFDs

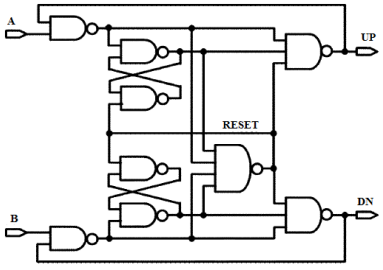


**Figure 3.** Gate level implementation of conventional PFDs [10]

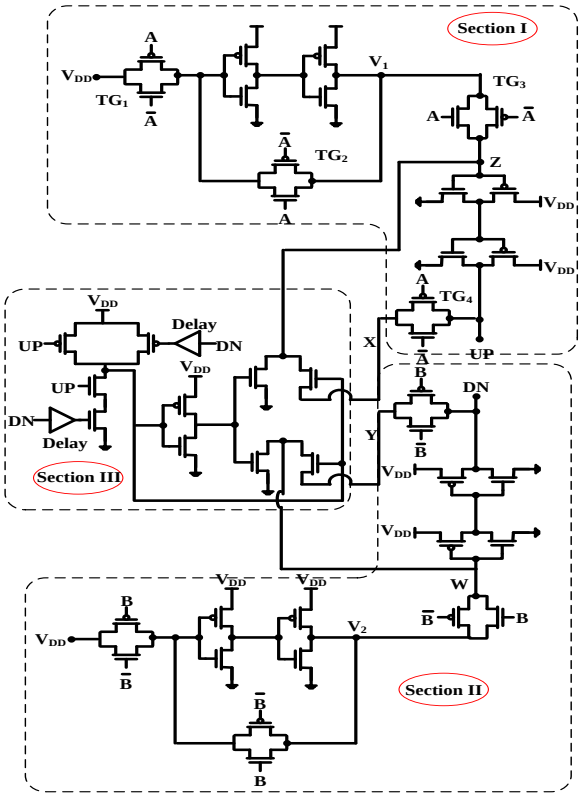


**Figure 4.** Proposed TG-based PFD

**TABLE 1.** Performance comparison

| Parameters | [11] | Conventional PFD [12] | [13 | This work |
|---|---|---|---|---|
| Technology | 0.13µm | 0.13µm | 0.13µm | 0.13µm |
| Supply voltage (V) | 1.2 | 1.2 | 1.2 | 1.2 |
| Power consumption @100MHz(µW) | 310 | 320 | 420 | 300 |
| Reset path Delay (ps) | 210 | 162 | 170 | 150 |
| Blind Zone Time (ps) | 10 | 120 | 250 | 140 |
| Maximum operating frequency | 1.6 | 1.1 | 2.2 | 1.7 |

**TABLE 2.** Power consumption at different frequencies

| Frequency | Power consumption (mW) |
|---|---|
| 100 MHz | 0.3 |
| 500 MHz | 0.453 |
| 1 GHz | 0.792 |
| 1.5 GHz | 0.956 |
| 1.7 GHz | 0.11 |

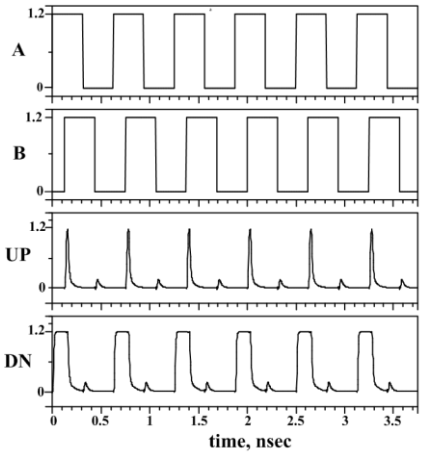


**Figure 5.** Waveforms of proposed high speed TG based PFD when DN is activated

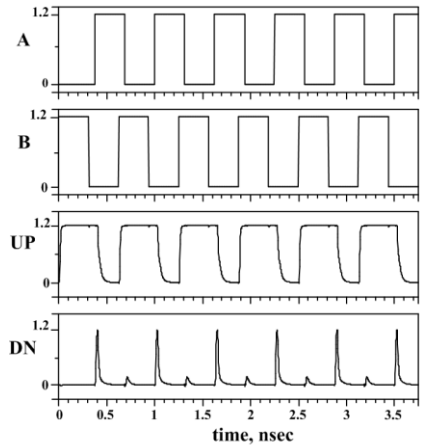


**Figure 6.** Waveforms of proposed high speed TG based PFD when UP is activated

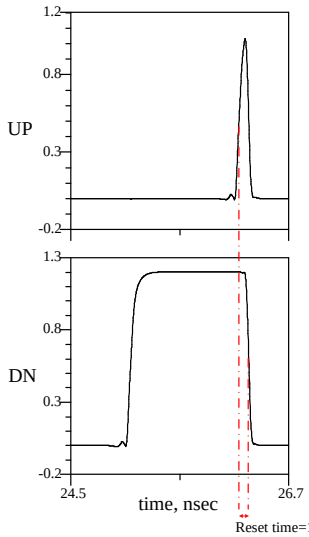


**Figure 7.** Reset time of proposed PFD

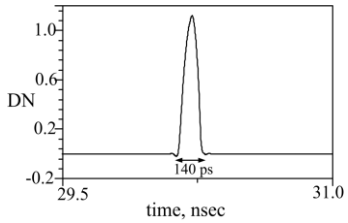


**Figure 8.** Blind zone time of proposed PFD

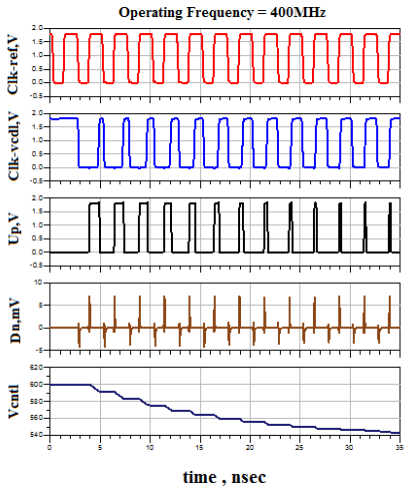


**Figure 9.** Waveforms of DLL with TG-based PFD to reach lock condition

## 4. CONCLUSIONS

In this paper a new phase-frequency detector is reported. The proposed phase-frequency detector is designed with transmission gates. This novel transmission gate based PFD is able to detect the phase differences less than 500 ps. In the other word, the proposed PFD can work in frequencies higher than 1.7 GHz, whereas a conventional PFD operates at frequencies less than 1.1GHz.

This new architecture is designed in TSMC 0.13 um CMOS Technology. In the proposed PFD, a capture range approximately twice of conventional PFDs has been achieved. To prove true working of proposed PFD, it is then used in DLL-based frequency synthesizer architecture. This DLL is designed in TCMS 0.18 um CMOS Technology. The simulation results confirm the theoretical predictions.

## 5. REFRENCES

1. Gholami, M. and Ardeshir, G., "Dual phase detector based delay locked loop for high speed applications", ***International Journal of Engineering-Transactions A: Basics***, Vol. 27, No. 4, (2014), 517-522.
2. Gholami, M., "A novel low power architecture for DLL-based frequency synthesizers", ***Circuits, Systems, and Signal Processing***, Vol. 32, No. 2, (2013), 781-801.
3. Rahimpour, H., Gholami, M., Ardeshir, G. and MiarNaimi, H., "Low settling time all digital DLL for VHF application", ***International Journal of Engineering-Transactions C: Aspects***, Vol. 28, No. 3, (2014), 419-425.
4. Chi, H.-J., Choi, Y.-H., Lee, S.-M., Sim, J.-Y., Park, H.-J., Lim, J.-J., Kang, P.-S., Lee, B.-Y., Hong, J.-C. and Lee, H.-S., "A 2-Gb/s intrapanel interface for TFT-LCD with a vsync-embedded subpixel clock and a cascaded deskew and multiphase DLL", ***Circuits and Systems II: Express Briefs, IEEE Transactions on***, Vol. 58, No. 10, (2011), 687-691.
5. Hoyos, S., Tsang, C. W., Vanderhaegen, J., Chiu, Y., Aibara, Y., Khorramabadi, H. and Nikolic, B., "A 15 MHz to 600 MHz, 20 mW, 0.38 mm split-control, fast coarse locking digital DLL in 0.13 m CMOS", ***Very Large Scale Integration (VLSI) Systems, IEEE Transactions on***, Vol. 20, No. 3, (2012), 564-568.
6. Gholami, M. and Ardeshir, G., "Analysis of DLL jitter due to voltage-controlled delay line", ***Circuits, Systems, and Signal Processing***, Vol. 32, No. 5, (2013), 2119-2135.
7. Gholami, M. and Ardeshir, G., "Jitter of delay-locked loops due to PFD", ***Very Large Scale Integration (VLSI) Systems, IEEE Transactions on***, Vol. 22, No. 10, (2014), 2176-2180.
8. Gholami, M., "Total jitter of delay-locked loops due to four main jitter sources", ***in IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, Vol. 24, No. 6, (2016), 2040-2049.
9. Gholami, M., Rahimpour, H., Ardeshir, G. and Miar-Naimi, H., "A new fast-lock, low-jitter, and all-digital frequency synthesizer for DVB-T receivers", ***International Journal of Circuit Theory and Applications***, Vol. 43, No. 5, (2015), 566-578.
10. Charles, C. T. and Allstot, D. J., "A calibrated phase/frequency detector for reference spur reduction in charge-pump PLLs", ***Circuits and Systems II: Express Briefs, IEEE Transactions on***, Vol. 53, No. 9, (2006), 822-826.
11. Park, K. and Park, I.-C., "Fast frequency acquisition phase frequency detectors with prediction-based edge blocking", in Circuits and Systems, ISCAS , IEEE International Symposium on, (2009), 1891-1894.
12. Ayat, M., Atani, R. E., Mirzakuchaki, S. and Zamanidoost, A., "Design and simulation of a cmos DLL-based frequency multiplier", in Industrial Electronics & Applications (ISIEA), 2010 IEEE Symposium on, (2010), 450-455.
13. Hu, W., Chunglen, L. and Wang, X., "Fast frequency acquisition phase-frequency detector with zero blind zone in PLL", ***Electronics Letters***, Vol. 43, No. 19, (2007). .

# Phase Frequency Detector Using Transmission Gates for High Speed Applications

M. Gholami

*Faculty of Engineering and Technology, University of Mazandaran, Babolsar, Iran*

*P A P E R I N F O*

*Paper history:*
Received 13 May 2016
Received in revised form 27 May 2016
Accepted 02 June 2016

*Keywords*:
Phase-frequency Detectors
Phase Detector
Delay Locked Loop
Phase locked Loop
Transmission Gate
Transceiver

**چکیده**

در این مقاله یک آشکارساز فاز–فرکانس جدید با استفاده از گیتهای انتقال داده ارائه شد، که قادر است اختلافهای فاز کمتر از ۵۰۰ پیکو ثانیه را آشکار نماید. به عبارت دیگر آشکارساز فاز–فرکانس پیشنهادی قابلیت عملکرد صحیح تا فرکانسهای بالاتر از ۱/۷ گیگا هرتز را دارد. این در حالی است که آشکارسازهای فاز–فرکانس متداول در فرکانسهایی کمتر از ۱/۱ گیگاهرتز کارایی دارند. این ساختار جدید در تکنولوژی ۰/۱۳ میکرون طراحی شده است. همچنین با توجه به نتایج شبیه سازی نیز ساختار پیشنهادی گستره قفلی در حدود دو برابر ساختار آشکارساز فاز–فرکانس متداول دارد. نتایج شبیه سازی ارائه شده موید محاسبات تئوری بوده است. همچنین مدار پیشنهادی جهت تصدیق عملکرد در یک حلقه قفل شده تاخیر مورد استفاده قرار گرفته است.

***doi**: 10.5829/idosi.ije.2016.29.07a.05*