



Implementation of Floating Output Interleaved Input DC-DC Boost Converter

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ABSTRACT

This paper explores and presents the analysis, design and implementation of a high voltage ratio topology of DC-DC converter. The DC-DC converter has high voltage ratio with reduced output voltage and output current ripple, also reduces the voltage and current rating of power electronic components compared with conventional boost converter. The voltage stress on the switches are reduced in this topology. Analysis, design and converter operating waveforms in the continuous conduction mode are provided along with design guidelines. The converter has been designed for rated power of 50W, input voltage of 24V, output voltage of 72V and switching frequency of 25 kHz. The floating output interleaved input high voltage gain converter is compared with conventional boost converter, hardware and simulation results are verified.

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1. INTRODUCTION

Fuel cells are considered to be one of the most promising sources of distributed energy because of their efficiency and low environmental impact. A fuel cell (FC) may be one of the solutions to decrease carbon dioxide emission. Fuel cells are low voltage current intensive sources. A single cell produces a voltage of approximately 0.7 to 1.2 V; therefore, several cells must be stacked to achieve high voltage output [1]. Power converters are often necessary to boost and regulate the voltage as means to provide stiff voltage. In order to use fuel cell as energy, it is necessary to have a stiff voltage source. The examination of various topologies of DC-DC boost converters and used for power conditioning of fuel cells. The life of fuel can be reduced and responds sluggishly, due to presence of ripple in input current. This problem can be overcome by interleaved topology [2, 3]. Initially, cascaded boost converter and interleaved converter are conventionally used to obtain the required high voltage gain. Higher losses in cascaded boost converter prove to be an obstacle to obtain high efficiency and high voltage gain [4].

Isolated converter topologies were used to achieve the required voltage gain, but these topologies require coupled inductors and transformers [5, 6]. Due to addition of coupled inductors and transformers, isolated converter becomes expensive and larger in size. It is necessary to have low input ripple current at the DC-DC boost converter in order to maximize the FC life time, and traditional DC-DC converter topologies have poor performance [7].

A cascade DC-DC converter composing of two phase-interleaved boost converters and three level series boost converters is proposed in [8]. A review of isolated and non-isolated boost DC-DC converters suitable for FC and photovoltaic grid connected applications is proposed in the literature [9]. The closed loop control implementation of DC-DC converter using conventional PI controller and an intelligent controller is presented in some studies [10, 11]. The drawbacks of isolated converters are overcome by non-isolated topologies [12]. In another work [13], DC-DC multilevel converters are discussed to achieve high voltage gain. The limitations of the conventional boost converters and interleaved boost converters applications are analyzed. Furthermore, the advantages and disadvantages of these converters are discussed in the literature [14].

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2. BOOST CONVERTER TOPOLOGIES

The basic conventional boost converter topology is shown in Figure 1. In boost converter, the output voltage is greater than the input voltage. In this topology, input current ripples are more, so not recommended for fuel cell applications. The voltage gain of conventional boost converter is:

$$\frac{V_0}{V_{in}} = \frac{1}{1-K} \tag{1}$$

The inductors current ripple Δi peak to peak amplitude is given by:

$$\Delta i = \frac{V_{in} \times K}{f_s \times L} \tag{2}$$

where f_s is the switching frequency, K is the duty ratio, V_{in} is the input voltage and L is the inductance. The value of inductor is given by:

$$L = \frac{V_{in} \times K}{f_s \times \Delta i_L} \tag{3}$$

The value of capacitance is given by:

$$C = \frac{I_0 \times K}{f_s \times \Delta V_C} \tag{4}$$

where V_{in} is the supply voltage, Δi_L is inductor ripple current, I_o is output current, ΔV_c is capacitor ripple voltage and k is duty ratio.

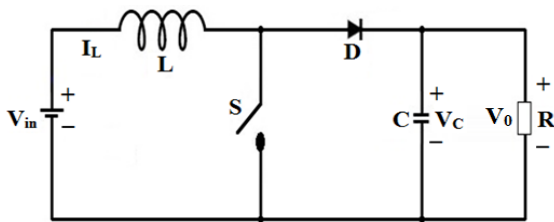


Figure 1. Boost converter (BC)

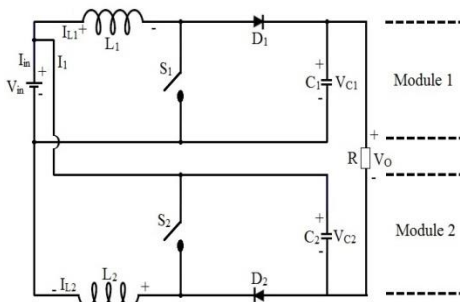


Figure 2. Floating output interleaved input boost converter

Two boost converters are connected in series at the output in order to get the high voltage gain. The series connection of two modules results in reduction of input current, output voltage and output current ripples and rating of the devices.

3. OPERATING PRINCIPLE OF FIBC

The high-gain floating output interleaved input boost converter topology is shown in Figure 2. In this section various modes of operation of boost converter operation are described in Figures 3-6.

The high voltage gain is obtained when the converter is operating for duty cycle greater than 50% ($K > 0.5$), the analysis of the converter is also presented for duty cycle less than 50% ($K < 0.5$). The power losses are neglected for analysis. Since both converters are boost type, the voltage across each capacitor is greater than the input voltage. Assume that converter is operated in continuous conduction mode (CCM) and the two converters have same duty ratio.

Based on assumption the two converters operate at the same duty cycle; it can be shown that:

$$V_{C1} = V_{C2} \tag{5}$$

The operating wave forms are plotted for both cases when the duty ratio is less than 50% ($K < 0.5$) and greater than 50% ($K > 0.5$).

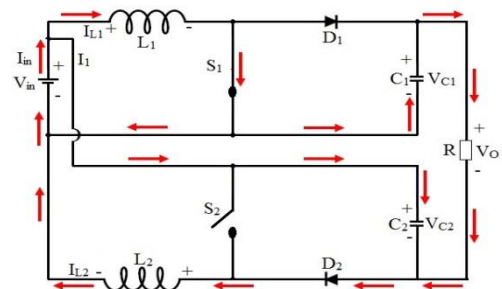


Figure 3. Mode I ($S_1=ON, S_2=OFF$)

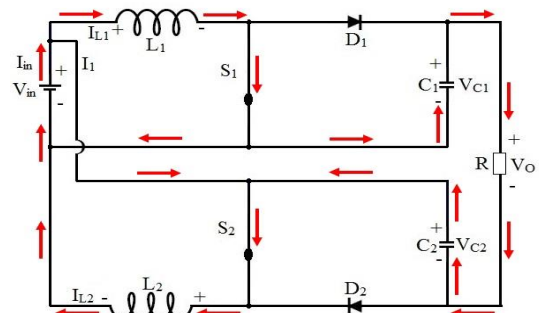


Figure 4. Mode II ($S_1=ON, S_2=ON$)

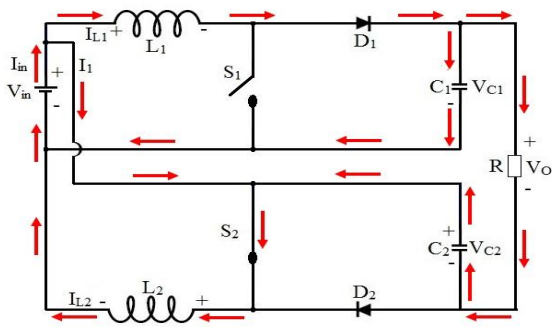


Figure 5. Mode III ($S_1=OFF, S_2=ON$)

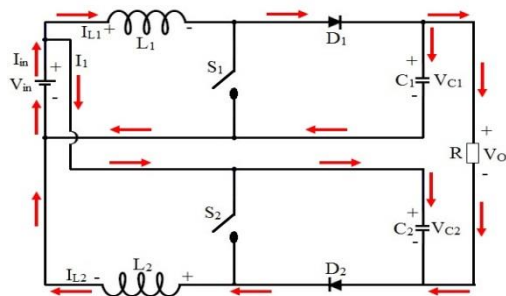


Figure 6. Mode IV ($S_1=OFF, S_2=OFF$)

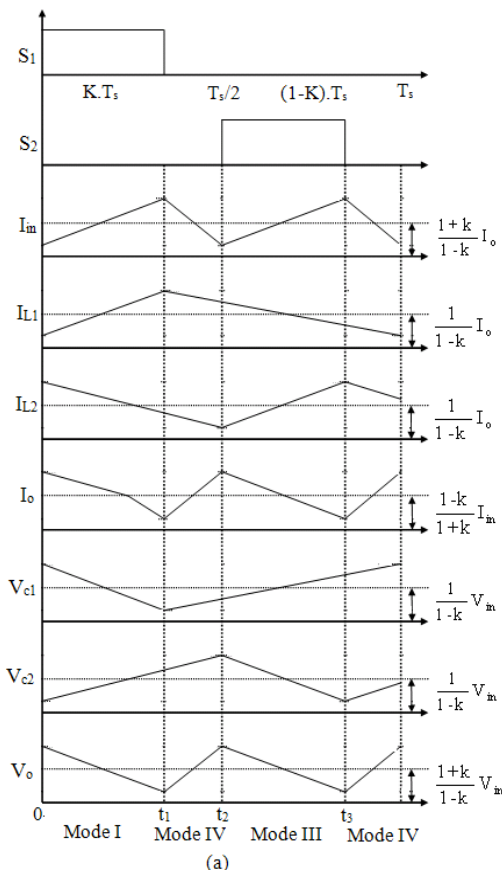


Figure 7. Operating waveforms for $K < 0.5$

3. 1. Operation for $K < 0.5$

Mode: I, $0 \leq t \leq t_1$

(S_1 is ON, S_2 is OFF)

The switch S_1 is ON, diode D_1 is reversed biased and the inductor L_1 starts charging from 0 to t_1 period. The inductor L_1 is being charged up to input source voltage V_{in} and the current through the inductor L_1 increases. The capacitor C_1 starts discharging through the load during this period. The voltage across the inductor is V_{in} .

The switch S_2 is OFF, diode D_2 is forward biased and the energy stored in inductor L_2 starts linearly discharging from 0 to t_1 as shown in Figure 7. The capacitor C_2 charges during this period.

The voltage across inductor L_2 is:

$$V_{L2} = V_{in} - V_{C2} \tag{6}$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \tag{7}$$

Mode: IV, $t_1 \leq t \leq t_2$ (S_1 is OFF, S_2 is OFF)

The switch S_1 is OFF, diode D_1 is forward biased and the inductor L_1 starts discharging from t_1 to t_2 period as shown in Figure 7. The capacitor C_1 charges during this period. The voltage across the inductor L_1 is:

$$V_{L1} = V_{in} - V_{C1} \tag{8}$$

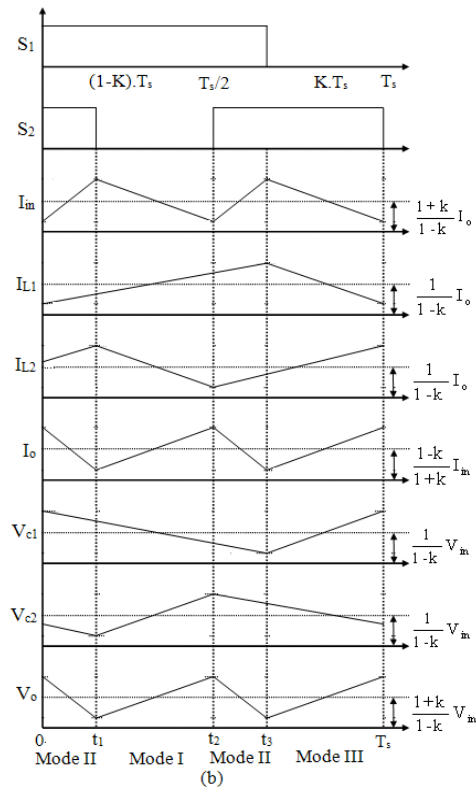


Figure 8. Operating waveforms for $K > 0.5$

The switch S_2 is OFF, diode D_2 is forward biased and the energy stored in inductor L_2 starts linearly discharging from t_1 to t_2 as shown in Figure 7. The capacitor C_2 charges during this period. The voltage across inductor L_2 is:

$$V_{L2} = V_{in} - V_{C2} \quad (9)$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \quad (10)$$

Mode: III, $t_2 \leq t \leq t_3$ (S_1 is OFF, S_2 is ON)

The switch S_1 is OFF, diode D_1 is forward biased and the inductor L_1 starts discharging form t_2 to t_3 period as shown in Figure 7. The capacitor C_1 charges during this period. The voltage across the inductor L_1 is:

$$V_{L1} = V_{in} - V_{C1} \quad (11)$$

The switch S_2 is ON, diode D_2 is reversed biased and inductor L_2 starts linearly charging from t_2 to t_3 as shown in Figure 7. The capacitor C_2 discharges through the load during this period. The voltage across inductor L_2 is:

$$V_{L2} = V_{in} \quad (12)$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \quad (13)$$

Mode: IV, $t_3 \leq t \leq T_s$ (S_1 is OFF, S_2 is OFF)

The switch S_1 is OFF, diode D_1 is forward biased and the inductor L_1 starts discharging form t_3 to T_s period as shown in Figure 7. The capacitor starts charging during this period. The voltage across the inductor L_1 is:

$$V_{L1} = V_{in} - V_{C1} \quad (14)$$

The switch S_2 is OFF, diode D_2 is forward biased and the energy stored in inductor L_2 starts linearly discharging from t_3 to T_s as shown in Figure 7. The capacitor starts charging during this period. The voltage across inductor L_2 is:

$$V_{L2} = V_{in} - V_{C2} \quad (15)$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \quad (16)$$

3. 2. Operation for $K > 0.5$

Mode: II, $0 \leq t \leq t_1$ (S_1 is ON, S_2 is ON)

The switch S_1 is ON, diode D_1 is reversed biased and the inductor L_1 starts charging form 0 to t_1 period. The inductor L_1 is being charged up to input source voltage V_{in} and the current through the inductor L_1 increases. The capacitor gets discharging during this period. The

voltage across the inductor is V_{in} . The switch S_2 is ON, diode D_2 is reversed biased and inductor L_2 starts linearly charging from 0 to t_1 as shown in Figure 8. The capacitor C_2 discharges through the load during this period. The voltage across inductor L_2 is:

$$V_{L2} = V_{in} \quad (17)$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \quad (18)$$

Mode: I, $t_1 \leq t \leq t_2$ (S_1 is ON, S_2 is OFF)

The switch S_1 is ON, diode D_1 is reversed biased and the inductor L_1 starts charging form t_1 to t_2 period. The inductor L_1 is being charged up to input source voltage V_{in} and the current through the inductor L_1 increases. The voltage across the inductor is v_{in} .

The switch S_2 is OFF, diode D_2 is forward biased and the energy stored in inductor L_2 starts linearly discharging from t_1 to t_2 as shown in Figure 8. The capacitor C_2 starts charging during this period. The voltage across inductor L_2 is:

$$V_{L2} = V_{in} - V_{C2} \quad (19)$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \quad (20)$$

Mode: II, $t_2 \leq t \leq t_3$ (S_1 is ON, S_2 is ON)

The switch S_1 is ON, diode D_1 is reversed biased and the inductor L_1 starts charging form t_2 to t_3 period. The inductor L_1 is being charged up to input source voltage V_{in} and the current through the inductor L_1 increases. The capacitor gets discharging during this period. The voltage across the inductor is V_{in} .

The switch S_2 is ON, diode D_2 is reversed biased and inductor L_2 starts linearly charging from t_2 to t_3 as shown in Figure 8. The capacitor C_2 discharges through the load during this period. The voltage across inductor L_2 is:

$$V_{L2} = V_{in} \quad (21)$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \quad (22)$$

Mode: III, $t_3 \leq t \leq T_s$ (S_1 is OFF, S_2 is ON)

The switch S_1 is OFF, diode D_1 is forward biased and the inductor L_1 starts discharging form $t_3 \leq t \leq T_s$ period as shown in Figure 8. The capacitor C_1 charges during this period. The voltage across the inductor L_1 is:

$$V_{L1} = V_{in} - V_{C1}$$

The switch S_2 is ON, diode D_2 is reversed biased and inductor L_2 starts linearly charging from $t_3 \leq t \leq T_s$ as shown in Figure 8. The capacitor C_2 discharges through the load during this period. The voltage across inductor L_2 is:

$$V_{L2} = V_{in} \tag{23}$$

The output voltage is:

$$V_o = V_{C1} + V_{C2} - V_{in} \tag{24}$$

4. ANALYSIS OF CONVERTER

Both modules operate in continuous conduction mode. The voltage across each capacitor C_1 and C_2 is:

$$V_{c1} = V_{c2} = \left(\frac{1}{1-K}\right) \times V_{in} \tag{25}$$

The two capacitors are always in series with voltage source in various modes of operation. The output voltage can be expressed as:

$$V_o = V_{C1} + V_{C2} - V_{in} \tag{26}$$

$$\frac{V_o}{V_{in}} = \frac{1+K}{1-K} \tag{27}$$

The voltage gain of the proposed converter is high when compared to conventional boost converter.

5. DESIGN ASPECTS OF CONVERTER

The inductor and capacitor components are derived from the operation of converter. When the duty ratio is less than 50% ($K < 0.5$)

$$L = \frac{2(0.5 - K)(V_C - V_{in})}{\Delta i_{in} f_s} \tag{28}$$

when the duty ratio is greater than 50% ($K > 0.5$)

$$L = \frac{2V_{in}(K - 0.5)}{\Delta i_{in} f_s} \tag{29}$$

where f_s is the switching frequency, K is the duty ratio, V_{in} is the input voltage and L is the inductance. Δi_{in} is ripple current. When the duty ratio is less than 50% ($K < 0.5$)

$$C = \frac{2I_o K(0.5 - K)}{\Delta V_o f_s} \tag{30}$$

when the duty ratio is greater than 50% ($K > 0.5$)

$$C = \frac{2I_o (K - 0.5)}{\Delta V_o f_s} \tag{31}$$

where f_s is the switching frequency, K is the duty ratio, ΔV_o is the ripple voltage and C is the capacitance.

6. SIMULATION RESULTS

The simulation parameters for both converters are designed for same output power rating but different duty ratios. The parameters are shown in Table 1. In the proposed converter the voltage and current ripples are reduced at 50% duty ratio.

6. 1. Gate Pulses of Converters

The gate pulses are generated for conventional boost converter with 66.6% duty cycle as shown in Figure 9 and for proposed converter with 50% duty cycle as shown in Figure 10. Ideal switches are used for simulation.

TABLE 1. Simulation parameters

Parameters	BC	FIBC
Output power	50W	50W
Output voltage	72V	72V
Output current	0.699A	0.699A
Load resistance	103Ω	103Ω
Frequency	25 kHz	25 kHz
Duty cycle	66.66%	50%
Input voltage	24V	24V
Input current	2.1A	2.1A
Inductance	6.08mH	1.827mH
Capacitance	5.18μF	1.555μF

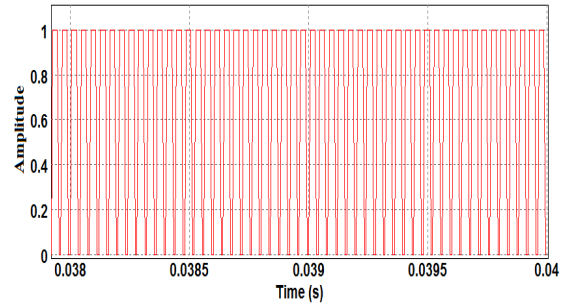


Figure 9. Gate pulses for conventional BC

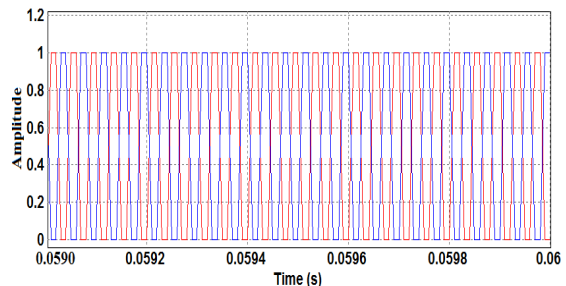


Figure 10. Gate pulses for FIBC

6. 2. Output Voltage of Converters Figures 11-12 depict the output voltage waveforms of conventional boost converter and floating output interleaved input boost converter. From simulation results it can be observed that output voltage ripples are reduced in floating output interleaved input boost converter.

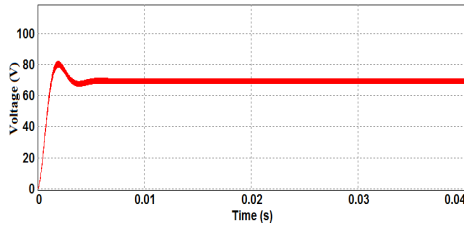


Figure 11. Output voltage BC

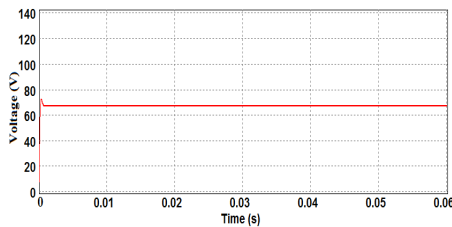


Figure 12. Output voltage of FIBC

6. 3. Input Current of Converters Figures 13-14 present the input current waveforms of conventional boost converter and floating output interleaved input boost converter. From simulation results, it is observed that output current ripples are reduced in FIBC.

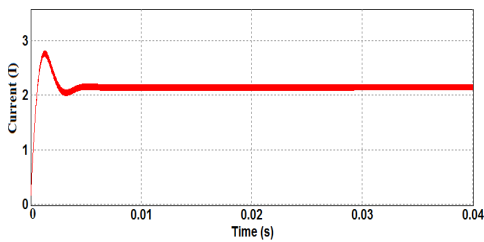


Figure 13. Input current of boost converter(BC)

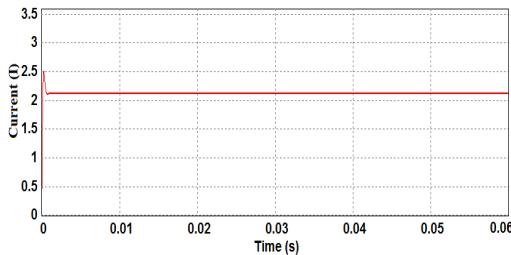


Figure 14. Input current of FIBC

6. 4. Comparison Results of BC and FIBC Table 2 presents the comparison of results obtained for BC and FIBC.

7. EXPERIMENTAL RESULTS

The presented FIBC and conventional BC topologies with the designed parameters are implemented in hardware. The critical value of inductance for designed parameters is 6.08mH for conventional BC and 1.827mH for FIBC converter. The critical value of capacitance arrived through the design is 5.18 μ F for conventional BC and 1.555 μ F for FIBC. However, the practical values used for implementation of the hardware are 10 μ F and 47 μ F for the conventional BC and FIBC, respectively.

7. 1. Gate Pulses for Converters The gate pulses are generated using pickit-3. The driver circuit output pulses for conventional BC with 66.6% duty cycle is shown in Figure 15 and for FIBC converter with 50% duty cycle for each switch with 180⁰ phase shift is shown in Figure 16.

7. 2. Output Voltage Waveform of Converters Figures 17-18 show the output voltage waveforms of boost converter and FIBC. From the results it can be observed that the average output voltages of BC and FIBC are 67V and 65.1V, respectively.

TABLE 2. Comparison results of BC and FIBC

Parameters	BC	FIBC
Inductance	6.08mH	1.827mH
Capacitance	5.18 μ F	1.555 μ F
Voltage across swithses	72V	50V
Input current ripple	4.6%	0.326%
Output current ripple	4.9%	0.560%
Output voltage ripple	5%	0.571%

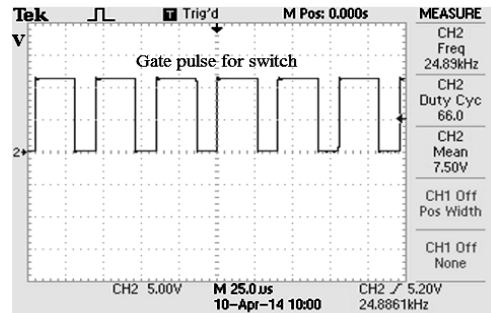


Figure 15. Gate pulses for BC

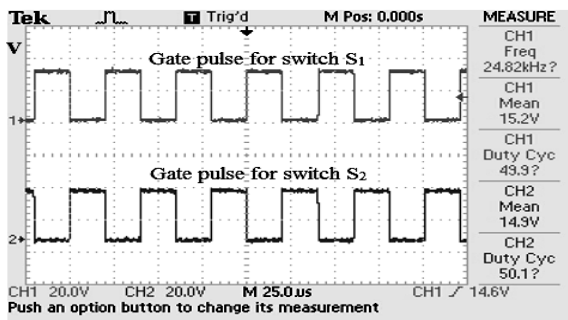


Figure 16. Gate pulses for FIBC

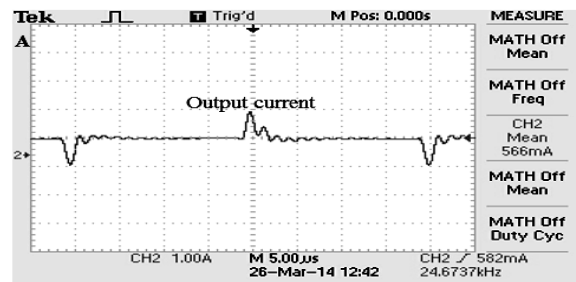


Figure 20. Output current waveform of FIBC

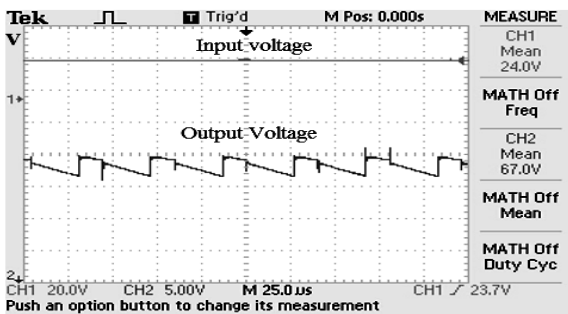


Figure 17. Output voltage waveform of BC

From hardware results it can be observed that the average output current of BC and FIBC is 652mA and 566 mA, respectively.

7. 4 Input Current Waveform of Converters

Figures 21-22 present the hardware input current waveforms of conventional BC and FIBC. From the results it can be observed that the average input current of BC and FIBC is 2.22 and 2.47A, respectively.

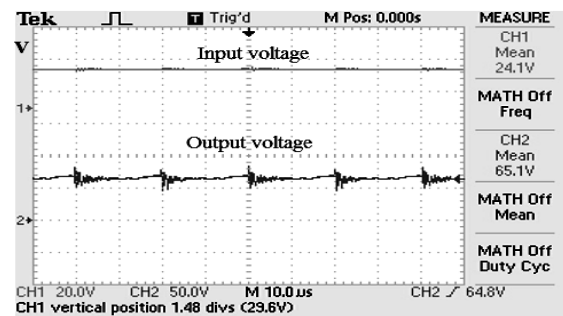


Figure 18. Output voltage waveform of FIBC

7. 5 Voltage Across Switches of Converter

Figure 23 shows the voltage across switch in conventional boost converter (BC). Figures 24 and 25 present the voltage across the two switches in FIBC. From hardware results it can be observed that the voltage stresses on the switches are reduced in FIBC.

7. 3. Output Current Waveforms of Converters

Figures 19-20 present the hardware output current waveforms of conventional BC and FIBC.

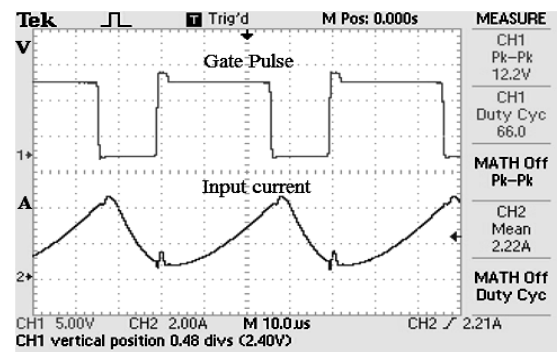


Figure 21. Input current waveform of BC

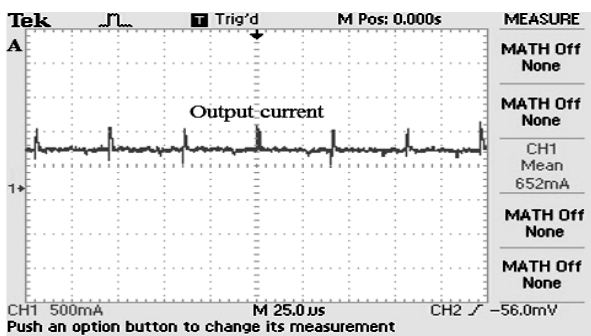


Figure 19. Output current waveform of BC

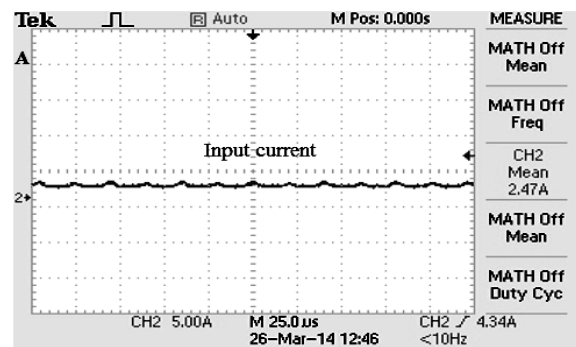


Figure 22. Input current waveform of FIBC

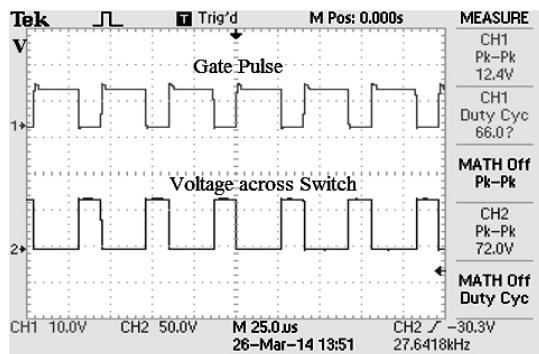


Figure 23. Voltage across switch in BC

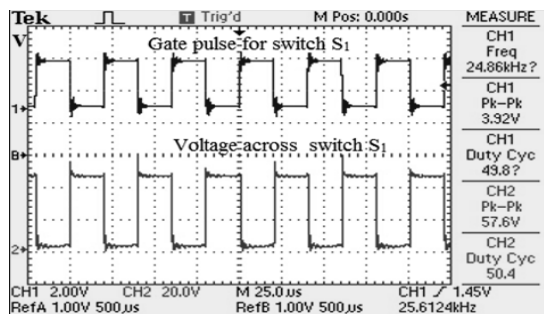


Figure 24. Voltage across switch S1 in FIBC

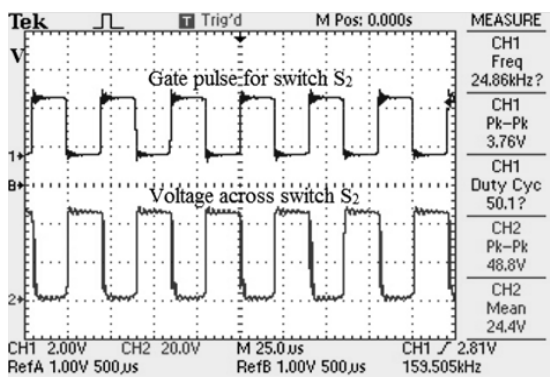


Figure 25. Voltage across switch S2 in FIBC

8. CONCLUSION

A generalized approach to derive a floating-output interleaved input DC-DC boost converter from basic boost converter is presented. The two BCs connected in series through load at output and input source are connected by interleaved method. A high voltage gain BC is derived with reduced input current, output current and output voltage ripples. The voltage stress across each device is less, so low voltage devices are applicable for floating output interleaved input boost converter. The floating output interleaved input boost converter has been designed for rated power of 50W, input voltage is 24V, output voltage is 72V and

switching frequency is 25 kHz. The performance of the presented topology is confirmed through experimental results.

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Implementation of Floating Output Interleaved Input DC-DC Boost Converter

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این مقاله به بررسی و ارائه تجزیه و تحلیل، طراحی و پیاده سازی یک توپولوژی با نسبت ولتاژ بالا مبدل DC-DC می پردازد. مبدل DC-DC با نسبت ولتاژ بالا با ولتاژ خروجی کاهش یافته و جریان خروجی موجی دارد، همچنین باعث کاهش ولتاژ و جریان توان اجزای الکترونیکی در مقایسه با مبدل بوست معمولی می شود. استرس ولتاژ در سوئیچ ها در این توپولوژی کاهش می یابد. تحلیل، طراحی و عامل تبدیل شکل موج در حالت انتقال مستمر همراه با دستورالعمل های طراحی ارائه شده است. مبدل برای قدرت 50W، ولتاژ ورودی 24V، ولتاژ خروجی 72V و فرکانس سوئیچینگ 25 کیلو هرتز طراحی شده است. مبدل ولتاژ بالا ورودی با خروجی شناور با مبدل بوست معمولی مقایسه شده است و نتایج سخت افزار و شبیه سازی تایید شده است.

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