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Dual Phase Detector Based on Delay Locked Loop for High Speed Applications

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ABSTRACT

In this paper a new architecture for delay locked loops is proposed. Static phase offset and reset path delay are the most important problems in phase-frequency detectors (PFD). The proposed structure decreases the jitter resulted from PFD by switching two PFDs. In this new architecture, a conventional PFD is used before locking of DLL to decrease the amount of phase difference between input and output of the DLL. Near locking, an XOR gate is used to act as a PFD which makes the DLL locks with less jitter. Also, the reset path time and glitch are decreased by using the XOR gate. The proposed architecture has been designed in TSMC 0.18um CMOS Technology. The simulation results support the theoretical design aspects.

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1. INTRODUCTION

Nowadays, Delay Locked Loops (DLLs) and Phase Locked Loops (PLLs) are widely used in high-speed systems, frequency synthesizers [1, 2], RAM [3], clock synchronization and clock and data recovery circuits [4]. They are unavoidable parts in communication systems. Due to the better jitter performance of DLLs, they are used more than PLLs when minimizing of jitter is important [5, 6]. Conventional DLLs are first order system, hence they are inherently stable. Also, they need a smaller chip area than PLLs [7].

In the design of frequency multiplier and clock and data recovery circuits, jitter is one of the most important parameters. Hence, designing a DLL with lower RMS jitter is of high importance. DLL consists of four main blocks: Chare Pump (CP), Phase Frequency Detector (PFD), Voltage Controlled Delay Line (VCDL) and Loop Filter. Non-ideal blocks and also mismatches in DLL result in jitter at the output of them. One of the main sources of jitter in DLLs is PFD [8]. Recent works try to decrease the phase offset in PFDs [9-11] by reducing the reset path delay [10, 11] or dead zone [9] in PFD to have better jitter performance. Although, these methods reduce jitter but they cause more chip area and complexity in systems.

The simplest and fastest PFD which can be used in DLLs or PLLs is an XOR gate. To have high speed DLLs, we need to use high speed PFDs. An approach to decrease the phase offset is to apply two PFDs in DLL architecture. In this paper a DLL with two PFDs is used to decrease the amount of RMS jitter, glitch and reset time. In the proposed architecture, a conventional PFD is used before locking of DLL to decrease the amount of phase difference between input and output of the DLL. When the DLL is about to lock, an XOR gate is used to act as a PFD which makes the DLL locks with less jitter. A conventional PFD is used because it can detect the phase differences between -2π to 2π while XOR gates can only detect the phase differences between 0 to 2π. The paper is organized as follows. Next section introduces the conventional DLL-based frequency synthesizer and some of its limitations. Section 3 describes the proposed low jitter and high frequency architecture for DLL-based frequency synthesizers. In this section, both system level and circuit level design of proposed DLL-based frequency synthesizer is explained. Simulations and the results are discussed in section 4.

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2. STATIC PHASE ERROR DUE TO CONVENTIONAL PFD IN DLLS

Figure 1 shows the architecture of conventional DLL. As can be seen in this figure, a conventional DLL consists of a Phase-Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LF) and a Voltage Controlled Delay Line (VCDL). The phase difference between REF and OUT signals is determined by PFD. The produced signal by PFD is sent to CP. To adjust the delay of each delay cell, CP and LF (Integrator) generate appropriate value for control voltage of VCDL (V_{cntl}) based on the phase differences of REF and OUT signals. This process is repeated until the DLL is locked. It should be mentioned that in lock condition, the input and output of VCDL are in phase and the delay which is produced by VCDL is exactly equal to T_{REF} (T_{REF} is the period of reference clock).This means that in lock condition REF and OUT have exactly one clock period difference.

One of the most important features of DLLs is that they show lower jitter than PLLs. All the building blocks of DLL can be source of the jitter. PFD is one of the main sources of the jitter in DLLs. Due to reset path delay in conventional PFD shown in Figure 2 a static phase error is generated. Figure 3 shows a common PFD in which NAND-based latches are used [10]. The reset path in this PFD consists of two two-input, one four-input, and one three-input NAND gates. The total delay of the reset path causes static phase error. So, to have better jitter performance, it is necessary to decrease the reset path delay.

Using an XOR gate instead of conventional PFD is one approach to solve these problems. Although, an XOR gate operates as fastest PFD, but it can only detect the phase offset between 0 to 2π. However, in DLLs a PFD is needed for detecting the phase offset between -2π and +2π (or 0 and 4π). Therefore, the conventional PFD cannot be replaced with an XOR gate for all conditions. Another challenge for decreasing the amount of jitter due to the static phase error of PFD is to pass the role of PFD to the XOR gate when the locking condition occurs in the DLL. That means, when a DLL is about to lock, the conventional PFD is stopped working and the XOR gate operates as a PFD. Since in this case, the phase offset between the reference clock and the output of VCDL (two inputs of PFD) is small (about the reset path delay of conventional PFD) the XOR gate is able to detect this small phase offset.

3. PROPOSED ARCHITECTURE

The proposed architecture for DLL which employs two PFD is shown in Figure 4. As can be seen from this figure, the proposed circuit has four more blocks: lock detector, integrator, comparator and an XOR gate compared with conventional DLL shown in Figure 1. The lock detector shows whether the DLL is not locked or is about to lock. The comparator compares the DC value of V_{Lock} with V_{REF}. V_{Select}, the output of the comparator, determines whether PFD-CP or XOR should be used in the feedback loop. In other words, if the DLL is near the lock condition, V_{Select} is logical ZERO and therefore S_2 is ON and S_1 is OFF and the feedback loop is closed with XOR gate. On the other hand, when the DLL is far from lock condition, V_{Select} is logical ONE and therefore S_1 is ON and S_2 is off. So, the feedback loop is closed with PFD and CP path. The lock detector detects the moment of DLLs lock (when REF and OUT are approximately in phase). In this design the lock detector circuit consists of only an XOR gate and an integrator to calculate the average of the signal at the output of XOR gate in each period (average of V_{Lock}).

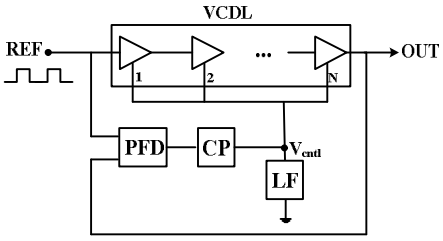

Figure 1. Architecture of conventional DLL.

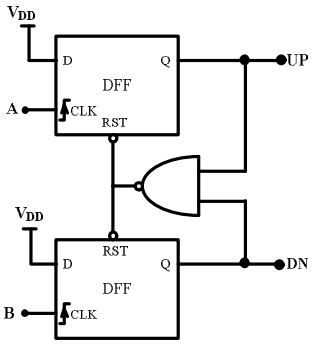

Figure 2. Conventional PFD.

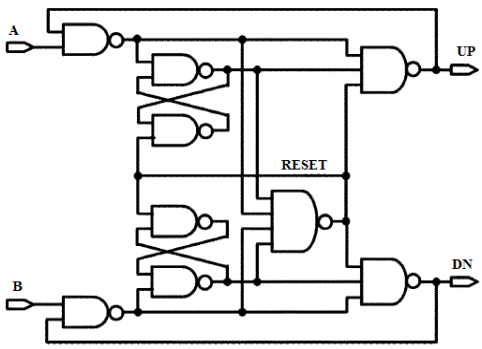

Figure 3. Gate level implementation of conventional PFDs.

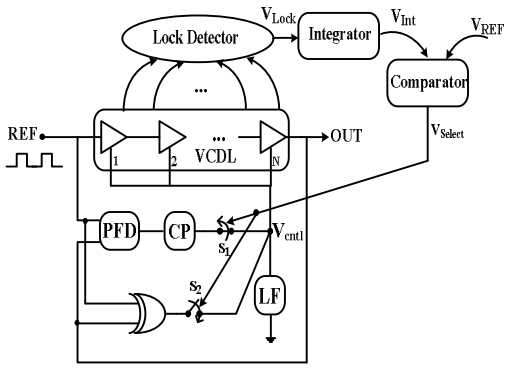

Figure 4. Proposed dual PFD delay locked loop.

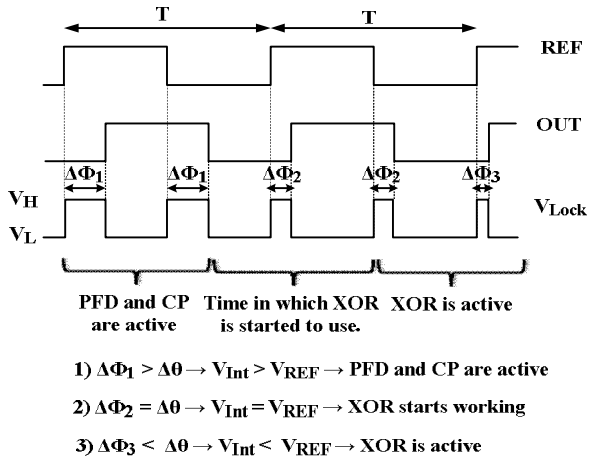

Figure 5. Related waveforms for lock detector circuit.

The two inputs of this XOR gate come from the input and output of the VCDL. Since, near the lock condition REF and OUT are approximately equal, XOR of them generates a signal with average close to zero. The output of this circuit (V_{Lock}) is sent to the comparator. In the comparator the average of V_{Lock} is compared with V_{REF}. V_{REF} is calculated from the required accuracy of the lock condition. In other words, if REF and OUT has a phase difference of $\Delta\theta$ ($\Delta\theta$ is small value) the lock detector and the comparator circuit should generate new value for V_{Select} to change the feedback path from PFD-CP to XOR gate. This means that the $\Delta\theta$ phase difference is a value that can be detected by the XOR gate. According to Figure 6 which shows V_{Lock} in three different cases, near the lock condition, V_{REF} should be:

$$V_{REF} = \frac{2\times\Delta\theta\times(V_H - V_L)}{T} \quad (1)$$

As mentioned before, $\Delta\theta$ is the phase difference of REF and OUT on which the path should be changed from PFD-CP to XOR. V_H and V_L are the maximum and minimum voltage of V_{Lock} and T is the period of the reference clock. When $V_{Int}>V_{REF}$, the feedback path is closed with PFD-CP path and when $V_{Int}<V_{REF}$, the feedback path is closed with an XOR gate to have a DLL with lower jitter.

4. SIMULATIONS AND RESULTS

The proposed dual PFD DLL is designed in TSMC 0.18um CMOS Technology in frequency near to 167MHz (T_{REF}=6ns) by using ADS (Advanced Design System) simulator. All building blocks of DLLs are implemented by CML logic as in [12]. Figure 6 shows the results of simulation of the proposed dual PFD delay locked loop. In this figure, waveforms are shown near the lock condition and before t=550ps, the conventional PFD is used and hence the output of XOR gate is not considered. After t=550ps, the XOR gate operates as a phase detector to have better jitter performance and lock condition and lower glitch and reset time. In this situation, the output of PFD-CP is not important. It should be mentioned that in t=550ps, V_{Select} is high to switch the path from PFD to XOR gate. Simulations show that since the signal width of the output of the XOR gate is decreased (glitch time) by order of 5 and also the variations in control signal when the XOR gate operates is smaller than that of PFD, therefore the output jitter is decreased. Figure 6 also indicates that the proposed architecture has a lower reset path and glitch time. Table 1 shows a comparison of this work with other related works. The proposed architecture consumes a little more power than conventional DLLs [12] but as shown, it can work in higher frequencies with better jitter performance.

TABLE 1. Comparison of this work with other

Authors	Technology	Power supply	Power	Cycles for lock	Peak to peak jitter	RMS jitter
† Shin et al. [13]	0.18 µm	1.8V	43mW@1.5GHz	15	7ps@1.5GHz	------
† Cheng et al. [14]	0.25 µm	2.5V	15mW@320MHz	22	15ps@200MHz	4.44ps@200MHz
† Chang et al. [15]	0.18 µm	1.4V-2.5V	23mW@700MHz	32	17.6ps@700MHz	------
† Yang et al. [16]	0.18 µm	1.8V	12.6mW@550MHz	14-134	12ps@550MHz	1.5ps@550MHz
* Gholami et al. [12]	0.13µm	1.2V	2.62mW@216MHz	40	------	10ps@216MHz
*This Work	0.18µm	1.8V	6.1mW@167MHz	44	17ps@167MHz	8ps@167MHz

† Measured *Simulated

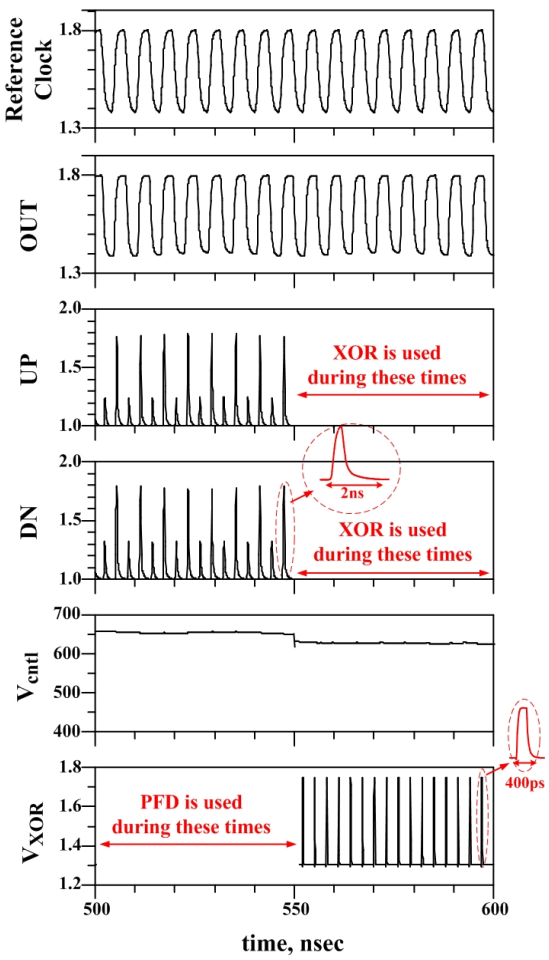

Figure 6. Waveforms of proposed dual PFD based DLL.

5. CONCLUSION

In this paper a new architecture for delay locked loops has been proposed in which two different PFDs have been used: a conventional PFD and an XOR gate. The conventional PFD works in the circuit before locking occurs and the XOR gate operates as a PFD when the DLL is about to be locked. The proposed architecture is designed in TSMC 0.18um CMOS Technology. The simulation results show that this architecture has a lower reset path and glitch time.

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چکیده

در این مقاله یک ساختار جدید برای حلقه‌های قفل شده تاخیر ارائه شده است. خطای فاز استاتیکی و تاخیر مسیر ریست از مهمترین مشکلات موجود در آشکارسازهای فاز- فرکانس می‌باشند. ساختار ارائه شده قادر است جیتر ناشی از آشکار ساز فاز- فرکانسرا با استفاده از سوییچ دو آشکارساز کاهش دهد. در این ساختار جدید ابتدا آشکار ساز فاز- فرکانس متداول برای کم کردن اختلاف فاز بین ورودی و خروجی حلقه قفل شده تاخیر، مورد استفاده قرار می‌گیرد. سپس در شرایط نزدیک قفل، یک گیت XOR به عنوان آشکارساز استفاده می‌گردد که منتهی به کم شدن جیتر در حلقه قفل شده تاخیر پیشنهادی خواهد شد. همچنین زمان مسیر ریست و زمان پرشهای ناخواسته (glitch) در ساختار پیشنهادی، با استفاده از گیت XOR کاهش می‌یابد. ساختار مورد نظر در تکنولوژی ۰/۱۸ میکرون CMOS شبیه‌سازی شده است. نتایج شبیه‌سازی، پیش‌بینی‌های تئوری ارائه شده را تایید کرده است.

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