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A Novel Low Voltage, Low Power and High Gain Operational Amplifier Using Negative Resistance and Self Cascode Transistors

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ABSTRACT

In this work, a low power, low voltage and high gain operational amplifier is proposed. For this purpose, a negative resistance structure is used in parallel with output to improve the achievable gain. Because of using self cascode transistors in the output, the proposed structure remains approximately constant in a relatively large output voltage swing causing an invariable gain. To evaluate the proposed method an op amp was designed in 0.18µm CMOS technology. The simulation results showed a gain of 84dB, unity gain bandwidth of 12.45MHz and phase margin of 81 degree; with 1V power supply and 1pF load capacitor.

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1. INTRODUCTION

Growing microelectronics industry and emerging short channel CMOS process forced circuit designer to design circuits with higher speed, lower voltage supply and power consumption [1-3]. On the other hand with the advent of electronic equipment in daily life, low power and low voltage along with higher performance designs caught the attention of designers. Unfortunately, the threshold voltage of CMOS transistors hasn't scaled down proportional to the technology [4], so the low voltage design remains a challenging area in the circuit design context [5, 6]. Op amps are one of the key elements in electronics circuits such as filters and A/D (D/A) convertors [7, 8]. In these applications, the high gain of op amps plays a critical role on the performance of the circuits so designing high gain and low voltage op amps is a challenging task for designers [9].

A few techniques have been proposed for increasing the gain of op amps like cascoding transistors that increases the output resistance [10]. However, this technique lowers output swing, so it cannot be considered in low voltage designs. Cascade stages is another approach to increase the gain but these structures usually need compensation circuit and are highly power consuming and low speed [11]. Gain boosting is another technique that like cascade stages have usually low speed [12].

Another approach for op amp gain enhancement is to use parallel negative resistance network at the output stage to increase the equivalent output resistance. There are a few works using this technique mainly because the negative resistance varies with output swing and the circuit loses its performance [13-17]. In this work, the cross coupled pair is used and directly connected to the output as the negative resistance, so no new node is added and the speed isn't degraded so much. Indeed without degrading the speed the gain is increased significantly.

As mentioned before, the main drawback of this technique is the dependency of to the negative resistance to the output swing. To overcome this problem, we introduce a new negative resistance network that is approximately independent to the output swing and holds its good features for large swings as well. The mentioned technique employs self cascode transistors. The rest of the paper is as follows, in section 2, typical op amps are studied and in section 3 the cross coupled pair generating negative resistance is introduced. In section 4, the cascode transistor based negative resistance is described. Section 5, shows the

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simulation results and discussions and finally section 6 concludes the paper.

2. TYPICAL OP AMPS

In the folded cascode op amps (Figure 1) the input differential pair converts the input voltage to current signal. The current signal is directed to the output node with high output resistance and generates the high amplitude output voltage signal.

The gain can be expressed as Equation (1):

$$|A_V| = G_m R_{out} \quad , \quad G_m \approx g_{m1}$$
$$R_{out} \approx \left[(g_{m3}+g_{mb3})r_{o3}(r_{o1} \quad r_{o5})\right] \left[(g_{m7}+g_{mb7})r_{o7}r_{o9}\right]$$
$$|A_V| \approx g_{m1}\{\left[(g_{m3}+g_{mb3})r_{o3}(r_{o1} \quad r_{o5})\right] \left[(g_{m7}+g_{mb7})r_{o7}r_{o9}\right]\} \quad (1)$$

where, r_{oi} and g_{mi} are the output resistance and transconductance of the i-th transistor. Equation (1) indicates that increasing the output resistance increases the op amp overall gain. To do this we can parallel a negative resistor with the output node as shown in Figure 2. Hence, Equation (2) can be written for the op amp gain.

$$|A_{V,new}| = G_m R_{out,new} \quad (2)$$

where, $R_{out,new}$ is the output resistance in the Figure 2. If we consider $R_N = R_{out} + \Delta R_{out}$ we have:

$$R_{out,new} = R_{out} \quad (-R_N) = R_{out} + \frac{(R_{out})^2}{\Delta R_{out}} \quad (3)$$

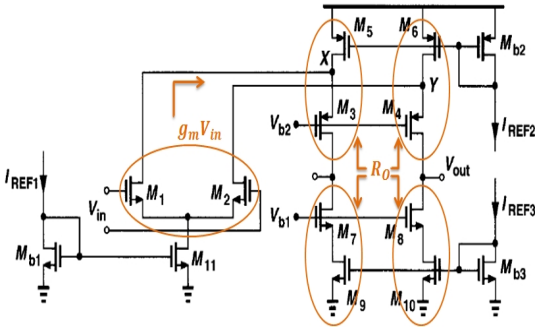

Figure 1. Folded cascade op amp and the simple voltage amplification mechanism.

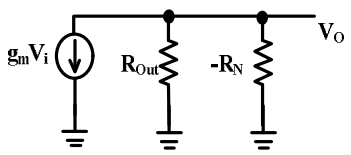

Figure 2. Op amp output node paralleled with a negative resistance.

As shown in Equation (3), small ΔR_{out} causes $R_{out,new}$ to be very larger than R_{out} so the new overall gain will be very larger than the former.

The key point here is that ΔR_{out} should be kept constant over output large swing. In section 3, we show that the traditional negative resistances behave well only over a small voltage interval then we will introduce a novel negative resistance with constant value over a large voltage swing.

3. THE PROPOSED OP AMP AND NEGATIVE RESISTANCE GENERATOR

One stage op amp with self cascode transistors topology is chosen for its low power consumption and power supply. As mentioned before, to increase the op amp gain we parallel a negative resistance to the output.

A simple cross coupled pair generating negative resistance is shown in Figure 3. The current-voltage curve of cross coupled pair is shown in Figure 4.

In Figure 4, the tail current for the curve with label n is n-times of the tail current for the curve with label 1. As shown in Figure 4, the cross coupled pair shows a negative resistance for a narrow voltage. Another key point here is that the curves slope (i.e. the negative resistance), would not remain constant with V_{NR} variations. This will result in the degradation of the negative circuit role for gain enhancement.

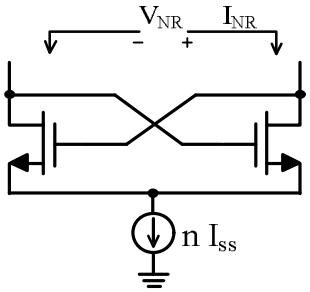

Figure 3. The negative resistance network.

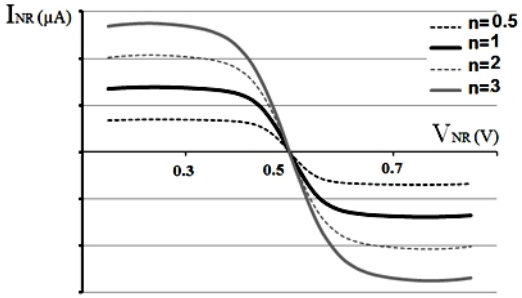

Figure 4. The current-voltage curve of circuit in Figure 3.

Figure 5 shows the negative resistance variations with the output swing. As shown in Figure 5, the negative resistance is constant for a limited output voltage interval (only about 0.2 V) which is not the same as output swing (rail to rail swing). To overcome this problem, we propose a new structure in which the voltage variation over the cross coupled transistors is very small in contrary to the output large swings. In fact, instead of putting the negative resistance directly at the output we use self cascode transistors and put the negative resistance at the drain of the second transistor.

4. SELF CASCODE TRANSISTORS

Using self cascode transistors is an approach that is used in low voltage designs. Figure 6 shows the mentioned transistors and their equivalent. In the Figure 6, gates of M1 and M2 are connected together. Using this combination increases the output resistance without considerably limiting its achievable swing. If both transistors in the Figure 6 have the same aspect ratio then the combinations is equivalent to a transistor with length of twice of each transistor. This means that the output resistance of this structure is more than a single transistor. The size of M1 is usually chosen much greater than M2. This will reduce the variations of V_{OD1}, because in this case the r_{ds1} to output resistance ratio decreases. This causes a small ratio of the output voltage swing put at the V_{DS1}. To improve the output resistance we put the negative resistance at the drain of M1 as shown in Figure 7. The V_{D1} to V_{D2} can be written as (4).

$$\frac{V_{D1}}{V_{D2}} = \frac{r_{ds1}}{r_{ds1}\left(1+g_{m2}r_{ds2}\right)+r_{ds2}} \quad (4)$$

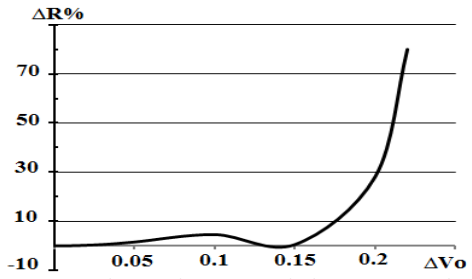

Figure 5. Negative resistance variations versus the output swing.

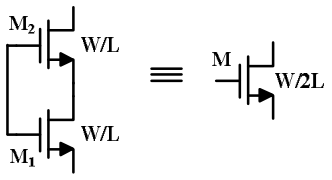

Figure 6. Self cascode transistors and the equivalent transistor

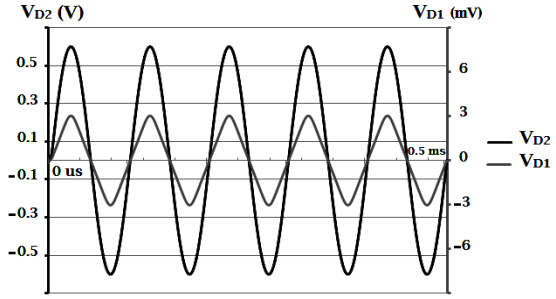

Figure 7. The variations of V_{D1} with respect to the output swing.

In Equation 4, r_{ds1} is the drain-source resistance of M1 in the triode region and r_{ds2} and g_{m2} are the drain-source resistance and transconductance of M2 in saturation region. Obviously, to decrease Equation 4, we should decrease r_{ds1} as much as possible. Regarding the relation between r_{ds1} and V_{D1}, we should decrease V_{D1} to an appropriate level. If r_{ds1} is chosen very small, then the tail current of the negative resistance network would have a great value.

Figure 7 shows the variations of V_{D1} with respect to the output swing. In Figure 7, for a 0.6V output swing V_{D1} experiences a 3 mV variation for which the negative resistance can be considered constant. Putting the negative resistance here provides us a large and constant output resistance over a large output voltage swing. Using this technique, we are now able to design a low voltage and high gain op amp. The designed op amp is discussed in section 5.

5. THE DESIGNED OP AMP

We use the telescopic topology with the minimum stages as the base structure of the designed op amp. The final structure is shown in Figure 8.

In the designed op amp shown in Figure 8, M_{1a}, M_{2a}, M_{3a} and M_{4a}, all are in the triode region, having a small drain to source resistance. So, to increase the equivalent resistor we need to parallel a small negative resistance with these transistors. For small negative resistance, cross coupled pair should be biased with a high tail current that is somehow a problem. To solve this problem we reduce the current of Mia using some additional transistor in parallel to those that leads to higher drain-source resistor. M_{12} and M_{13} are the auxiliary transistors that are added to the circuit to increase the resistance at the drain of input transistors. This causes the major input current signal to direct to the output node and consequently the op amp overall gain is improved.

In the bode diagram, $A_V = \Delta V_o(f)/\Delta V_{in}(f)$ shown in Figure 9, it can be find out that with a proper design we

can obtain very high gain with a 1V DC supply. In addition, regarding to the simple structure of the op amp, there is no need to add compensation circuit.

The output swing is V_{DD}-$2V_{od}$. Note that in the same bias current, self cascode transistors approximately need the same overdrive voltage as a single transistor. So, without restricting the output swing the proposed op amp shows a very higher gain.

The op amp specifications are compared to the other works in Table 1.

6. CONCLUSIONS

In this work a novel low voltage and high gain op- amp is proposed using self cascode transistors. The key point here is the high resistance at the output that remains constant over the whole output swing area. Because of minimum stacking stages used in this work, other specifications such as output swing, circuit speed and power consumption are better or at least comparable to the previous works.

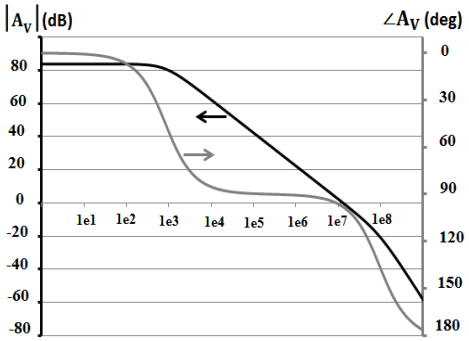

Figure 9. The bode diagram of overall gain of op amp.

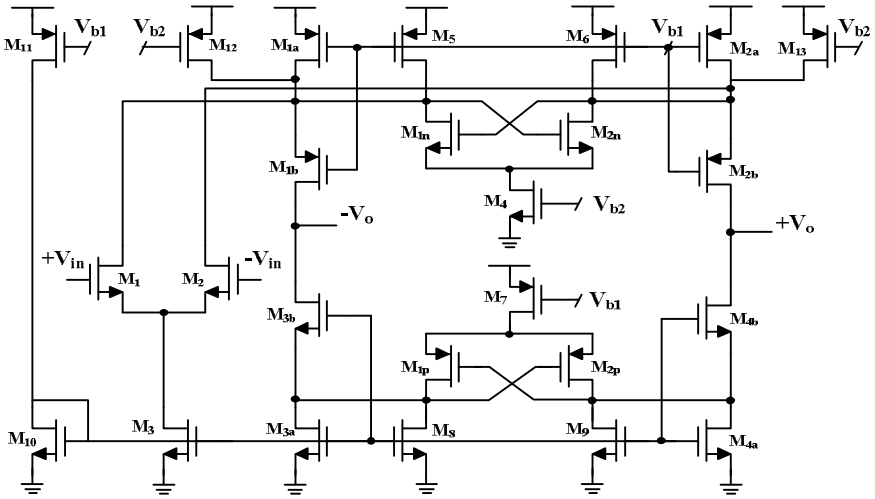

Figure 8. The designed op amp.

TABLE 1. The comparison of proposed op amp specifications with other works.

	Proposed op amp	[4]	[18]	[19]	[20]
Power supply (V)	1	0.6	0.8	0.8	0.9
Open loop gain (dB)	84	73.5	60	49	62
Unit gain frequency (MHz)	12.45	0.013	0.6	69.2	0.54
Phase margin (Degree)	81	54.1	58	42	52
Maximum Signal swing (V)	±(0.07-0.93)	0.04-0.56	0.6	R-R	--
Slew rate (V/µSec)	9.7	0.0147	0.75	9.6	0.23
CMRR (dB)	62.3	67.4	63	89.6	129
PSRR (dB)	74	58.1	58	57.4	76
Power consumption (µW)	85	0.55	54.5	28.6	9.9
Input Voltage noise (nV/√Hz)	645@1KHz	290@1KHz	--	--	--

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A Novel Low Voltage, Low Power and High Gain Operational Amplifier Using Negative Resistance and Self Cascode Transistors

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چکیده

در کار ارائه شده، ساختاری از تقویت کنندهٔ عملیاتی با بهرهٔ بالا و توان پایین بهمراه منبع تغذیه پایین معرفی شده است. برای دستیابی به ویژگی های گفته شده با اتصال موازی ساختار مدار مقاومت منفی در خروجی آپ امپ، بهرهٔ مدار بطور قابل توجهی افزایش می یابد. همچنین با استفاده از ساختار ترانزیستورهای Self cascode در خروجی آپ امپ پیشنهادی، بهبود بهره با وجود تغییرات زیاد ولتاژ در خروجی همچنان برقرار است. برای ارزیابی روش پیشنهادی از طراحی آپ امپ در تکنولوژی CMOS 0.18 µm استفاده شده که شبیه سازی ها بهرهٔ 84 dB، پهنای باند بهرهٔ واحد 12.45 MHz و حاشیهٔ فاز ۸۱ درجه را با منبع تغذیهٔ 1V و خازن خروجی 1 pF نشان داد.

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