FULLY DIFFERENTIAL CURRENT BUFFERS BASED ON A NOVEL COMMON MODE SEPARATION TECHNIQUE

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Abstract In this paper a novel common mode separation technique for implementing fully differential current buffers is introduced. Using the proposed method two high CMRR (Common Mode Rejection Ratio) and high PSRR (Power Supply Rejection Ratio) fully differential current buffers in BIPOLAR and CMOS technologies are implemented. Simulation results by HSPICE using 0.18µm TSMC process for CMOS based structures in 1.4V supply voltage and transistor models NUHFARRY and PUHFARRY for BJT based one in 1.6V supply voltage show CMRR of 32.9dB and 33.1dB for CMOS based and BJT based fully differential current buffers respectively. The proposed fully differential current buffers show PSRR- of 114dB and 116dB in CMOS and BIPOLAR technologies respectively while their PSRR+ are 100dB and 109dB respectively. The proposed common mode separation technique can also be arranged in partial positive feedback configuration to provide high current gain too. Simulation results of this configuration in CMOS technology, show current gain and CMRR of 20.86dB and 53.91dB respectively. The proposed method tends to be a fundamental technique in current mode signal processing capable to be much further improved and utilized. Favorably, corner case simulation results of the proposed structures prove their robustness against technology process.

Keywords Common Mode Separation Technique, Fully Differential Current Buffer, Fully Differential Operation, High CMRR Current Input Stage, High PSRR, Low Voltage Design.

چکیده این مقاله روشی جدید را برای جداسازی سیگنال‌های حالت مشترک جهت پیاده‌سازی بافرهای جریانی تمام تفاضلی معرفی می‌نماید. با استفاده از روش پیشنهاد شده بافرهای جریانی تمام تفاضلی با نرخ حذف حالت مشترک بالا و نرخ حذف منبع تغذیه بالا در دو تکنولوژی دوقطبی و CMOS ارائه می‌شوند. مدارهای ارائه شده در تکنولوژی CMOS با استفاده از پارامترهای فرایند ۰/۱۸ میکرومتر TSMC و مدارهای ارائه شده در تکنولوژی دوقطبی با استفاده از مدل ترانزیستورهای NUHFARRY وPUHFARRY و با کمک نرم افزار HSPICE طراحی و شبیه‌سازی شده‌اند. ولتاژ تغذیه استفاده شده برای مدارهای طراحی شده در تکنولوژی های دوقطبی و CMOS بترتیب برابر ۱/۶ ولت و ۱/۴ ولت می‌باشد. بافرهای جریانی کاملاً تفاضلی طراحی شده نرخ حذف حالت مشترک ۳۲/۹ dB و ۳۳/۱ dBرا بترتیب درتکنولوژی های CMOS و دوقطبی ارائه می-دهند. نرخ حذف منبع تغذیه منفی آنها نیز بترتیب برابر ۱۱۴ dB و ۱۱۶ dB و نرخ حذف منبع تغذیه مثبت نیز برابر ۱۰۰dB و ۱۰۹ dB بترتیب برای تکنولوژی های CMOS و دوقطبی می‌باشد. روش حذف حالت مشترک معرفی شده همچنین می‌تواند برای تامین بهره جریانی بالا در ساختار فیدبک مثبت جزئی بکار رود. نتایج شبیه‌سازی در تکنولوژی CMOS برای این حالت، نرخ حذف حالت مشترک ۵۳/۹۱dB و بهره جریانی۲۰/۸۶ dB را نشان می‌دهد. نتایج شبیه‌سازی در گوشه‌های چهارگانه نیز مقاومت خوب مدارهای پیشنهادی را در مقابل خطاهای ناشی از فرآیند تکنولوژی به اثبات می‌رساند. روش ارائه شده یک روش بنیادی در پردازش حالت جریان می‌باشد که قابلیت بهبود و گسترش زیادی دارد.

1. INTRODUCTION

An analog circuit design using the current mode approach has recently gained considerable attention. High slew rate, high bandwidth, simple circuitry and low voltage operation are some advantages of

current mode circuits compared to voltage mode ones [1-3]. Low voltage operation of current mode circuits has gained more importance due to semiconductor technology down scaling and reliability issues [4]. This scaling has also led to the popularity of mixed-signal design in System-on-Chips (SOCs) which analog and digital circuits are assembled on one chip. Thus, along with low voltage operation, analog designers have to concern about power and ground fluctuations caused by the switching of the digital portion of mixed analog-digital circuits. As a result low voltage current mode structures with high PSRR and high CMRR which are able to suppress power and ground coupled noise as well as unwanted common mode signals are critically needed.

Current buffers are main building blocks of current mode signal processing circuits. Their main characteristics are low input impedance, high output impedance and a current gain of unity. A few application examples are as follows:

1- They are used to isolate the on-chip circuitry from the large parasitic capacitances at the chip input pads to allow taking full advantage of the speed capabilities of the current-mode circuits [5].
2- Voltage mode circuits can be converted to their current mode counterparts using Adjoint network theorem based on current buffers [6-7].
3- Current buffers are used in high bandwidth data communication applications [8-9].
4- Various types of filters and oscillators can be implemented using current buffers [10-11].
5- Current buffers are used at the input stage of most current mode circuits especially current mode amplifiers [12-13].

As fully differential signal processing is commonly used in many fields mainly because of its inherent immunity to common mode signals, clock feed through, interferences and other types of common mode disturbances [1, 14-15], a fully differential current buffer is more beneficial especially in the case of Mixed Mode designs.

The most popular types of current buffers are common gate (CG) in CMOS technology, common base (CB) in BJT technology [8, 16-17] and various types of current mirrors which are employed in current mode circuits [18-20]. The second-generation current conveyor (CCII) can also be used as current buffer [21]. Unfavorably due to the employment of voltage-mode followers, such current buffers lose most of the potentials of current mode signal processing. A common problem in all above mentioned current buffers is that they are in single input single output arrangement and therefore their output currents are sensitive to all types of unwanted input signals and disturbances.

In [22-23] common mode feedback (CMFB) has been used to design fully differential current buffers based on CB and CG stages. Common mode feedback applied on CB stage in [22] has resulted in a current gain of -12dB and CMRR of 28dB. Low current gain and the need for additional current mirrors (to subtract the 'upper' and 'lower' output collector currents to provide a balanced high impedance differential output) which further increase chip area and power consumption are major drawbacks of current buffer reported in [22]. It is also in BJT technology and requires very large supply voltage. The CMFB based fully differential current buffer reported in [23] needs fully balanced inputs which limits its application. On the other hand in the structures including CMFB, stability conditions should be maintained which complicates the design procedure [24-25].

The orderly current buffer (OCB) introduced in [26] has fully differential structure based on CB stage. It achieved high CMRR and fully differential operation employing a novel negative feedback based technique. Unfavorably it has high power consumption (6.7mW or larger) and its stability conditions should be considered in the design procedure. On the other hand, it is implemented in BICMOS technology which is very expensive.

Three fully differential current buffer topologies were reported in [27]. In these topologies multiple current buffers were used to subtract input signals as is shown in Fig.1. Some drawbacks of these topologies are; increased power consumption and chip area, unbalanced input impedances (in Fig.1-a), lower output impedance (in Fig.1-b), needing tight matching between current buffers (especially in Fig.1c).

Properly connected current mirrors along with common gate stage can also be used to design fully differential current buffer [28]. In this approach, matching between P type and N type current mirrors are very difficult. Mismatching between current

mirrors results degraded CMRR and PSRR for fully differential current buffers employing this approach. Although the method used in [7, 29-30] for designing fully differential current buffers was successful in reducing common mode currents, however it produced CMRR which is very sensitive to the transistors parameters.

Due to the increasing importance of fully differential structures, in this work a new common mode separation technique is introduced to design high CMRR fully differential current buffers. In the proposed method, a common mode separation circuit is connected in parallel with CG or CB current buffers input terminals which act in a way that provides a low impedance path to ground for unwanted common mode inputs preventing them to flow through the main current mode circuit. On contrary, this novel circuit has very high input impedance for differential mode inputs thus facilitates these inputs to reach the current buffer output terminals. As in the proposed approach common mode signals are separated from differential mode ones, we call it 'common mode separation technique'. The interesting property of this method is that in the case of common mode signals it provides both a low impedance path to ground and high input impedance through the main body of current buffer. This double action doubly rejects common mode signals. It is worth nothing that unlike some of the previously used methods, the proposed method does not need balanced inputs for proper operation. This feature thus, both In section II basic concept of the proposed idea is described and two fully differential current buffers based on CG and CB stages are presented. Section III includes the proposed high current gain stage. Simulation results are presented in section IV and finally section V concludes this paper.

2. PROPOSED FULLY DIFFERENTIAL CURRENT BUFFERS

2.1. Implementation of Common Mode Separation Circuit Conceptual schematic of the proposed idea is shown in Fig. 2a. To separate differential mode input signals from unwanted common mode ones, the proposed common mode separation circuit is connected to inputs of current mode circuit in parallel. In the case of common mode inputs as is shown in Fig. 2 b, it opens a low

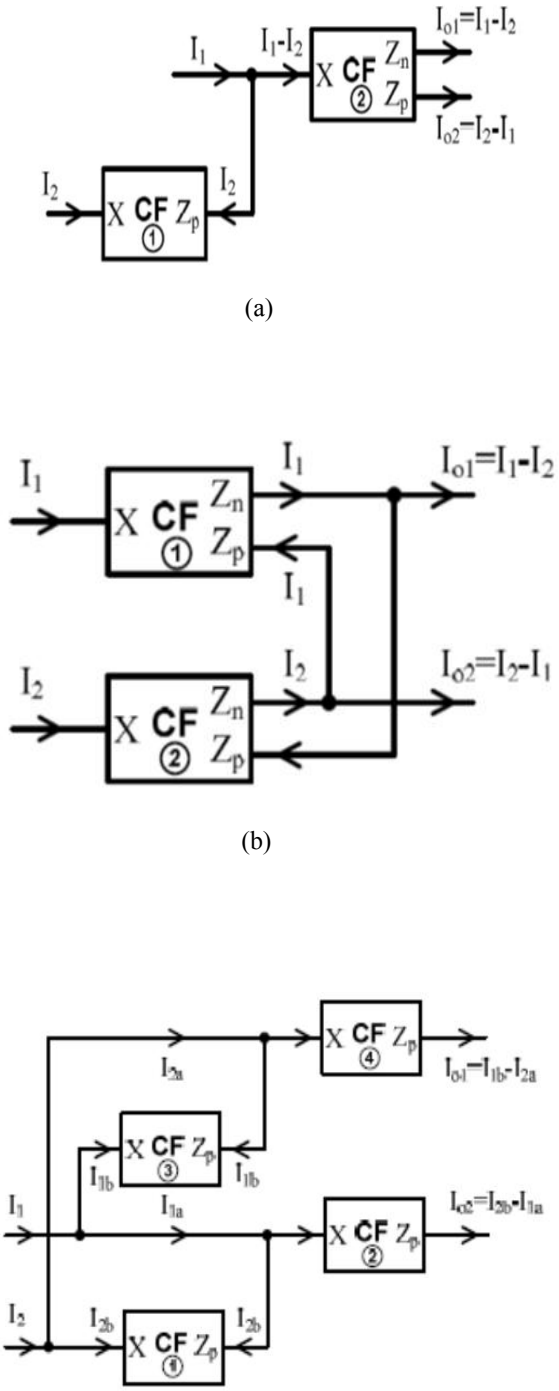

Figure 1. Fully differential current buffer topologies using single input-single output current buffers [27]

impedance path to ground for common mode currents. But in the case of differential mode inputs common mode separation circuit provides a high input impedance and differential mode input currents are directly conducted to the output of the main current mode circuit as is shown in Fig. 2c. Common mode separation circuit can be implemented using either CMOS or BJT transistors. It can also be applied to both CG and CB stages as will be shown next in this section.

Implementation of common mode separation circuit in CMOS technology is shown in Fig. 3 which can be implemented in BIPOLAR technology in the same way. It consists of M_1-M_2 differential pair, M_5 level shifter and M_3-M_4 NMOS transistors. Voltage at the source node of differential pair, i.e. K node, plays an important role in the operation of the proposed common mode separation circuit. In the case of differential mode inputs, voltage at node K will be at virtual ground due to the M_1-M_2 differential pair action. This will make M_3-M_4 NMOS transistors gate voltages, i.e. KK node, at virtual ground (via M_5 level shifter) and their differential mode drain currents equal to zero. Since source nodes of M_3-M_4 transistors are connected to V_{SS}, the gate-source small signal voltages of those transistors become zero too. As the result, a high impedance (equal to the output impedance of M_3-M_4 transistors i.e. $ro_{3,4}$) path is provided for differential mode currents which allows only a negligible portion of differential mode input currents to be drown by common mode separation circuit, leaving ideally the whole differential input currents to get the output terminals of current buffer.

In the case of common mode inputs, voltage at node K will be roughly equal to input nodes voltages i.e. $V_A=V_B=V_K$. This is mainly due to the voltage tracking action of M_1-M_2 differential pair. Equality of input terminals voltages with node K voltage (and node KK voltage) implies that gate-drain voltage of M_3-M_4 NMOS transistors is equal to zero. Hence M_3-M_4 transistors act as diode connected transistors providing a low input impedance path of $1/gm_{3,4}$ for common mode currents in which $gm_{3,4}$ is transconductance of M_3-M_4 transistors. As a result in the case of common mode inputs, M_3-M_4 transistors directly conduct the

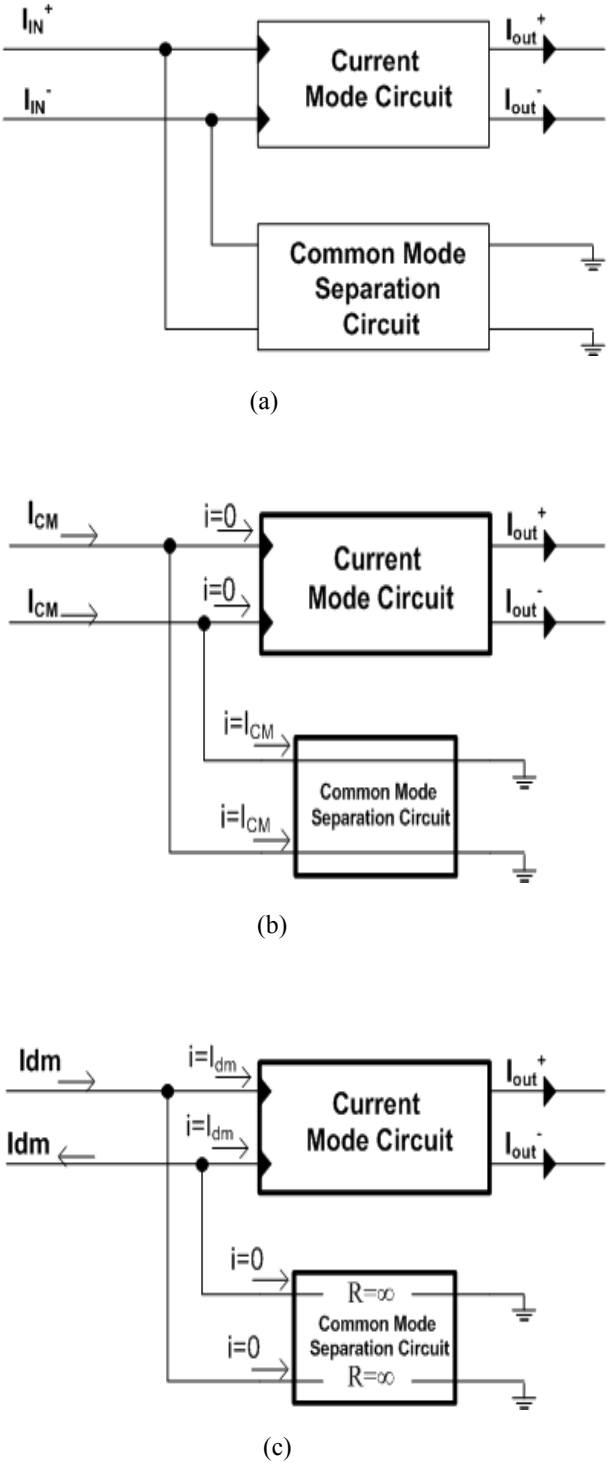

Figure 2. Conceptual schematic of the proposed idea a) basic form b) in common mode configuration c) in differential mode configuration

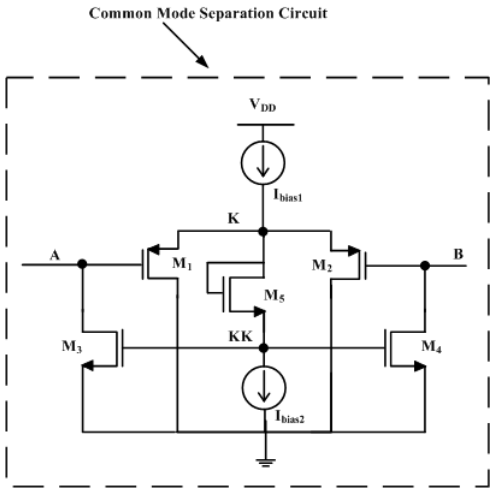

Figure 3. Implementation of common mode separation circuit in CMOS technology

input common mode currents to ground, allowing ideally, zero common mode current to get the output terminal of current buffer.

In Figures 5 and 6 the proposed common mode separation circuit is applied to CG and CB stages respectively to separate differential mode currents from unwanted common mode ones in order to design a fully differential current buffer.

2.2. Fully Differential Current Buffer Design Based on Common Mode Separation Technique Fig. 4 shows two CG stages which were conventionally used to process differential signals. In this configuration M_{N1}-M_{N2} are common gate transistors biased through I_{bias} current sources and M_B transistor. Current mirrors M_{m1}-M_{m2} and M'_{m1}-M'_{m2} transfer the input signals to the loads. In this configuration, both unwanted common mode currents and differential mode ones are transferred to the loads resulting in a CMRR of zero dB for the current buffer of Fig. 4.

The proposed fully differential current buffer is shown in Fig. 5. It is constructed by adding the proposed common mode separation circuit of Fig. 3 to the inputs of conventional current buffer of Fig. 4. It utilizes M_{N1}-M_{N2} CG stages and common mode separation circuit implemented with M_1-M_5 transistors. Favorably M_3-M_4 transistors of the common mode separation circuit are also used to bias M_{N1}-M_{N2} transistors. The gate nodes of M_{N1}-M_{N2} are connected to K node of the common mode separation circuit. Interestingly the proposed fully differential current buffer of Fig. 5 has only three more transistors compared to conventional one of Fig. 4.

It is convinent to expalin the operation of the proposed fully differential current buffer of Fig. 5 by defining input signals (Iin^+ and Iin^-) in terms of their common mode and differential mode componenets as:

$$Iin^+ = \frac{Id}{2} + I \quad (1)$$

$$Iin^- = -\frac{Id}{2} + Ic \quad (2)$$

Where:

$$Ic = \frac{Iin^+ + Iin^-}{2} \quad (3)$$

$$Id = Iin^+ - Iin^- \quad (4)$$

In the case of common mode inputs where $Iin^+ = Iin^- = Ic$, the input terminals' voltages are equally propotional to input common mode currents, i.e. $V_A = V_B = \alpha Ic$. Due to voltage tracking action of M_1-M_2 differential pair, voltge at node K will be rougly equal to the input terminals voltages i.e. $V_K = V_A = V_B$. This implies a zero gate-source voltage for M_{N1}-M_{N2} transistors in common gate stages. As expalined earlier, in the case of common mode inputs, M_3-M_4 gate-drain voltages are also equal to zero turning these transistors to diode connected ones which provide a low impedance path of $1/gm_{3,4}$ to ground for common mode currents. As a result drain current of M_3-M_4 is equal to common mode input currents and due to zero gate-source voltage of M_{N1}-M_{N2}, their common mode drain current will be zero. On the other hand, M_{N1}-M_{N2} transistors in common gate stages have zero gate-source voltage and show high output impedance of ro_N for common mode currents in which ro_N is output impedance of M_{N1}-M_{N2} transistors. Common mode gain of fully differential current buffer of Fig. 4 can be found from:

$$A_C = [(1-a)gm_{N1,N2} + \frac{1}{1+gm_{3,4}.ro_N}] \quad (5)$$

where, $gm_{N1,N2}$ and ro_N are transconductance and output resistance of M_{N1}-M_{N2} transistors respectively and "a" is common mode voltage gain between input terminals (i.e. A and B) and node K which can be represented as:

$$a = \frac{2\,gm_P.(R_{Ibias_1} \| R_{Ibias_2})}{1 + 2.gm_P.(R_{Ibias_1} \| R_{Ibias_2})} \qquad (5\text{-}1)$$

In which, gm_p is M_1-M_2 transistors transconductances, R_{Ibias1} and R_{Ibias2} are equivalent output resistances of I_{bias1} and I_{bias2} current sources respectively.

In the case of differential mode inputs (Iin^+=-Iin^-=0.5Id), M_1-M_2 differential pair makes node K to be at virtual ground. As is explained before for Fig. 3, M_3-M_4 transistors show high impedance of $ro_{3,4}$ for differential mode input signals. Hence a negligible portion of differential mode input currents will flow into M_3-M_4 transistors via $ro_{3,4}$. On the other hand, gate terminal of M_{N1} and M_{N2} transistors will be at virtual ground while their source nodes are at V_B and V_A respectively making gate-source voltage of M_{N1} and M_{N2} equal to $-V_B$ and $-V_A$ respectively. As a result M_{N1}-M_{N2} will performe as simple CG stages providing low impedance paths of $1/gm_{N1,N2}$ to outputs (in which $gm_{N1,N2}$ are transconductances of M_{N1}-M_{N2} transistors) for differential mode input signals. Differential mode gain of the proposed buffer can thus be found from:

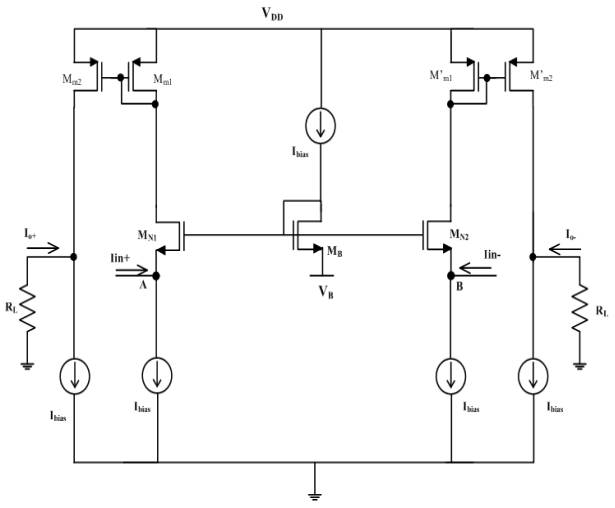

Figure 4. Conventional fully differential CG based current buffer

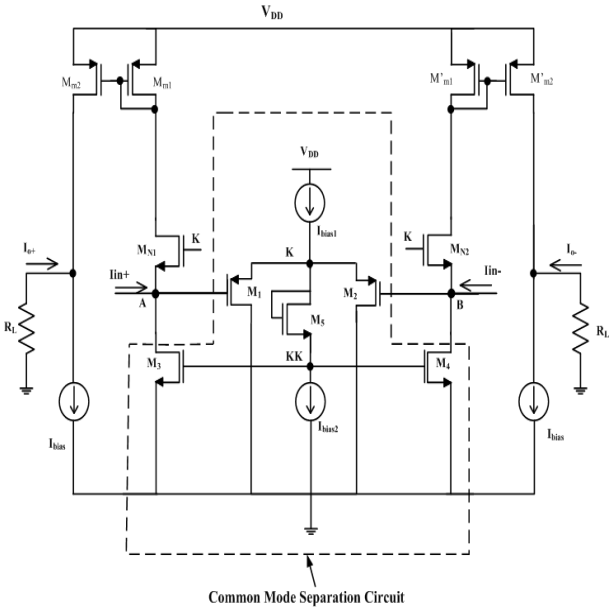

Figure 5. Proposed fully differential current buffer in CMOS technology

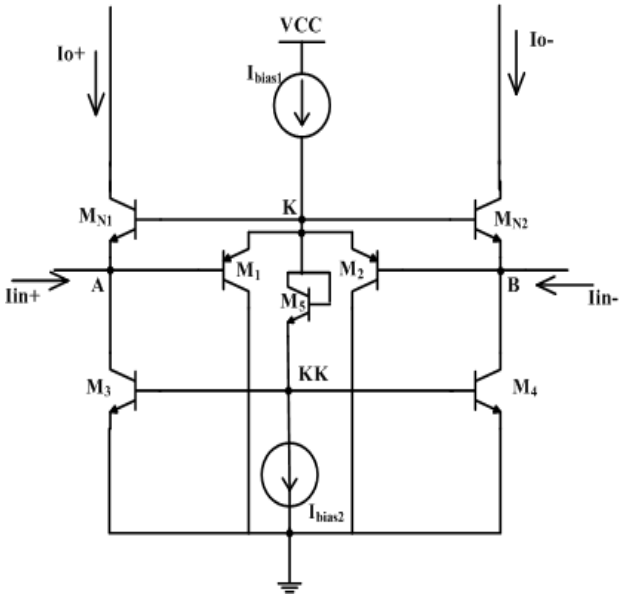

Figure 6. Proposed fully differential current buffer in BIPOLAR technology

$$A_D = \frac{gm_{N1,N2}.ro_{3,4}}{1+gm_{N1,N2}.ro_{3,4}} \quad (6)$$

Using (5) and (6), the resulted CMRR for the proposed current buffer will be as:

$$CMRR = \frac{A_D}{A_C} = \frac{gm_{N1,N2}.ro_{3,4}.(1+gm_{3,4}.ro_{N1,N2})}{[(1-a)gm_{N1,N2}.(1+gm_{3,4}.ro_{N1,N2})+1](1+gm_{N1,N2}.ro_{3,4})} \quad (7)$$

Assuming, a≈1 and $gm_{N1,2}.ro_{3,4}>>1$ simplifies CMRR as:

$$CMRR = ro_{N1,N2}.gm_{3,4} \quad (8)$$

Fig. 6 shows the BJT version of the fully differential CB stage implemented with common mode separation technique. In this structure, M_{N1}-M_{N2} along with M_3-M_4 transistors forms the common base stages and the proposed common mode separation circuit is formed with M_3-M_4 NMOS transistors, M_1-M_2 differential pair and M_5 level shifter. The operation of this circuit is the same as its CMOS counterpart. Note that for simplicity, load current mirrors are not shown.

2.3. Common Mode Separation Technique in Partial Positive Feedback Configuration The proposed common mode separation technique can be arranged in a partial positive feedback configuration to provide a high differential current gain and higher CMRR and PSRR. This configuration in CMOS technology is shown in Fig. 7. As is shown in Fig.7, in this structure, the gates of M_3-M_4 NMOS transistors in common mode separation circuit are directly connected to the input nodes (instead of node KK in Fig.3) and gates of common gate NMOS transistors (M_{N1}-M_{N2}) are connected to the source node of differential pair (M_1-M_2) i.e. K node. For simplicity, PMOS current mirrors and loads are not shown.

In the case of common mode inputs, both input nodes have equal voltage i.e. $V_A=V_B=V_C$, so the drain-gate terminals of M_3-M_4 NMOS transistors are short circuited and hence these transistors act as diode connected transistors providing a low impedance path to ground for common mode signals. Meanwhile, voltage of node K is approximately equal to the input node's voltages because of the voltage tracking action of differential pair (M_1-M_2) in common mode separation circuit. So the gate-source of M_{N1}-M_{N2} transistors will be zero and negligible common mode current will flow into these transistors through their output impedances.

The proposed structure of Fig. 7 has a very interesting operation in the case of differential mode inputs. In this mode, gates of M_{N1}-M_{N2} transistors become virtual grounded (because these nodes are directly connected to the source of M_1-M_2 differential pair which is at virtual ground in differential mode) so these transistors will act as simple common gate stages with input resistance of $1/gm_{N1,N2}$ but M_3-M_4 NMOS transistors establish a partial positive feedback loop which can be used to produce both high gain and high CMRR. It can be proved that the differential mode current gain due to partial positive feedback can be found from:

$$Aid = \frac{\frac{gm_{3,4}}{gm_{N1,N2}}}{1-(\frac{gm_{3,4}}{gm_{N1,N2}})} = \frac{\eta}{1-\eta} \quad (9)$$

As stated in [31-32], by proper choosing of η so that $0<\eta<1$, a high gain and stable current input stage can be obtained. Using (9) the CMRR of the proposed circuit of Fig.7 becomes as:

$$CMRR \approx ro_{N1,N2}.gm_{3,4}.\frac{n}{1-\eta} \quad (10)$$

As can be seen from (10), structure of Fig.7 has higher CMRR compared to proposed current buffers.

3. SIMULATION RESULTS

To verify the potentials of the proposed common mode separation technique, proposed fully differential current buffers of Figs. 5 and 6 along with high current gain stage of Fig.7 are designed and simulated by HSPICE using 0.18μm CMOS process parameters for MOS based structures and transistor models NUHFARRY and PUHFARRY [33] for BJT based one. The used bias currents and voltages are shown in Table1. Transistors aspect ratios in CMOS based circuits are also presented in

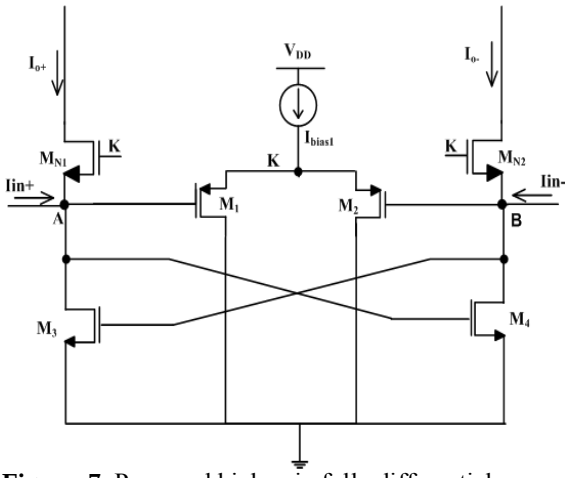

Figure 7. Proposed high gain fully differential current input stage

Table 2. Those are so chosen to get the best possible and reliable results following relations (5) through (10). As in the case of Fig. 5, output currents of the proposed circuits in Figs. 6 and 7 are transferred to the loads using simple current mirrors. In the CMOS based structures, used aspect ratios in all current mirrors and current sources are 50μm/0.5μm. The used load in the simulations is a 1kΩ resistor parallel with 1pF capacitor. In practice, the CB block is mostly used in current mode processing where the impedance of the output node is so low that acts dominantly resistive.

TABLE1. Used bias currents and voltages

	V_{DD} (V)	V_{CC} (V)	I_{bias1} (μA)	I_{bias2} (μA)
Current Buffer of Fig.5	1.4	-	10	5
Current Buffer of Fig.6	-	1.6	50	5
high gain stage of Fig.7	1.4	-	10	-

TABLE 2. Transistors aspect ratios

	Transistor	W(μm)/L(μm)
Current Buffer of Fig. 5	M_1-M_2	3.5/0.5
	M_3-M_4	45/0.5
	M_5	10/0.5
	M_{N1}-M_{N2}	10/0.5
High current gain stage of Fig. 7	M_{N1}-M_{N2}	30/0.5
	M_1-M_2	4.5/0.5
	M_3-M_4	20/0.5

Current gain (Ai) frequency performance of the proposed structures are shown in Fig. 8 which show current gains of -0.2dB and -0.53dB for the proposed current buffers of Fig.5 and Fig.6, respectively. This implies that common mode separation circuit takes a negligible portion of differential mode currents causing its large portion to be flown through CB and CG stages. Proposed common mode separation circuit has also successful operation in partial positive feedback configuration which results a current gain of 20.86dB for the proposed current gain stage of Fig. 7. The -3dB frequencies are 144MHz and 49.7MHz for the proposed CMOS based and BJT based current buffers, respectively. High current gain stage has also a high -3dB frequency of 80.3MHz.

Fig. 9 shows CMRR frequency performance of the proposed structures. It proves successful operation of the proposed common mode separation technique in alleviating common mode inputs. The resulted CMRR are 32.9dB, 33.1dB and 53.91dB for the CMOS based current buffer of Fig. 5, BJT based current buffer of Fig.6 and CMOS based current gain stage of Fig. 7, respectively. The frequencies at which CMRR approaches 0dB are 675MHz, 385MHz and 3700MHz for the CMOS based current buffer of Fig. 5, BJT based current buffer of Fig. 6 and current gain stage of Fig. 7, respectively. These results prove the great strength of the proposed common mode separation technique in eliminating high frequency unwanted common mode signals.

Stability of the proposed current gain stage is investigated by applying a step input with amplitude of ±1μA. The resulted outputs are shown in Fig. 10 which prove its sufficient stability.
To examine the ability of the proposed circuits in rejecting supply and ground coupled noises, their PSRR performance are also investigated. Results are shown in Fig. 11 which show high PSRR for the proposed structures.

Simulation results are summarized in Table 3. The reported power dissipation also includes the bias circuitry that consists simple (two transistors) current sources and consumes very few power.
Corner case simulation results are also studied and reported in Table 4 which shows a robust performance for the proposed current buffers.

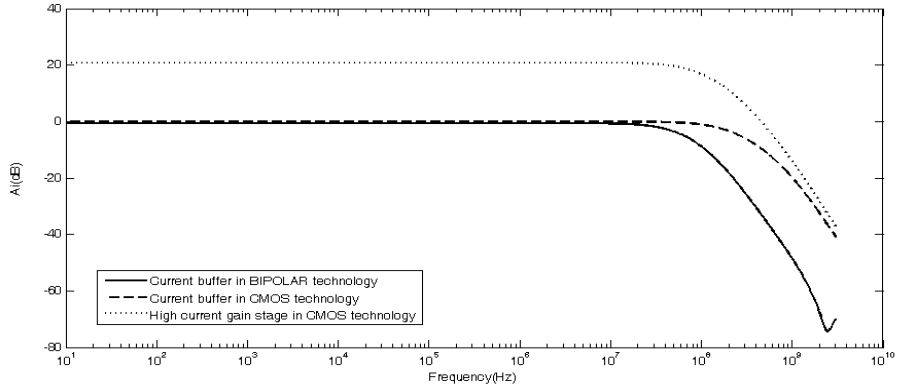

Figure 8. Ai frequency performance of proposed structures

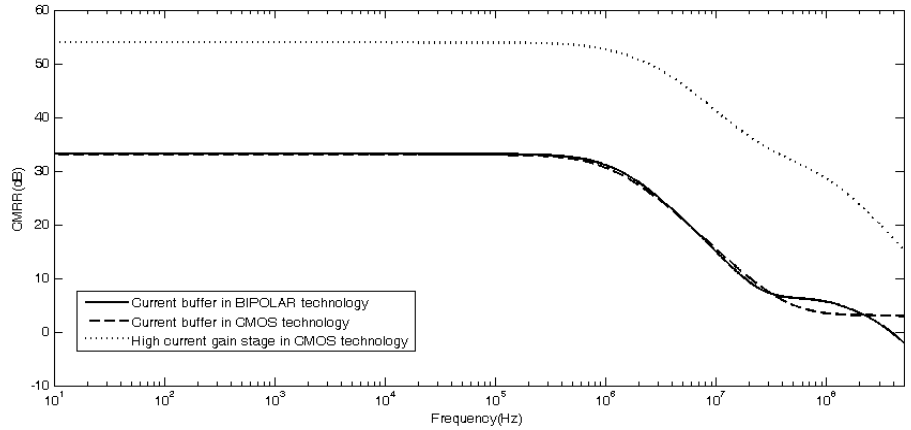

Figure 9. CMRR frequency performance of proposed structures

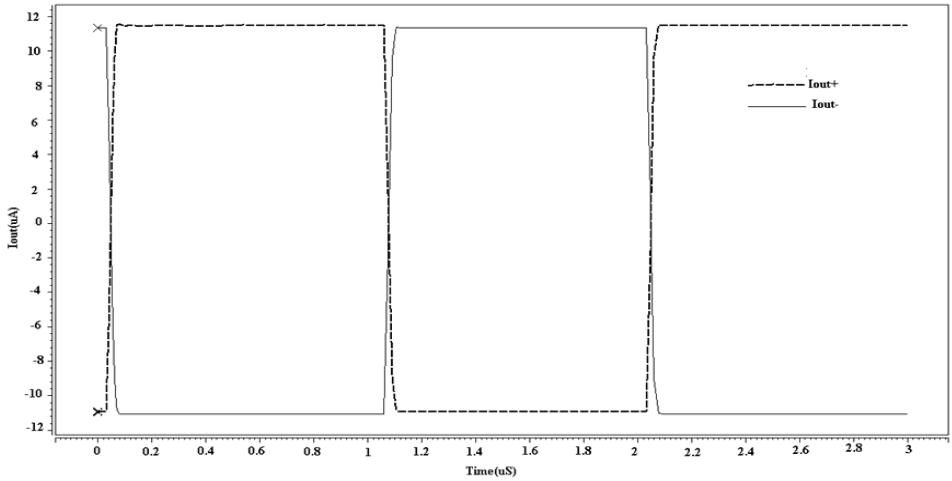

Figure 10. Step response of high current gain stage

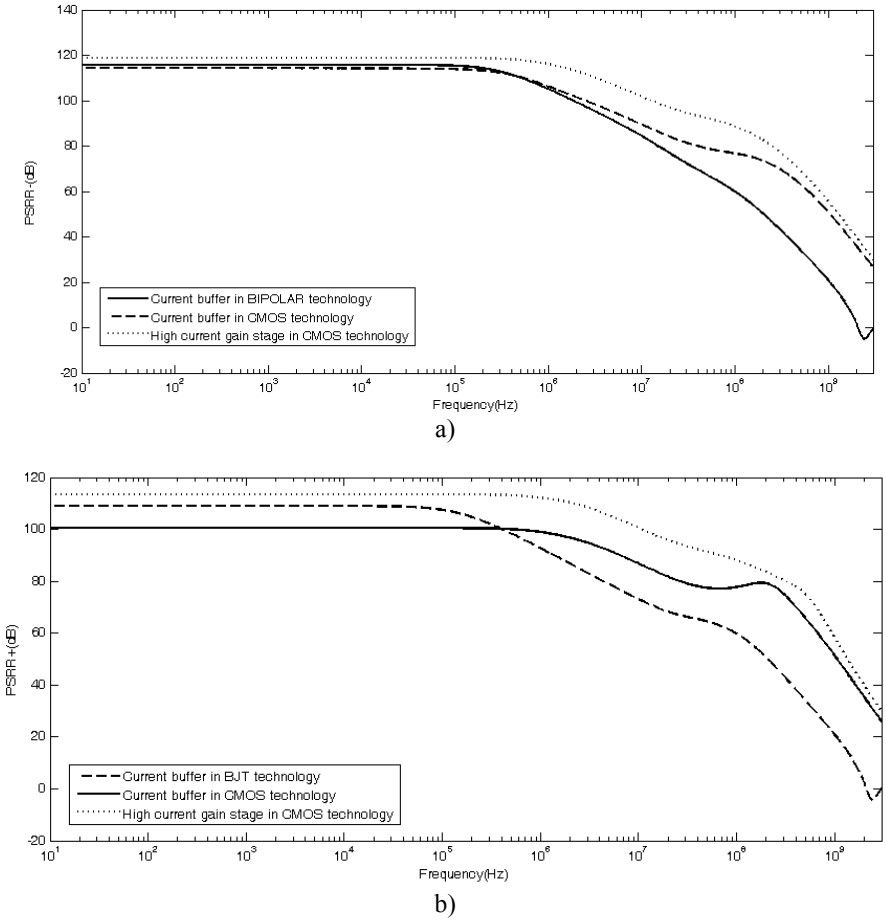

Figure 11. PSRR frequency performance of proposed structures a)PSRR- b)PSRR+

TABLE 3. Proposed Current Buffers (CB) and high current gain stage specifications

	Proposed current buffer		High Current Gain Stage
	In CMOS	In Bipolar	
Ad(dB)	-0.2	-0.54	20.86
f-3dB (MHz)	144	49.7	80.3
CMRR(dB)	32.9	33.1	53.91
f_T of CMRR (at which CMRR=0dB)	675MHz	385Mhz	3700MHz
PSRR-(dB)	114	116	118.85
PSRR+(dB)	100	109	113.50
$P_D(\mu W)$	179	379	305

TABLE 4. Corner case simulation results of the proposed Current Buffre(CMOS) and high current gain stage specifications

		CMOS CB	High Current Gain Stage
Ad(dB)	SS	-0.16	25.5
	FS	-0.48	5.33
	SF	0.38	29.2
	FF	-0.01	20.4
f-3dB (MHz)	SS	175M	259M
	FS	384M	47.7M
	SF	370M	90.7M
	FF	196M	43.4M
CMRR(dB)	SS	27.2	48.8
	FS	19.1	16.4
	SF	32.9	65.9
	FF	33.6	55.8
f_T of CMRR (at which CMRR=0dB)	SS	10GHz	3.5GHz
	FS	10GHz	4.7GHz
	SF	608MHz	337MHz
	FF	7.7GHz	3.5GHz

Simulation results of the proposed current buffers are compared with other related works in Table 5. As can be seen, the proposed current buffers offer low voltage operation compared to others. The BJT version of the proposed current buffer also has very low power consumption compared to other BJT based current buffers while that of CMOS version is much less than other CMOS types and comparable with that of the best one (to be notified that the consumed power reported for [29] excludes the power of bias circuitry which is some tens micro watts).

4. CONCLUSION

This paper proposes a novel method to design fully differential current buffers. In the proposed method, common mode currents are conducted to ground while differential mode ones are forwarded to the output loads. It is thus called Common Mode Separation technique. The proposed technique combined with partial positive feedback is used to design low power and low voltage high gain current input stages.

TABLE 5. Comparison of the proposed current buffers with other related works

Refs.	Technology	Ad		CMRR	Supply Voltage	Power dissipation	Year
		Value (dB)	f-3dB (MHz)				
[22]	BJT	-12dB	NA	52dB	NA	NA	1990
[23]	CMOS	-6.02dB	>37MHz	38dB	5V	22mW	1998
[26]	BJT	66mdB	831MHz	55dB	±1.5V	6.7mW	2010
[27]	CMOS	NA	57MHz	50dB	±1.5V	NA	2009
[28]	CMOS	6dB	1.25MHz	62dB	5V	3mW	1991
[29]	CMOS	0.1dB	369MHz	98dB	±0.75V	0.135mW	2010
proposed	CMOS	0.172dB	144MHz	32.9	1.4V	0.179mW	2011
	BJT	-0.54dB	49.7Mhz	33.1	1.6V	0.379mW	2011

Based on the proposed method, two fully differential current buffers and a high gain current input stage are introduced and simulated presenting a sufficiently high CMRR and PSRR. Simplicity is another important characteristic of the proposed method. There is no need to concern about stability conditions in the proposed structures. Compared to conventional current buffers, the proposed one has only three more transistors while offering high CMRR and true fully differential operation. This technique is at the beginning of its life and is gifted much more capabilities to be opened and improved by further attentions of interested researchers.

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