A NOVEL STRUCTURE FOR REALIZATION OF A PSEUDO TWO PATH BAND-PASS FILTER

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Abstract In this paper, a modified auto zeroed integrator is used to design and simulate a low-voltage high-Q switched capacitor pseudo 2-path filter. The filter is a sixth–order Chebyshev band-pass filter operating at sampling frequency of 1MHz and center frequency of 250 kHz with a quality factor of 50. The proposed filter has both low-voltage and high speed properties of the auto zeroed integrators and accurate center frequency of N-path band-pass filters. The operating voltage is 1.5v with no use of voltage bootstrapper circuit. Simulation is done using HSPICE and 0.25µm CMOS technology.

Keywords Auto Zeroed Integrator, Switched-capacitor, Pseudo-2-path Filter, Ladder Filters.

چکیده در این نوشتار یک فیلتر شبه دو مسیره سوییچ‌خازنی ولتاژ پایین با ضریب کیفیت بالا با استفاده از انتگرال‌گیر خود صفر شونده بهینه‌شده طراحی و شبیه‌سازی شده است. فیلتر فوق، یک فیلتر میان‌گذر درجه ششم چبی‌شف است که در فرکانس ساعت یک مگاهرتز کار می‌کند. فیلتر پیشنهادی هم دارای خواص ولتاژ پایین و سرعت بالای مدارات مجهز به انتگرال‌گیر خود صفر شونده است و هم از دقت بالای فیلترهای چند مسیره در تحقق فرکانس مرکزی بهره می‌برد. فرکانس مرکزی این فیلتر ۲۵۰ کیلوهرتز و ضریب کیفیت آن ۵۰ است. فیلتر فوق در ولتاژ تغذیه ۱/۵ ولت و بدون استفاده از مدارات بوت استراپ برای بالا بردن ولتاژ کار می‌کند. شبیه‌سازی با استفاده از نرم افزار اسپایس و تکنولوی ۰/۲۵میکرو متر انجام شده است.

1. INTRODUCTION

Widespread usage of portable electronic system designs have resulted to inevitable use of low-voltage, low-power analog integrated circuits. In addition, designing an accurate and high frequency circuit in a low-voltage application is a complicated procedure.

The fine accuracy of switched capacitor (SC) circuits and particularly SC filters are well known [1]. However, the Q factor and the operating frequency of the SC filters lack the required specification of many desired circuits. In the process of filter design, cascading method is not an appropriate solution for high Q circuit due to its sensitivity to the capacitive variations. The well known characteristic of the ladder filter is its less pronounced effect on the above problem [2].

The main difficulty of low-voltage SC circuit design is the driving voltage of the input CMOS switches. Two conventional approaches for low-voltage SC design, using standard CMOS technologies, are currently implemented. The first is bootstrapping method [3] which generates higher voltages to drive the gate of input switches, although the existence of on-chip high voltages is not recommended for deep-submicrometer CMOS processes [4].The second is switched-opamp method [5,6], where the switching action is done by a switched opamp. This method is a real low-

voltage solution in SC circuits, but it is not suitable for high-speed SC circuit applications because of turning on/off time of the opamp. This shortcoming of the switched opamp is reduced by the application of an auto-zeroed integrator (AZI). The low voltage, high frequency application of AZI for SC circuits was reported [7] where the basic AZI circuit [8] was modified for this purpose. Power consumption and settling time of the previous AZI circuit were improved as reported by Rashtian et al. [9]. The improved AZI (IAZI) circuit utilizes a two mode clock controlled opamp to reduce the power consumption and settling time of the AZI circuit by a current steering mechanism. Based on the IAZI [9], here the new $z \rightarrow -z^2$ block is presented. The $z \rightarrow -z$ transformation is a well known technique to transform a low-pass filter to a high-pass filter [2,10]. With respect to properties of SC filter frequency response, high-pass SC filter could be a band-pass filter with a center frequency of $f_{clk}/2$, but without sufficient nyquist range. Using a 2-path filter is a renowned method for spreading the nyquist range in this kind of circuits [11,12]. In this method, center frequency of band-pass filter only depends on the clock frequency and capacitor variations are eliminated.

In this paper, using the $z \rightarrow -z^2$ transformation, a third order low-pass ladder filter is transformed to a band-pass filter. In effect, the proposed filter has both low-voltage, high speed properties of IAZI circuits and fine accuracy of N-path structures. With respect to previous work [11] the proposed circuit has much higher sampling and center frequency while having approximately the same quality factor.

This paper is organized as follows. In section 2, the IAZI circuit and $z \rightarrow -z^2$ block are described. In section 3, the procedure for designing the band-pass filter is explained and finally in section 4 simulation results are presented.

2. A NEW $z \rightarrow -z^2$ INTEGRATOR BLOCK CONSTRUCTED BY IAZI

Figure 1 shows the basic differential AZI block where in the first phase (φ_1) both of $+V_{out}$ and $-V_{out}$ are set to V_{CM} and C_1 capacitors sample the inputs. In the next phase (φ_2), this circuit acts as an integrator. In general, the transfer function of AZI circuit is:

$$\frac{C_1}{C_{i1}} \frac{(z^{-\frac{1}{2}} - 1)}{1 - z^{-1}} \quad (1)$$

If the inputs come from another AZI with inverted clock phase, the altered transfer function is:

$$\frac{C_1}{C_{i1}} \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} \quad (2)$$

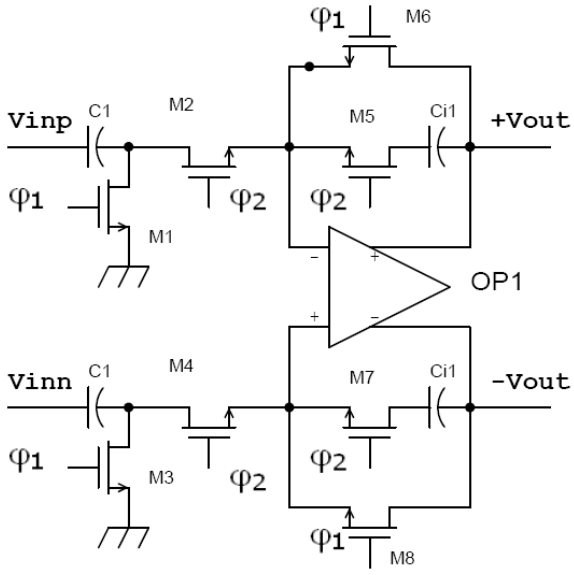

Figure 1. Basic auto zeroed integrator circuit.

In the AZI circuit of Figure 1, all switches are nMOS transistors whose sources are connected to the common-mode voltage V_{CM} and the gates are clocked by V_{DD} voltage. This is the reason that the charge injection and clock feed-through are not signal dependent and can be cancelled in a fully differential structure.

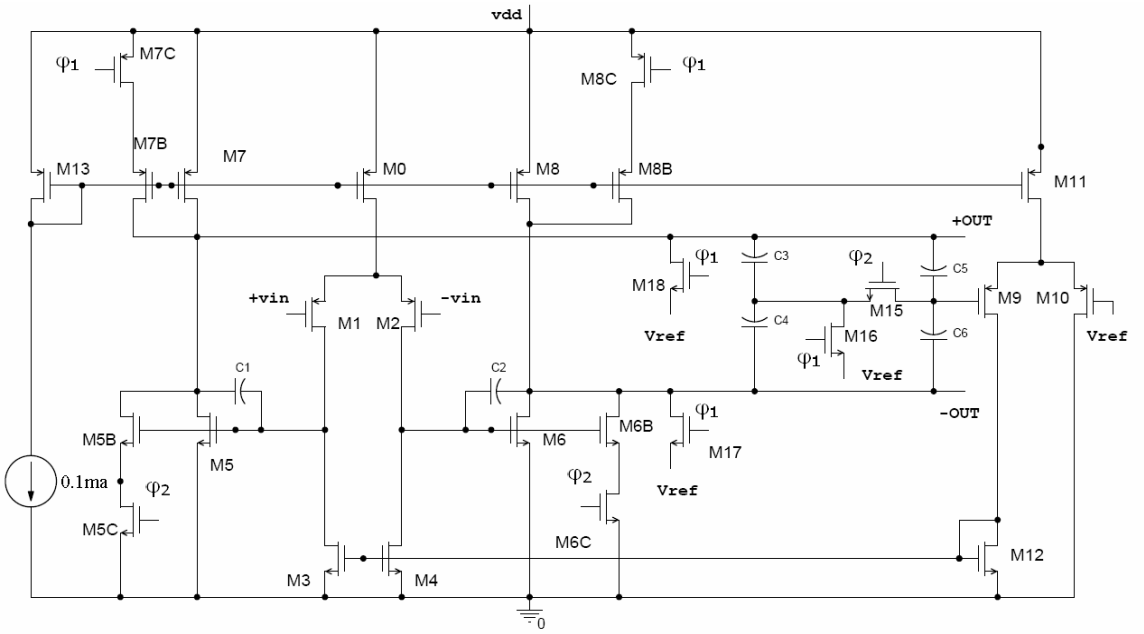

Figure 2. Pseudo switched op-amp presented by Rashtian [9].

In Figure 1, during phase (φ_1) the output and input of the op-amp are connected by switches (M6&M8) and the final value of the output voltage is a dc voltage (V_{CM}). Doing so, the linear action of the opamp is not critically essential and setting of the output voltage at V_{CM} can be done by external switches.

Based on the above idea, in the work done by Rashtian [9], a pseudo switched opamp with two current levels in the output stage is presented as shown in Figure 2 where the current steering action is done by transistors M_{5B}-M_{8B}. The W/L ratio of the current steering transistors is ten times greater than M_5-M_8. The current steering mode is controlled by transistors M_{5C}-M_{8C}. In the integration phase (φ_2), the output stage current is normal but in the other phase (φ_1), it is under low current condition. This can be called as a pseudo switched opamp configuration with an improved characteristic of power consumption without speed reduction characteristics of switched opamps. In the phase (φ_1) the output voltage is set to V_{CM} by the non-linear action of nMOS switches M_{17} and M_{18}.

Unlike the switched opamp technique, the nonlinear action of these switched transistors and the linear action of the opamp without current steering transistors i.e. (M_{5B}-M_{8B}) will result in the same final steady state value with reduced power consumption. As a result of the above, the nMOS switches M_{17} and M_{18} are only used to reduce the settling time. Transistors M_9, M_{10}, M15, M_{16}, and capacitors (C_3~C_6) make the common-mode feedback circuit. A detailed explanation of the opamp is also presented [7,9]. The opamp used in this work is the same as the opamp presented by Rashtian [9] but it is biased at lower current reference (0.1 mA) due to lower clock frequency.

Based on the IAZI idea, a new $z \rightarrow -z^2$ block is constructed as shown in Figure 3. Equation (3) shows the mathematical sequence in the time domain and equation (4) shows the z domain transfer function of this circuit if the input comes from the output of another IAZI block [13].

$$V_o(n+\frac{1}{2})T = \frac{C_{in}}{C_{A1}} V_i(n-1)T - \frac{C_{Bl}}{C_{A1}} V_o(n-\frac{3}{2})T \quad (3)$$

$$\frac{V_o(z)}{V_i(z)} = \frac{C_{in}}{C_{A1}} \frac{z^{-\frac{3}{2}}}{1+\frac{C_{Bl}}{C_{A1}} z^{-2}} \quad (4)$$

The sequence of clock phases (φ_1 , φ_2 ,φ_A and φ_B) has an important role in this structure. As it is

shown in Figure 3, the voltage effect of sampled input by C_{in} at (n-1)T appears on the C_{A1} capacitor at $\left(n+\frac{1}{2}\right)T$.

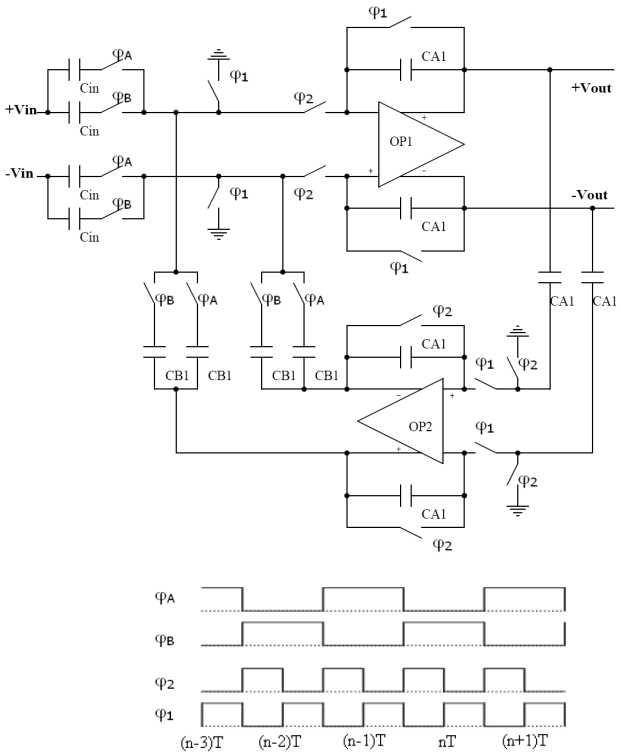

Figure 3. The main $z \rightarrow -z^2$ Block.

In general C_{B1} and C_{A1} are equal and the denominator of equation (4) would be $(1+z^{-2})$, which is a simple transformation of $z \rightarrow -z^2$ integrator. Based on this block, transformation of a low-pass ladder filter to a high-pass one is achieved by replacing the integrators of a low-pass filter by this block.

3. DESIGN PROCEDURE

In this paper, a pseudo-2-path band-pass filter with center frequency of 250 KHz and quality factor of 50 is presented. Based on a third order Chebyshev low-pass RLC filter with cut off frequency of 2.5 KHz which is shown in Figure 4, a low-pass ladder SC filter using IAZI is designed.

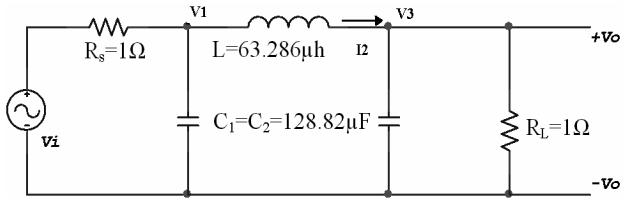

Figure 4. The 3th order Chebyshev low-pass RLC filter with cut off frequency of 2.5 KHz and 1db ripple in pass band.

The state space equations of Figure 4 are extracted from this circuit:

$$V_1 = \frac{1}{SC_1}\left(\frac{V_{in} - V_1}{R_S}\right) - I_2$$
$$I_2 = \frac{1}{SL}(V_1 - V_3) \qquad (5)$$
$$V_3 = \frac{1}{SC2}\left(I_2 - \frac{V_3}{R_L}\right)$$

Figure 5 is the state space diagram of the LPF filter attained by equation (5). Replacing the integrators in this figure with IAZI and utilizing the proposed input stage in [14], a third order low-pass SC filter is achievable, but here, we only replace the integrator blocks with $z \rightarrow -z^2$ SC block to construct a pseudo two path band-pass filter.

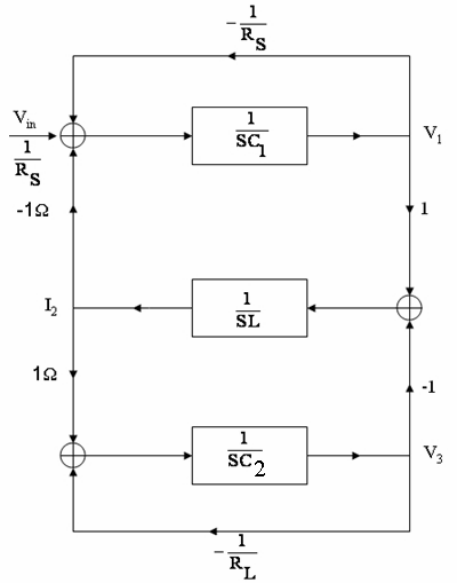

Figure 5. State space block diagram.

Figure 6 shows the schematic of the proposed band-pass filter that is resulted from substituting the integrators and resistors of Figure 5 by $z \rightarrow -z^2$ SC block and proper SC configuration, respectively. Equation (6) shows the mathematical sequence in the time domain. The z domain transfer function of the filter calculated from this relation is shown in equation (7).

There are two high-pass filters in this figure working at two paths. Sampling frequency of every path (φ_A and φ_B) is set to 0.5 MHz whereas the frequency of φ_1 and φ_2 is 1 MHz. The entire circuit works at clock frequency of 1MHz in spite of the fact that the two high-pass filters are working at clock frequency of 0.5 MHz. Cut off frequency of the high-pass filters are 247.5 KHz that is equal to (500/2-2.5) KHz. Frequency response of each SC high-pass filter is the same as a band-pass filter with center frequency of $f_{clk}/2$ and bandwidth of 5KHz($2f_L$). Table (1) lists capacitor values which are calculated after dynamic range scaling.

TABLE 2. Poly-Poly Capacitor values

C23, C32	0.2pF
CA1	16.69pF
CA2	13.29pF
CA3	6.23pF
CB1	16.44pF
CB2	13.29pF
CB3	6.107pF
C12	0.255pF
C21	0.42pF
Cin	0.25pF
C11,C22,C33	2pF

4. SIMULATION RESULTS

Figure 7 shows the transient response of the differential output signals of the filter with (Vin)p-p=2V and f_{in}=250KHz when the sampling frequency is 1MHz and V_{dd}=1.5V. Simulation was done using 0.25µm CMOS technology and HSPICE. Frequency response of the pseudo 2-path filter is shown in Figure 8a. Data points are plotted from transient analysis of HSPICE simulator for different frequencies with (Vin)p-p = 2V.

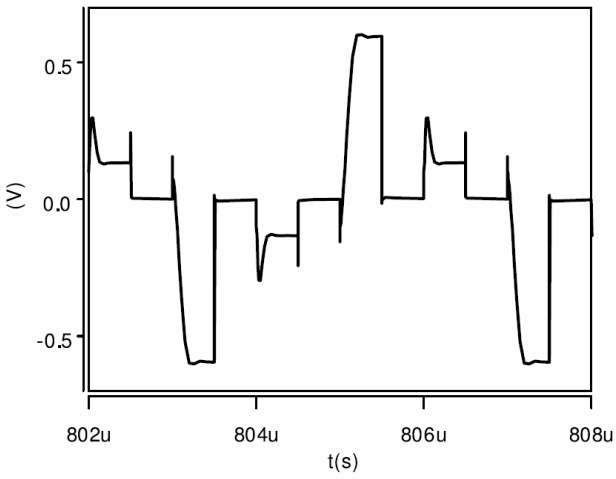

Figure 7. Differential transient response of the filter at center frequency and Vin=2Vp-p.

As shown in Figure 8b, center frequency and band-width of the filter are 250 kHz and 5 kHz, respectively. As a property of a pseudo-2-path filter, the center frequency of the interested pass-band is accurately located at 250 kHz, which is exactly 1/4 of the sampling frequency (1MHz).

$$
\begin{aligned}
V_{O1}(n+1)T &= -\frac{C_{in}}{C_{A1}}V_i(n+1)T + \frac{C_{in}}{C_{A1}}V_{in}(n-\frac{1}{2})T - \frac{C_{B1}}{C_{A1}}V_{O1}(n-1)T - \frac{C_{21}}{C_{A1}}V_{O2}(n-1)T \\
V_{O2}(n+1)T &= -\frac{C_{B2}}{C_{A2}}V_{O2}(n-1)T + \frac{C_{12}}{C_{A2}}V_{O1}(n-1)T - \frac{C_{32}}{C_{A2}}V_{O3}(n-1)T \\
V_{O3}(n+1)T &= -\frac{C_{B3}}{C_{A3}}V_{O3}(n-1)T + \frac{C_{23}}{C_{A3}}V_{O2}(n-1)T
\end{aligned} \tag{6}
$$

$$
\frac{\alpha_1\beta_2\lambda_2\, z^{-4}(z^{-\frac{3}{2}}-1)}{(1+\alpha_2 z^{-2})\,[(1+\beta_1 z^{-2})(1+\lambda_1 z^{-2})+\beta_3\lambda_2 z^{-4}]} \quad \text{where } \alpha_1 = \frac{C_{in}}{C_{A1}}, \alpha_2 = \frac{C_{B1}}{C_{A1}}, \tag{7}
$$

$$
\alpha_3 = \frac{C_{21}}{C_{A1}}, \beta_1 = \frac{C_{B2}}{C_{A2}}, \beta_2 = \frac{C_{12}}{C_{A2}}, \beta_3 = \frac{C_{32}}{C_{A2}}, \lambda_1 = \frac{C_{B3}}{C_{A3}}, \lambda_2 = \frac{C_{23}}{C_{A3}}.
$$

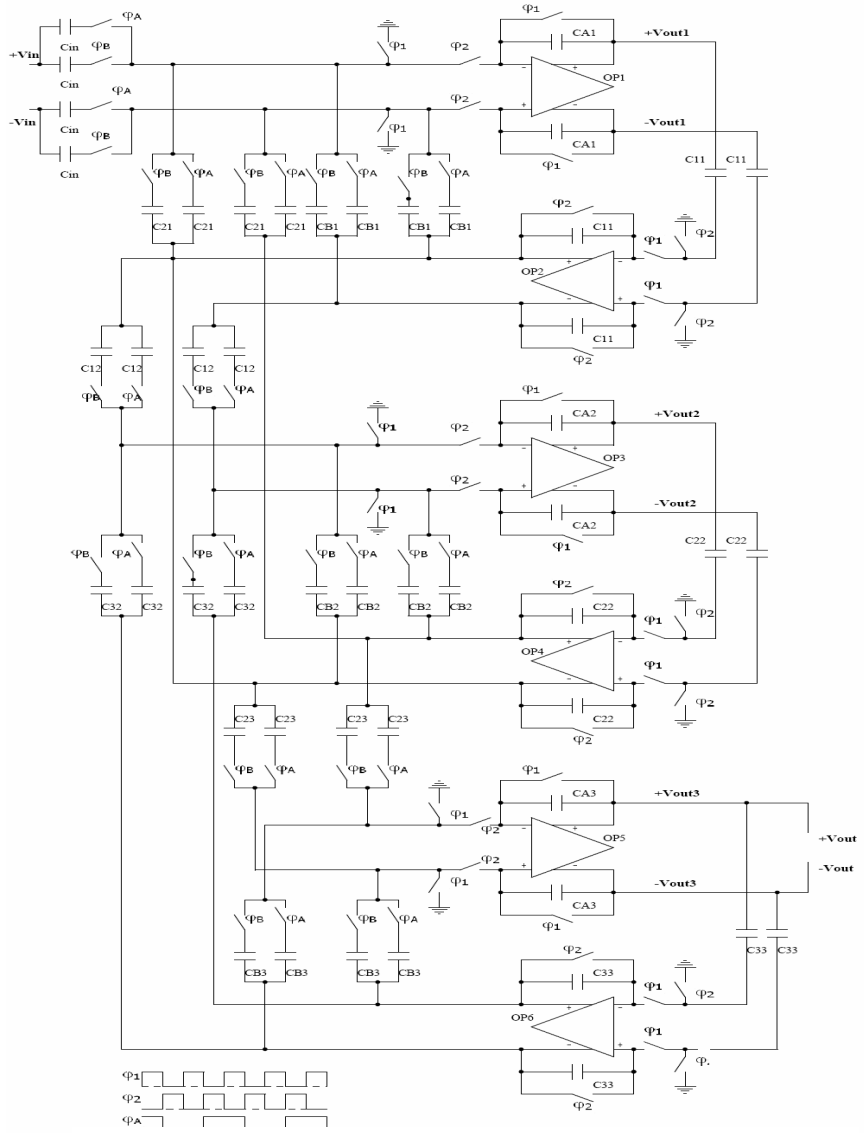

Figure 6. Proposed pseudo 2-path SC band-pass filter.

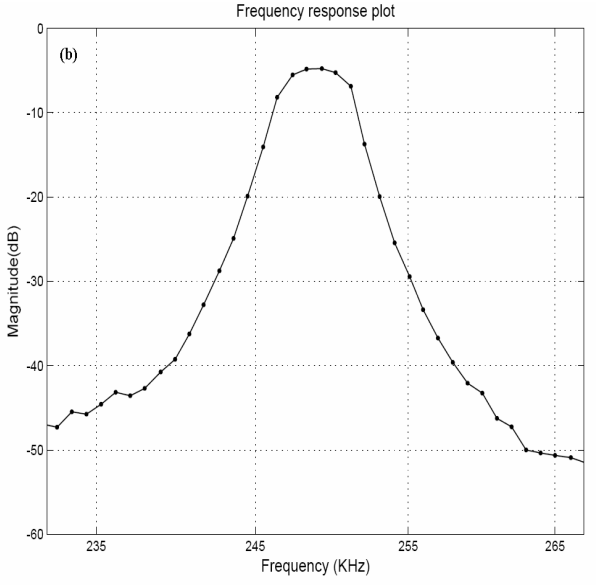

Figure 8. Frequency response of the proposed filter which is extracted by running of transient time analysis simulation at different frequencies.

The shown band-pass gain is almost -6dB, since the basic RLC filter block has the same value of 1 Ω for both R_L and R_S. Normalized spectrum of the differential output using 4096 points FFT at (V_{in})=1V_{p-p} and f_{in}=249.755859375 KHz is shown in Figure 9a. The input frequency is selected according to Roberts [15]. In Figure 9b, the third to ninth harmonics that are folded to band-pass region, are illustrated. As shown, the third-harmonic component of the input signal is at f_s-(3×f_{in})= 250.732421875 kHz, which is folded in the pass-band range. Table 2 shows the overall specification of the proposed filter.

Effect of relative capacitors accuracy on frequency response is also considered. Upper and lower limit of the frequency response where the relative capacitors accuracy is supposed to 0.1% is shown in Figure (10). This figure is obtained from 500 different series of capacitor values. Simulation is done by MATLAB using equation (7). As shown in Figure (10), the center frequency of the filter is not related to capacitor values but the amount of band-pass gain is affected slightly.

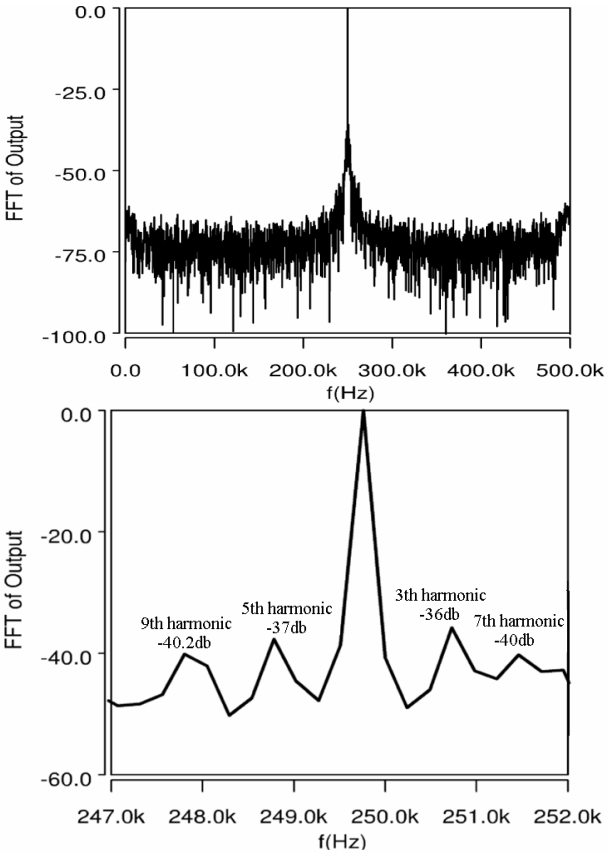

Figure 9. Normalized spectrum of differential output using 4096 points FFT at Vin=1Vp-p and input frequency of fin=249.755859375KHz.

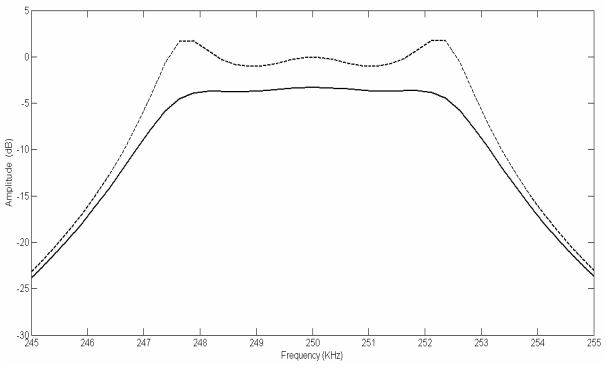

Figure 10. Upper and lower limit of frequency response where the relative capacitor accuracy is supposed to 0.1%.

TABLE 2. Overall specification of the proposed band-pass filter

Technology	0.25 μm CMOS
Supply voltage	1.5V
Centre frequency	250 KHz
Band-width	5KHz
Sampling frequency	1MHz
IM3 for Vin = 1Vpp(V_O=0.6Vpp) and fin =249.755859375 KHz	-72 dbc
Power consumption	1.68 mW
Maximum Differential Output Swing	1.2Vp-p

5. CONCLUSION

A novel structure for realization of $z \rightarrow -z^2$ based on an improved auto zeroed integrator is presented. This idea is a new method for designing n-path filters operating at higher clock frequencies compared to switched opamp methods and lower operating voltage with respect to conventional circuits. This new structure is applied to design a high Q pseudo two-path band-pass filter by transforming a low pass ladder filter into a band-pass filter. The center frequency of the proposed filter is 250 KHz and bandwidth of 5 KHz.

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