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Design and Performance Analysis of High-k Gate All Around Fin-field Effect Transistor

K. Rohith Sai, K. Girija Sravani, K. Srinivasa Rao, B. Balaji*, V. Agarwal

Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Green Fields, Vaddeswaram, Andhra Pradesh, India

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A B S T R A C T

This paper introduces and investigates a symmetrical structural design centered around a Nanoscale Fin Field-Effect Transistor (Fin-FET). Employing advanced tcad simulation techniques, the study discusses the characteristics of the Fin-FET. Here, a comprehensive exploration of the device performance across a spectrum of parameters, including drain current, electric field distribution, surface potential variations, energy band configurations, carrier concentration behaviors, and the Ion/Ioff ratio. Through rigorous analysis, the research sheds light on the symmetrical design's impact on these fundamental aspects of the Fin-FET's operation. The insights gained from this study hold the potential to enhance our understanding of device behavior, paving the road for refined designs and optimized utilization of Fin-FET technology in advanced semiconductor applications. Several types of engineering's are applied to test the device under various aspects. Gate engineering, doping engineering, and work function engineering were applied to test the device drain current characteristics. Therefore, this proposed has been widely adopted in modern Nano scale semiconductor devices.

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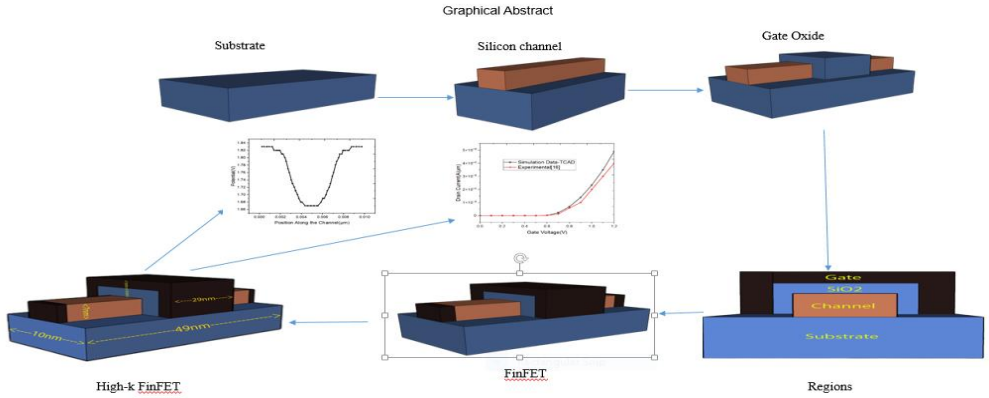
Graphical Abstract



NOMENCLATURE

eV	Energy bands	*SS*	Sub-threshold slope
SiO_2	Silicon dioxide	*Ion*	On state current
Ioff	Off state current	I_d	Drain Current
Vgs	Gate to source voltage	V_{ds}	Drain to source voltage

*Corresponding Author Email: vahividi@gmail.com (B. Balaji)

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1. INTRODUCTION

Last few years, the relentless demand for smaller, faster, and more energy-efficient electronic devices has driven semiconductor manufacturers to continually advance transistor technology. The traditional device such as planar metal oxide-semiconductor field-effect transistor (MOSFET) designs in the nano scale semiconductor field, which had served well for many years, faced insurmountable physical limitations as feature sizes shrank into the nanometer range. Challenges such as leakage currents, power dissipation, and gate control complexities became significant barriers to sustaining the continuous scaling predicted by Moore's Law (1).

The emergence of Fin Field-Effect Transistor (Fin-FET) technology marked a transformative moment in semiconductor design, providing a departure from the conventional planar MOSFET structure. This innovation reinvigorated the possibilities for performance scaling and energy efficiency improvements. The origin of Fin FET technology can be traced back to the early 2000s, when semiconductor engineers and researchers embarked on a quest to develop new transistor designs capable of overcoming the inherent limitations of planar MOSFETs. This quest led to the concept of the Fin FET architecture, characterized by its distinctive three-dimensional channel structure resembling fins. This novel architecture not only offers improved control over current flow but also effectively reduces undesirable leakage paths (2, 3). A significant milestone in the adoption of Fin FET technology was Intel's introduction of the Tri-Gate transistor in 2011. This event marked a crucial step, showcasing the practical application of Fin FETs in modern microprocessors and validating their potential to outperform traditional transistor designs. The introduction of Fin FETs has been instrumental in advancing semiconductor technology and enabling the development of more powerful and energy-efficient electronic devices (4, 5).

The operating principle of Fin FETs is deeply rooted in their distinctive structure, where the channel region is raised vertically above the substrate, resembling a fin. This structural configuration results in elevated gate control achieved by surrounding the fin with gate material. This arrangement enhances electrostatic control, leading to reduced leakage and more efficient operation. The Fin FETs offer several significant advantages, including reduced leakage currents, faster switching speeds, higher packing densities, and lower power consumption. These attributes collectively empower electronic devices with enhanced computational capabilities and energy efficiency, making them well-suited for advanced applications in consumer electronics, data centers, and emerging technologies like the Internet of Things (IoT). However, despite the transformative impact of Fin FET technology on the semiconductor industry, it is not without its challenges. The intricacies of manufacturing the intricate fin-like structures introduce complexities that could affect yields and production costs. Furthermore, as transistor dimensions continue to shrink into the nanoscale, new phenomena like quantum tunneling and variability become more prominent, necessitating innovative solutions to maintain the projected gains in performance. However, despite the transformative impact of Fin FET technology on the semiconductor industry, it is not without its challenges. The intricacies involved in manufacturing the intricate fin-like structures introduce complexities that could affect yields and production costs (6-10).

In the domain of nano-scale semiconductor technology, Fin FET have emerged as a groundbreaking solution that transcends the limitations inherent in traditional planar MOSFET designs. As transistor dimensions continue to shrink towards the nanometer scale, the challenges stemming from quantum mechanical effects, leakage currents, and power dissipation become increasingly acute (11). In response, FinFETs present an innovative three-dimensional architecture, wherein the channel takes on the form of a vertically protruding fin from the substrate. This distinctive arrangement not only enhances gate control but also effectively mitigates issues tied to short-channel effects, enabling precise modulation of current flow at an atomic scale (12, 13). The incorporation of Fin FETs within the nano-scale domain has inaugurated a novel epoch in semiconductor innovation, underpinning the development of exceptionally efficient and high-performance integrated circuits that serve a diverse spectrum of applications – ranging from portable devices to cutting-edge computing systems (14, 15).

This research paper introduces a study focused on a symmetrical structural design involving a Fin Field-Effect Transistor (FIN-FET) as shown in section 2. Through advanced TCAD simulation techniques, the investigation delves into the intricate characteristics of the FIN-FET, exploring parameters like drain current, electric field distribution, surface potential variations, energy band configurations, carrier concentration behaviors, and the Ion/Ioff ratio as shown in section 3. The research sheds light on how this symmetrical design influences these fundamental aspects of the FIN-FET's operation. The insights gained hold the potential to refine device designs and optimize the application of FIN-FET technology in advanced semiconductor contexts. Additionally, the paper evaluates the impact of gate engineering, doping engineering, and work function engineering on the device's drain current, contributing to a comprehensive understanding of its performance under various aspects.

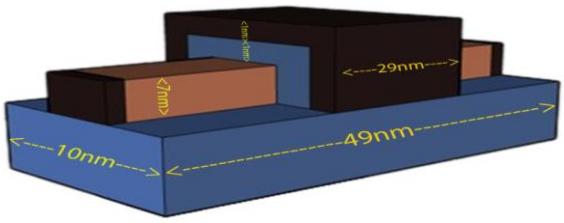
The High-k GAA-FinFET device has been widely adopted in modern semiconductor technology,

particularly in advanced integrated circuits. This proposed device offers better electrostatic control over the channel, resulting in improved performance compared to traditional planar transistors. This is crucial for achieving higher speed and lower power consumption in electronic devices. The three-dimensional FinFET design helps mitigate leakage current issues prevalent in smaller transistor sizes. This reduction in leakage current contributes to lower power consumption and improved energy efficiency. The manufacturing process for Fin FET is more complex compared to traditional planar transistors. This complexity can result in increased production costs and challenges in fabrication.

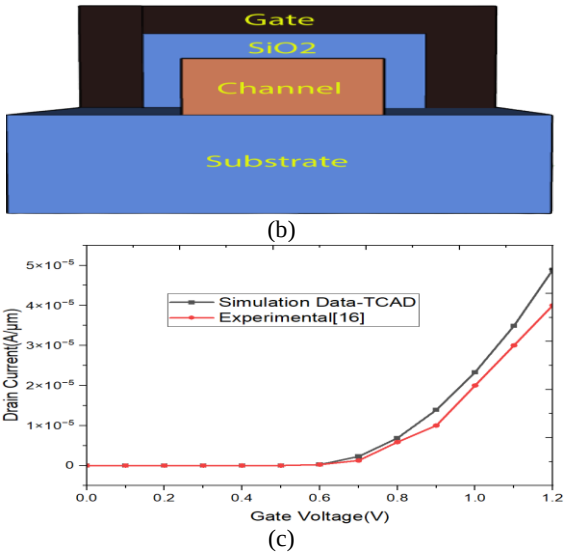
2. STRUCTURE OF PROPOSED DEVICE

The schematic view of the proposed device Fin-FET is shown in Figure 1. The 3-D ATLAS simulator is utilized to conduct device simulations. These parameters define the characteristics of the device under consideration. The gate length of 29 nm, fin thickness of 9 nm, and fin width of 10 nm determine the physical dimensions of the transistor. The channel thickness of 7 nm refers to the thickness of the conducting channel in the transistor. The gate oxide thickness (Tox) of 1 nm represents the thickness of the oxide layer between the gate and the channel (16-18). The source and drain length (Source and Drain) are both set at 10 nm. The source/drain doping level is 1x10^20 atoms/cm^3, indicating the concentration of dopant atoms in the source and drain regions. The gate work function is 4.9 eV, signifying the energy level required to extract an electron from the gate and introduce it into the channel, influencing the transistor's behavior. These parameters collectively define the operational characteristics and behavior of the proposed device (19).

In the design and analysis of the Fin FET device, a comprehensive set of advanced simulation models has been employed to accurately capture its electrical and physical behavior (20, 21). The chosen models include Schrödinger-Poisson solver (Schro), Non-Equilibrium Green's Function with multisubband (NEGF_MS), Oxide Schrödinger (Ox. Schro), semi-classical particle-based transport (sp. fast), and two-dimensional geometry representation (sp. geom=2dyz) as shown in Figure 2.



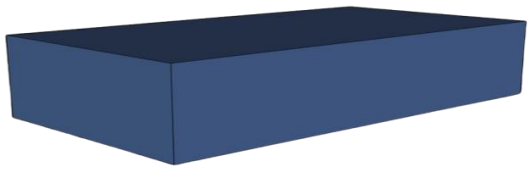
(a)



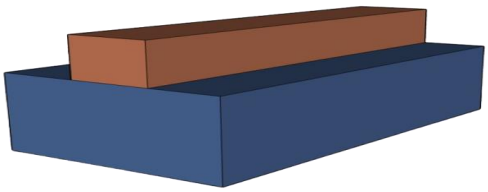
(b)

(c)

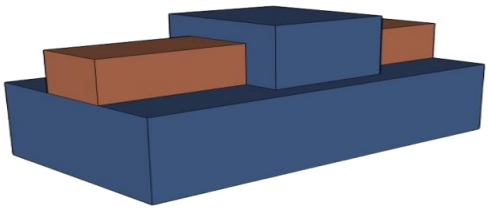
Figure 1. The structure of *the* proposed device (a) Dimensions of the device (b) Regions of the device (c) Calibrated Drain Currents



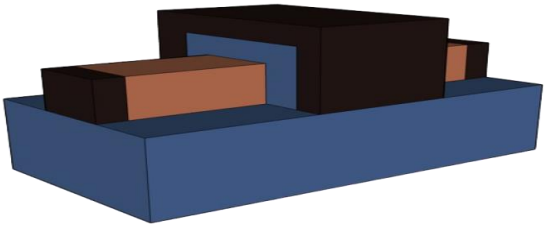
(a) Silicon Substrate



(b) Implementation of the silicon channel



(c) Adding Gate Oxide



(d) Adding Metals

Figure 2. The Tentative Fabrication Process Flow of the proposed FinFET device

FinFET is designed in a three-dimensional structure, where the channel is a raised fin surrounded by the gate on all sides. This design allows for better electrostatic control of the channel and mitigates short-channel effects. In contrast, planar transistors have a two-dimensional structure, and as transistor sizes shrink, controlling the channel becomes more challenging. The three-dimensional FinFET design helps to reduce leakage current significantly. Leakage current is a critical concern in smaller transistor sizes due to increased quantum tunneling effects.

The parameters used for the simulation of the proposed device and performance parameters are shown in Table 1 and the comparison table is shown in Table 2.

3. RESULTS AND DISCUSSIONS

3. 1. Gate Engineering Modifying the gate thickness in FinFET devices has a significant impact on their performance characteristics. Specifically, - reducing the gate thickness plays a crucial role in enhancing the device's performance. Decreasing the gate thickness allows for better electrostatic control over the channel. This results in more precise regulation of the transistor's behavior. Thinning the gate effectively manages short-channel effects, which can be a challenge in nanoscale transistors.

This improvement is critical for maintaining reliable transistor operation. The reduction in gate thickness increases gate capacitance. This increased capacitance provides greater control over the channel's behavior, enabling more effective gate regulation. Thinner gates lead to a decrease in the threshold voltage required for transistor activation. This is beneficial for achieving higher on-currents, which are essential for faster and more efficient transistor operation. Addressing concerns related to power leakage is a crucial aspect of modern semiconductor design. Thinner gates help in reducing power leakage, which is essential for energy-efficient device operation. Augmenting the gate thickness in Fin FETs introduces divergent consequences. A thicker gate diminishes gate capacitance, introducing complexities in the effective modulation of the channel's conductance. While this adjustment could aid in reducing off-state leakage current, it could concurrently lead to sluggish switching speeds and sub-optimal electrostatic dominance over the channel (24).

TABLE 1. The dimensions of the proposed FinFET device

Parameters	Values
Gate Length	29 nm
Fin Thickness	9 nm
Fin Width	10 nm
Channel thickness	7nm
Tox	1nm
Source	10nm
LDrain	10nm
S/Doping	1E20
Gate work function	4.9ev

TABLE 2. The comparison of the proposed Fin FET Device of its electric parameters with previous works

Parameters	Proposed Device	(9)	(22)	(23)
Ion	$5.79e^{-05}$	$2.05e^{-05}$	$2.24e^{-05}$	$1.11e^{-05}$
Ioff	$1.43e^{-18}$	$5.2e^{-11}$	$1.08e^{-11}$	$6.9e^{-13}$
Ion/Ioff	$4.05e^{+13}$	$2.5e^{+06}$	$1.85e^{+06}$	$1.61e^{+07}$
SS	55mV/D	---	75mV/D	61.97mV/D

Figure 3 shows the variation in drain current for different gate thickness. A reduction in gate thickness brings about a notable increase in drain current. As such, the decision to manipulate the gate thickness necessitates meticulous consideration, weighing the desired trade-offs between performance, power efficiency, and switching speed. This evaluation should align with the distinctive application and design requisites of the FinFET device (25).

3. 2. Effect of Changing Doping Concentration The doping concentration within FinFET structures yields significant changes in the drain current, revealing a direct correlation between doping levels and device performance. Elevated doping concentrations in the source and drain regions lead to an increased pool of charge carriers primed for conduction. This surplus of carriers translates into a higher drain current, facilitated by the amplified availability of charge carriers for seamless transport between the source and drain terminals. In contrast, reducing doping concentrations curtails the available carriers, subsequently diminishing the overall drain current. This controlled manipulation of

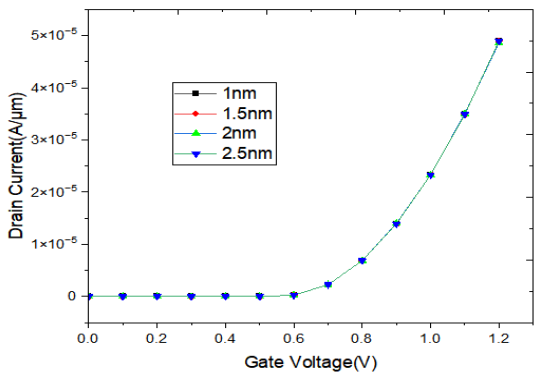


Figure 3. The Drain current characteristics of the proposed device for different gate thickness (1, 1.5, 2, 2.5nm)

doping concentration emerges as a potent strategy for tailoring the electrical traits of FinFETs. Through deliberate adjustments in doping levels, a fine equilibrium can be achieved, optimizing conduction efficiency while simultaneously curbing leakage currents. This dynamic tuning of doping concentration stands as a versatile approach for refining the performance characteristics of the device to meet specific application demands (26).

Figure 4, shows the variation in drain current for different doping concentrations. With a rise in doping concentration within the source and drain regions of FinFET structures, the abundance of available charge carriers for conduction experiences a significant surge. This excess of charge carriers plays a pivotal role in driving a substantial increase in the drain current. This augmentation is facilitated by the heightened availability of charge carriers, enabling efficient transportation between the source and drain terminals (27). Consequently, this heightened carrier concentration contributes to an elevated level of conductivity, thereby enhancing the overall performance of the device. By elevating the doping concentration, the device's suitability for facilitating current flow is enhanced, leading to an amplification of its capacity to manage electrical signals.

3. 3. Effect of Changing Work Functions The work function within the Fin FET framework across the range of 4.9 to 5.3 introduces noticeable alterations in the drain current, uncovering a direct correlation between work function values and the device's operational prowess. As the work function progressively increases from 4.9 to 5.3, a transformation occurs in the energy barrier situated at the gate-channel interface. This evolution in the energy barrier has a direct impact on how charge carriers respond to the gate voltage's influence—altering the balance between attraction and repulsion. With a higher work function, the energy barrier becomes narrower, facilitating a more efficient regulation of charge carrier flow between the source and drain regions. This heightened gate control culminates in an amplified drain current, as charge carriers encounter reduced resistance during their traversal (28).

Figure 5 shows the relationship between drain current and gate voltage for varying work functions ranging from 4.9eV to 5.3eV in the FinFET device. As the work function increases, the modulation of drain current becomes more pronounced, highlighting the pivotal role of work function in influencing device behavior and performance (29).

3. 4. The Optimization of the Proposed Device Incorporating modifications to the device based on the analysis of drain current, we have established fixed values for the gate thickness, doping concentration, and the work function of the gate metal. The parameters such as electric field, surface potential, energy bands, and carrier concentration have been analyzed for the suggested device.

In Figure 6, we have observed the spatial profile of the electric field of this proposed device within the channel of a FinFET. Understanding the energy bands within a FinFET is pivotal for comprehending its electronic behavior.

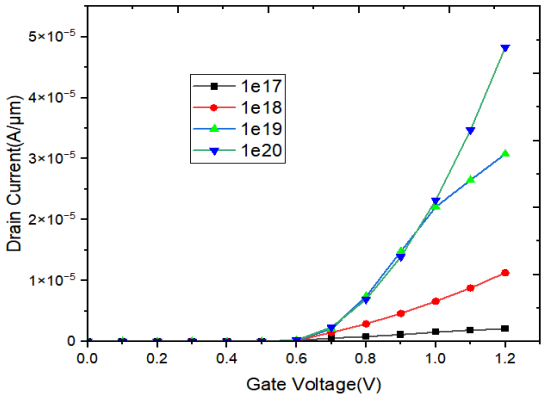


Figure 4. The drain current for gate voltage for different doping concentration (1e17, 1e18, 1e19, 1e20)

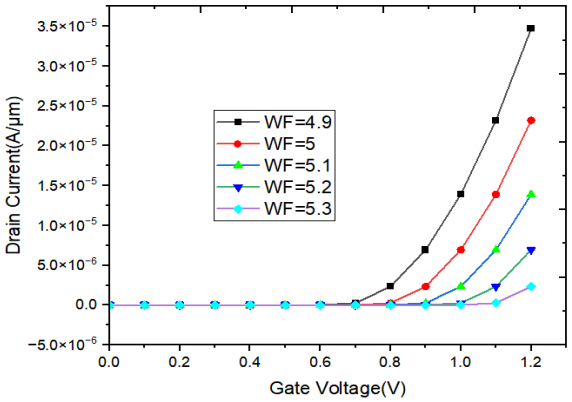


Figure 5. The variation in drain current with respect to gate voltage for different work functions (4.9-5.3)

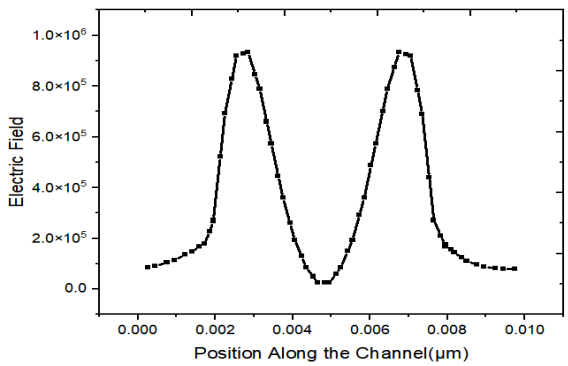


Figure 6. The electric field concerning position along the channel for the proposed device

Figure 7 is a comprehensive visualization of the energy bands across the channel length within a Fin FET device. Consequently, this graphical representation enhances our understanding of the interplay between spatial positioning and energy distribution, a pivotal factor in shaping the device's overall performance characteristics.

Figure 8 is a visual depiction that effectively showcases the distribution of potential across the length of the channel within a Fin FET device. This provides valuable insights into the progressive changes in potential as they relate to spatial position within the channel. Notably, the unique three-dimensional structure of the fin-like channel introduces intricate variations in potential along both the vertical and lateral dimensions.

Figure 9 is a visual portrayal that offers insight into the alteration of carrier concentration across the channel's length within a Fin FET (Fin Field-Effect Transistor) device. This representation sheds light on the transformation of charge carrier density—whether electrons or holes—relative to the spatial location within the channel. The concentration undergoes subtle shifts as one traverses from the source to the drain region. The channel's distinct three-dimensional fin-like design introduces complex changes in carrier concentration, encompassing both vertical and lateral dimensions.

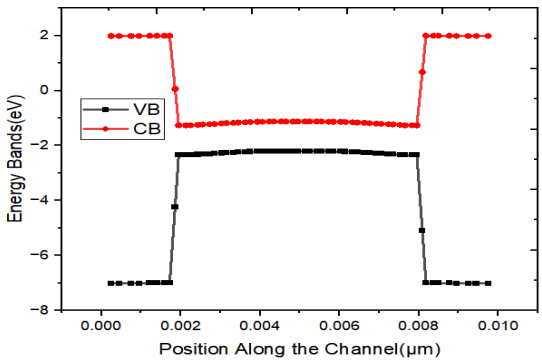


Figure 7. The energy bands concerning position along the channel for the proposed device

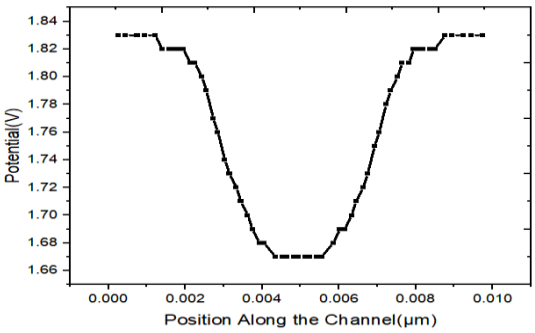


Figure 8. The potential concerning position along the channel for the proposed device

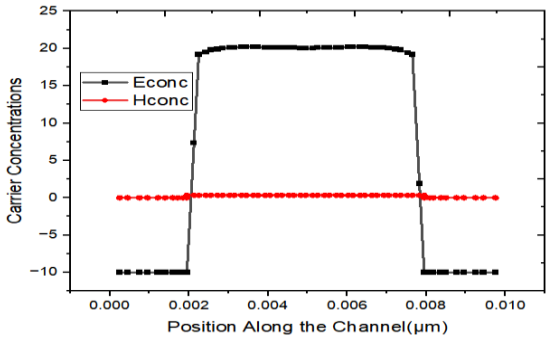


Figure 9. The carrier concentration with respect to position along the channel for the proposed device

4. CONCLUSION

This paper presents a comprehensive investigation into a symmetrical structural design centered around the Fin Field-Effect Transistor (Fin-FET). Through the utilization of advanced TCAD simulation techniques, the study delves deeply into the intricate characteristics of the Fin-FET, analyzing a wide array of crucial parameters such as drain current, electric field distribution, surface potential variations, energy band configurations, carrier concentration behaviors, and the Ion/Ioff ratio. The symmetrical design's impact on these fundamental operational aspects of the Fin-FET has been rigorously examined, providing valuable insights into its behavior. The findings of this research contribute significantly to our understanding of the Fin-FET's behavior and performance. These insights hold substantial promise for the advancement of semiconductor technology, as they can guide the development of refined designs and optimized utilization of Fin-FETs in advanced applications.

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Persian Abstract

چکیده

این مقاله یک طراحی ساختاری متقارن را با محوریت ترانزیستور اثر میدانی باله نانومقیاس (Fin-FET) معرفی و بررسی می‌کند. این مطالعه با استفاده از تکنیک‌های شبیه‌سازی tcad پیشرفته، ویژگی‌های Fin-FET را مورد بحث قرار می‌دهد. در اینجا، یک کاوش جامع از عملکرد دستگاه در طیفی از پارامترها، از جمله جریان تخلیه، توزیع میدان الکتریکی، تغییرات پتانسیل سطحی، پیکربندی‌های باند انرژی، رفتارهای غلظت حامل و نسبت یون / یون است. از طریق تجزیه و تحلیل دقیق، این تحقیق تأثیر طراحی متقارن را بر این جنبه های اساسی عملکرد Fin-FET روشن می کند. بینش‌های به‌دست‌آمده از این مطالعه، پتانسیل افزایش درک ما از رفتار دستگاه، هموار کردن راه را برای طراحی‌های دقیق و استفاده بهینه از فناوری Fin-FET در کاربردهای نیمه‌رسانای پیشرفته دارد. چندین نوع مهندسی برای آزمایش دستگاه در جنبه های مختلف اعمال می شود. مهندسی گیت، مهندسی دوپینگ و مهندسی عملکرد کار برای آزمایش ویژگی‌های جریان تخلیه دستگاه استفاده شد. بنابراین، این پیشنهاد به طور گسترده ای در دستگاه های نیمه هادی در مقیاس نانو مدرن پذیرفته شده است.