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A New Generalized Step-up Multilevel Inverter Topology Based on Combined T-type and Cross Capacitor Modules

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A B S T R A C T

This paper presents a new symmetrical switched-capacitor (SC) multilevel inverter topology which can convert the input DC voltage to a step-up multilevel AC waveform on the load. This proposed multilevel inverter consists of one T-type and several cross-capacitor modules. The structure of the generalized multilevel inverter is such that the peak inverse voltage (PIV) remains constant as the number of cross-capacitor modules increases which leads to reduce the total standing voltage (TSV) of the switches and cost function compared to other traditional topologies. The introduced structure can inherently generate the positive, negative, and zero voltage levels on the output without the back-end H-bridge section. The capacitor's voltages in the T-type and cross modules are inherently balanced, simplifying the control system under the nearest level control (NLC) switching strategy. To verify the performance of the proposed topology, several simulations and experimental results for a type 13-level inverter are provided by MATLAB and TMS320F28379D DSP, respectively.

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1. INTRODUCTION

Nowadays, multilevel inverters (MLIs) are being developed for application in renewable energy resources, high voltage DC (HVDC) systems, electrical vehicles, microgrid systems, and so on [1, 2]. They can generate a staircase voltage which leads to reducing the total harmonic distortion (THD) and size of the passive filter on the output. The other advantages of multilevel inverters consist of low voltage stress on the semiconductor devices (switches and diodes), low dv/dt stress, and high efficiency [3, 4]. Generally, the MLIs are divided into three conventional groups: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB). The NPC and FC-type inverters have many diodes and capacitors in their structures, respectively. However, some topologies such as active-NPC and transistor-NPC have been developed by researchers for overcoming it, but these configurations still require extra auxiliary circuits for balancing the neutral point [5-7]. The CHB-based topologies need several isolated input DC sources to obtain a number of high voltage levels on the output. For many applications such as photovoltaic (PV) systems and wind turbines, it is necessary that a step-up inverter is applied to increase the input DC voltage [8, 9]. It must be stated that none of the three conventional topologies mentioned above can boost the input DC voltage. So, researchers introduced several approaches to achieve this purpose. One of the approaches is to use a coupling inductor or transformer in a multilevel inverter structure [10-14]. However, in low frequencies (lower than 50 Hz), the inductors and transformers make the system drastically bulky and expensive. Alemi-Rostami and Rezazadeh [10] introduced a boost multilevel inverter with the presence of a coupling inductor. Nevertheless, the voltage gain has not been assessed for various frequency ranges. Moreover, using an H-bridge as a polarity generation circuit increases the PIV of switches when the number of modules is increased. An increase in PIV leads to an

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increase in the voltage rating of switches and thus increases the volume and cost of the whole system. Ghanbari, and Tousi [11] presented a boost transformer-based binary hybrid multilevel inverter which is required only a single DC source instead of several isolated DC sources. However, in this scenario, in addition to increasing the volume of the system, it requires several H-bridge cells leading to an increase in the TSV. Another approach to obtain the boost capability of MLIs is to use circuits based on switched-capacitor (SC) which inherently have the self-balancing ability [15, 16]. However, there are two concerns about this type of MLIs. One is the complexity of the system due to a high number of device counts such as switches and capacitors and another is the performance in high-frequency (HF) conditions for many applications such as high-speed motors, induction heating, and electric vehicles. Several SC-based MLIs have been reported with a reduction in the number of semiconductor devices, but with an increase in the modules, the PIV of switches has been drastically increased [17-23]. Hussan et al. [17] introduced an SC topology for smart grid application with two T-type capacitor modules. The T-type modules can inherently balance the capacitor voltages. However, using three isolated DC power sources is the most important challenge related to this topology. Taheri et al. [18] presented a 17-level SC multilevel inverter topology with several cross-capacitor modules. In this configuration, the number of switches has been drastically reduced. Nevertheless, by increasing the cross-capacitor modules (especially in asymmetrical mode), the PIV of switches is increased to achieve the number of high voltage levels. Recently, Khenar et al. [24] introduced a boost self-balancing SC multilevel inverter based on combined T-type and cross-capacitor modules which can keep PIV constant by increasing the capacitor modules. However, obtaining the 13-level output voltage, it requires 23 switches, 4 diodes, and 6 capacitors. So, in the number of high voltage levels, the inverter introduced by Khenar et al. [24] needs a high number of capacitors. According to the discussion made above, this paper presents a new structure of SC multilevel inverter with the following properties,

i. Step-up capability without the presence of any transformer and inductor.
ii. Constant PIV in the switches with increasing the number of modules.
iii. 13-level topology with single DC bus, 20 switches, 4 capacitors, and without power diode.
iv. Performance in low frequency (LF) and HF conditions.

Generally, the proposed topology has two important characteristics. First, it provides a high gain voltage on the load (as much as 6). Secondly, by increasing the number of cross-module, the peak inverse voltage (PIV) remains constant, leading drastically to reduce the total standing voltage of the switches. The rest of this paper has been arranged as follows: section 2 introduces the proposed topology with switching states. Section 3 gives the comparison of the new SC multilevel inverter with other conventional topologies. Section 4 elaborates on the nearest level control as the switching technique. The calculations of capacitance values and power losses in the proposed topology are performed in section 5. In section 6, several simulations and experimental results are conducted to verify the performance of the proposed topology. Finally, the conclusions are organized in section 7.

2. CIRCUIT OF THE PROPOSED TOPOLOGY

2. 1. 13-level Structure The circuit structure of the proposed 13-level inverter is shown in Figure 1.

This figure contains one T-type module and two cross-capacitor modules. The T-type module includes six switches ($S_1S_2S_3S_4S_5S_6$) and two capacitors (C_{t1} and C_{t2}). The cross-capacitor modules consist of a non-expandable part with switches ($S_7S_8S_9S_{10}S_{11}S_{12}$) and capacitor C_f and an expandable part with switches ($S_{13}S_{14}S_{15}S_{16}S_{17}$) and capacitor C_m. In general, the proposed 13-level topology consists of 20 switches (with 3 bi-directional switches), 4 capacitors, a zero diode, and one DC bus (V_{dc}). For achieving the high voltage gain on the output, the capacitors C_f and C_m can be connected together as parallel with the sum of the capacitors C_{t1} and C_{t2}. Table 1 and Figure 2 show the switching states and current commutation paths of the proposed multilevel inverter, respectively. The current commutation paths are arranged to obtain the voltage levels $\pm1V_{dc}$, $\pm2V_{dc}$, $\pm3V_{dc}$, $\pm4V_{dc}$, $\pm5V_{dc}$, $\pm6V_{dc}$, and $0V_{dc}$. According to states 6 and 8 in Table 1, and Figures (2h) and (2b), the capacitors C_{t1} and C_{t2} are charged by T-type throughout switches $S_1S_4S_5S_3$ and $S_1S_2S_5S_6$, respectively, up to $1V_{dc}$ in a self-balancing manner.

On the other hand, referring to states 5 and 10, and Figures (2g) and (2j), the capacitors C_f and C_m can be

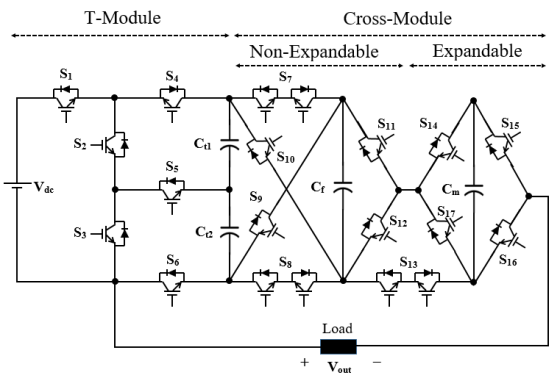
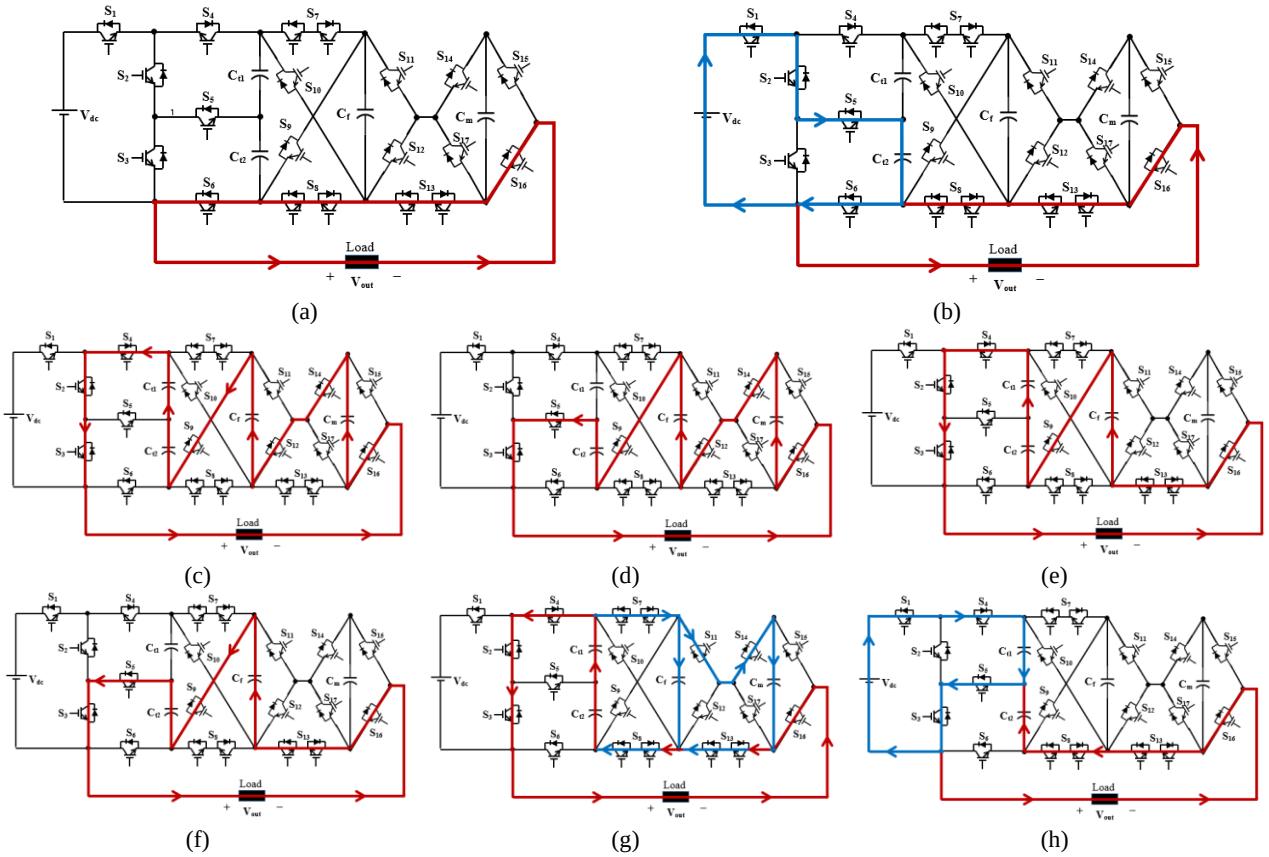


Figure 1. Proposed step-up 13-level inverter topology

TABLE 1. Switching states for the proposed 13-level inverter. The symbols C, D, and W indicate charge, discharge, and without change, respectively

Process	States	T-module	Cross-module		$C_{t1}C_{t2}C_fC_m$	V_{out}
			Non-Expandable	Expandable		
		$S_1S_2S_3S_4S_5S_6$	$S_7S_8S_9S_{10}S_{11}S_{12}$	$S_{13}S_{14}S_{15}S_{16}S_{17}$		
Switching states/capacitor states/voltage levels	1	011100	001001	01010	D-D-D-D	$+6V_{dc}$
	2	001010	001001	01010	W-D-D-D	$+5V_{dc}$
	3	011100	001000	10010	D-D-D-W	$+4V_{dc}$
	4	001010	001000	10010	W-D-D-W	$+3V_{dc}$
	5	011100	110010	11010	D-D-C-C	$+2V_{dc}$
	6	001010	010000	10010	C-D-W-W	$+1V_{dc}$
	7	101111	010000	10010	W-W-W-W	$0V_{dc}$
	8	110011	010000	10010	W-C-W-W	$0V_{dc}$
	9	001010	100010	01100	D-W-W-W	$-1V_{dc}$
	10	000001	110010	11100	D-D-C-C	$-2V_{dc}$
	11	001010	100010	00101	D-W-W-D	$-3V_{dc}$
	12	000001	100010	00101	D-D-W-D	$-4V_{dc}$
	13	001010	000110	00101	D-W-D-D	$-5V_{dc}$
	14	000001	000110	00101	D-D-D-D	$-6V_{dc}$
PIV/$1V_{dc}$		1-1-1-1-1-2	4-4-4-4-2-2	4-2-2-2-2	-------	-------



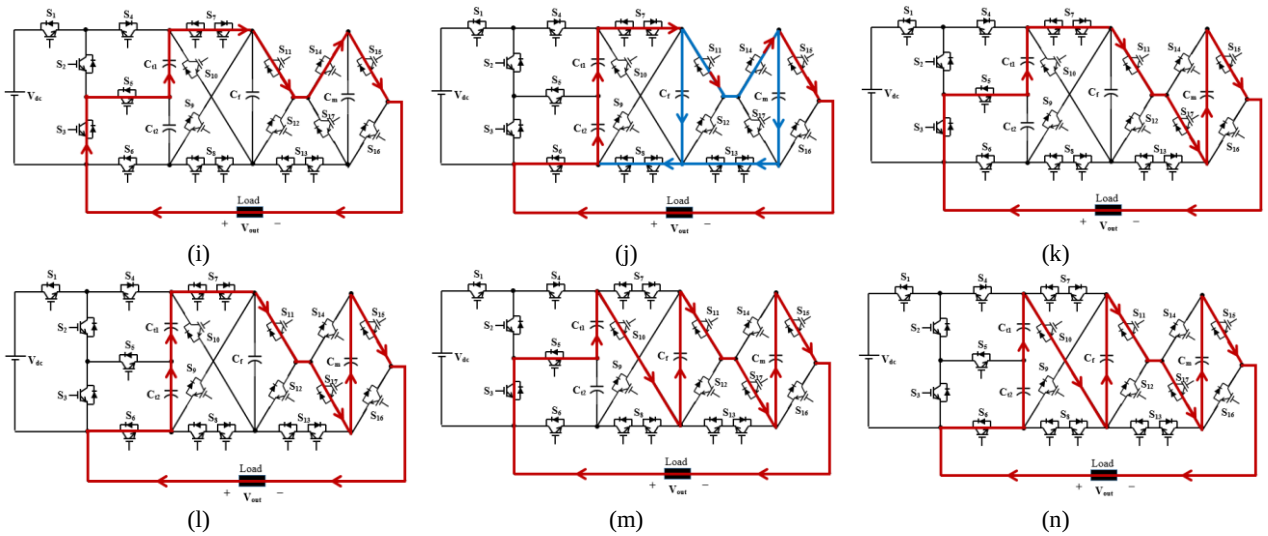


Figure 2. Current commutation paths to generate various voltage levels on the output according to switching states shown in Table 1. (a) $0V_{dc}$, (b) $0V_{dc}$, (c) $+6V_{dc}$, (d) $+5V_{dc}$, (e) $+4V_{dc}$, (f) $+3V_{dc}$, (g) $+2V_{dc}$, (h) $+1V_{dc}$, (i) $-1V_{dc}$, (j) $-2V_{dc}$, (k) $-3V_{dc}$, (l) $-4V_{dc}$, (m) $-5V_{dc}$, and (n) $-6V_{dc}$.

simultaneously charged up to $2V_{dc}$ through the sum of the voltages of capacitors C_{t1} and C_{t2}. Hence, the total voltage of the capacitors is obtained as $6V_{dc}$, which is equal to the voltage gain and the number of voltage levels in the half-cycle of the output in the proposed 13-level multilevel inverter.

2. 2. Generalized Structure According to Figure 3, the proposed SC multilevel inverter can be extended by several cross-modules consecutively to obtain the high number of voltage levels on the output. With the addition of each expandable module, the PIV of the switches remains constant. Table 2 shows the number of device counts and blocking voltage of switches for the N-level proposed topology.

As shown in this table, the switches ($S_1S_2S_3S_4S_5$) and (S_9S_{10}) have the lowest ($1V_{dc}$) and the highest ($4V_{dc}$) blocking voltage, respectively. So, the PIV of the switches in the proposed multilevel inverter is $4V_{dc}$.

3. COMPARISON WITH OTHER TOPOLOGIES

In this section, the proposed SC multilevel inverter is compared with other topologies [20-24] in view of the number of switches, number of diodes, number of capacitors, TSV, and cost function (CF). According to Table 3, which lists these parameters, the proposed topology has the lowest number of capacitors and TSV. For instance, in the 13-level case, the number of capacitors in the literature [20-24] is 5, 5, 5, 5, and 6,

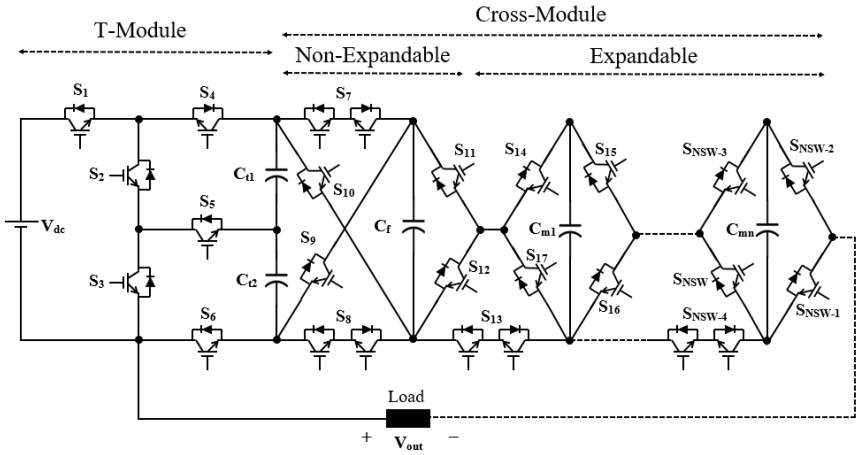


Figure 3. Generalized proposed SC multilevel inverter

TABLE 2. characteristics of proposed SC multilevel inverter for N level and N_{sw} switch

Parameter	Value
Number of switches (N_{sw})	1.5N+0.5 (N=9, 13, 17, 21, …)
Number of gate drivers (N_g)	1.25N+0.75 (N=9, 13, 17, 21, …)
Number of capacitors (N_C)	0.25N+0.75 (N=9, 13, 17, 21, …)
Blocking voltage for T-module	$1V_{dc}$ for all switches expect S_6 ($2V_{dc}$)
Blocking voltage for Non-Expandable module	$4V_{dc}$ for all switches expect S_{11} and S_{12} ($2V_{dc}$)
Blocking voltage for Expandable module	$2V_{dc}$ for all switches expect (N_{SW}-4)-th switch ($4V_{dc}$)

respectively while it is equal to 4 in the proposed topology. Now, lets the CF be defined as follows:

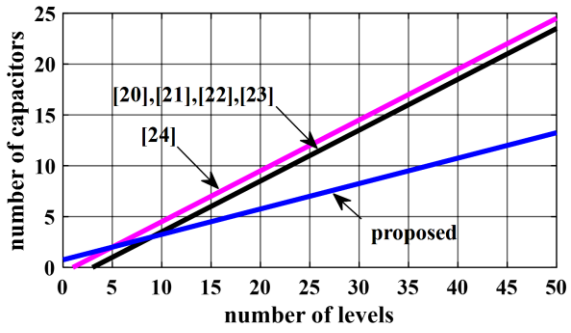
$$CF = N_{semiconductor} + N_C + \alpha \times \frac{TSV}{V_{dc}} + \beta \times \frac{PIV}{V_{dc}} \quad (1)$$

where $N_{semiconductor}$ is the number of switches and diodes. Moreover, α and β are the weight of TSV and PIV against the number of device counts ($N_{semiconductor}$ + N_C), respectively. α and β are selected more than 1 when the TSV and PIV are more important than the device counts. On the other hand, α and β are selected less than 1 when the TSV and PIV are less important than the device counts. For a more detailed review, Figure 4 is shown graphically the comparison of the proposed multilevel inverter with others. As shown in Figure 4(b), the PIV for [24] and proposed topologies remain constant with increasing the number of levels.

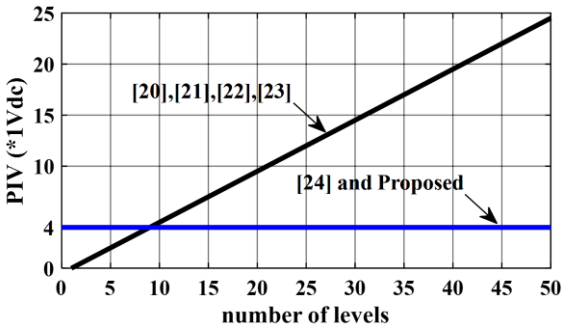
Moreover, according to Figure 4(d), the proposed multilevel inverter has the lowest CF than other topologies whether with α=β=0.5 or with α=β=1.5. In a general view, it seems that the introduced inverter has close competition with the literature [24]. However, the number of capacitors and the CF in the proposed topology are more favorable.

TABLE 3. Comparison of the proposed multilevel inverter with other topologies for an N-level output voltage

Parameters	[20]	[21]	[22]	[23]	[24]	Proposed
number of switches	$\frac{3N-1}{2}$	$\frac{2N+6}{2}$	$\frac{N+7}{2}$	$\frac{3N-1}{2}$	$\frac{3N+7}{2}$	$\frac{3N+1}{2}$
Number of capacitors	$\frac{N-3}{2}$	$\frac{N-3}{2}$	$\frac{N-3}{2}$	$\frac{N-3}{2}$	$\frac{N-1}{2}$	$\frac{N+3}{4}$
Number of diodes	0	$N-1$	$N-3$	0	0	0
PIV for H-bridge switches	$\frac{N-1}{2}V_{dc}$	$\frac{N-1}{2}V_{dc}$	$\frac{N-1}{2}V_{dc}$	$\frac{N-1}{2}V_{dc}$	No need	No need
Maximum PIV for switches	$\frac{N-1}{2}V_{dc}$	$\frac{N-1}{2}V_{dc}$	$\frac{N-1}{2}V_{dc}$	$\frac{N-1}{2}V_{dc}$	$4V_{dc}$	$4V_{dc}$
TSV(×$1V_{dc}$)	$\frac{7N-13}{2}$	$\frac{N^2}{4}+2N-\frac{5}{4}$	$\frac{N^2}{4}+\frac{3}{2}N-\frac{7}{4}$	$\frac{N^2+18N-19}{8}$	$\frac{7N-11}{2}$	3N



(a)



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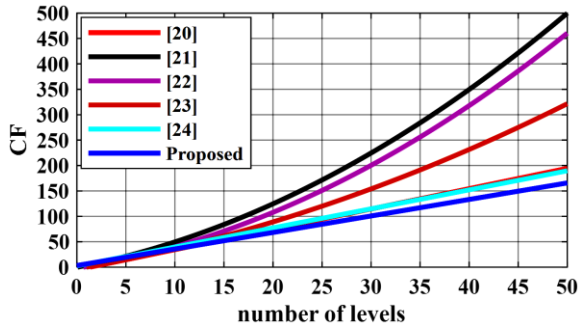
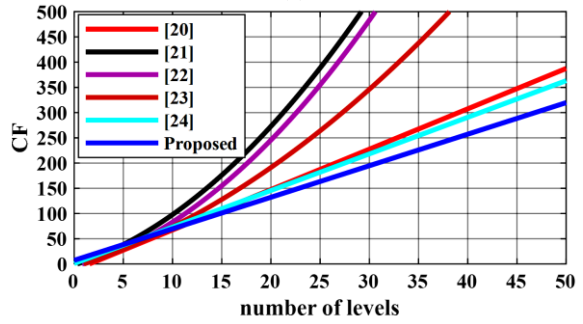


(c)



(d)

Figure 4. Comparison of the proposed topology with others. (a) number of capacitors, (b) PIV, (c) CF for α=β=0.5, and (d) CF for α=β=1.5

4. NEAREST LEVEL CONTROL

There are two general switching techniques for the multilevel inverter which are called as high switching frequency (HSF) and fundamental switching frequency (FSF) [25]. In the HSF switching techniques such as multi-carrier pulse width modulation (MC-PWM), one full sinusoidal wave is compared with several sawtooth waves with switching frequencies higher than 2kHz. This technique is used mostly for closed-loop control systems [26]. On the other hand, switching techniques based on FSF cause lower power losses on the inverter than HSF techniques. The most famous of the FSF techniques are nearest level control (NLC) and selective harmonic elimination (SHE). In the SHE scheme, by solving several non-linear equations using the Newton-Raphson method, the switching angles for generating gate pulses are obtained. However, at a high number of voltage levels, solving equations becomes very complicated and boring [27]. In the NLC switching technique, a full sinusoidal wave as the reference signal (V_{ref}) is compared with a multi-step signal so that the output voltage is close to a multilevel wave, leading to simplifying the control of the switches. For this purpose, first, the reference signal is normalized by the maximum voltage level factor (V_{omax}) then it is quantized in form of a multi-step wave. Finally, the quantized wave decides which switch to activate [28, 29]. Figure 5 shows briefly how to implement the NLC switching technique which has been considered in this work. In this figure, t_i is the switching time of the i^{th} level, and it is described as follows:

$$t_i = \frac{1}{\omega}\sin^{-1}\left(\frac{2i-1}{N-1}\right),\quad i=1,2,3,\ldots,\frac{N-1}{2}. \tag{2}$$

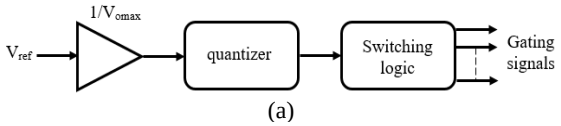
where ω is the reference angular frequency and it is formulated as $\omega=2\pi f_s$.

5. CAPACITANCE AND POWER LOSSES CALCULATIONS

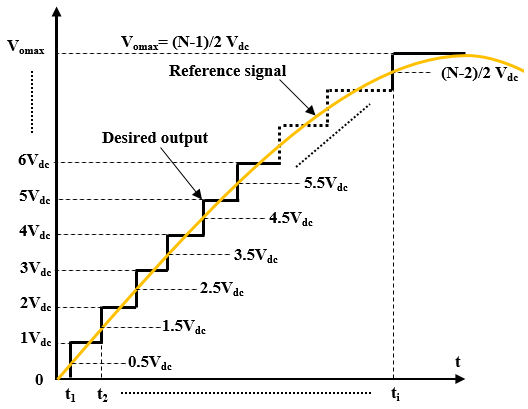
In this section, the capacitance and power losses are calculated for a type 13-level proposed topology. In all cases, it is assumed the load is purely resistive.

5. 1. Capacitance Calculation As shown in Figure 1, there are four capacitors in the proposed 13-level inverter which can be charged and discharged at various instant intervals. The capacitors C_{t1}, C_{t2}, C_f, and C_m are charged up to $1V_{dc}$, $1V_{dc}$, $2V_{dc}$, and $2V_{dc}$, respectively. To charge these capacitors at the mentioned voltages, it is necessary to know the optimal value of the capacitance values.

For this purpose, the largest discharging cycle (LDC) of the capacitors is considered. Using Table 1, it can be depicted the charging and discharging time intervals of the capacitors which are shown in Figure 6. As shown in this figure, the LDC of the capacitors C_{t1}, C_{t2}, C_f, and C_m is between (t_1 to T/2-t_1), (t_1+T/2 to (T-t_1)), (t_3 to T/2-t_3), and (t_5 to T/2-t_5), respectively. It should be noted that the



(a)



(b)

Figure 5. NLC switching technique for the pulse generation in the proposed multilevel inverter (a) block diagram (b) graphical presentation

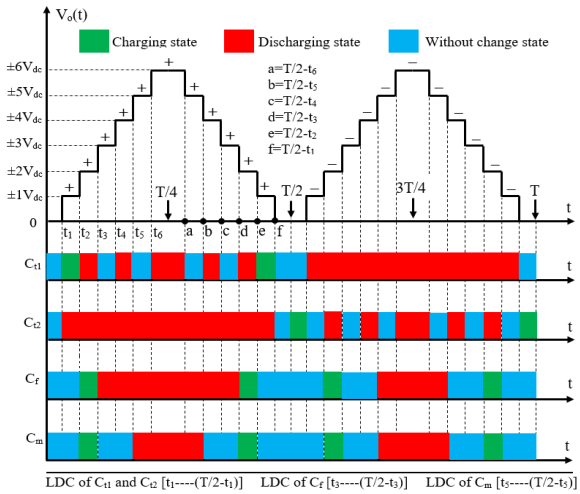


Figure 6. Charging and discharging time intervals of the capacitors C_{t1}, C_{t2}, C_f, and C_m used in the proposed topology

LDC of the capacitors C_{t1} and C_{t2} is equal to each other, leading to equalize of capacitances C_{t1} and C_{t2} (i.e. $C_{t1}=C_{t2}$). So, the calculation of the capacitance is only performed for one of them.

The expression for the discharging states of the capacitors C_{t1}, C_{t2}, C_f, and C_m in the LDC time interval are described as follows:

$$\Delta Q_{C_{t1}} = \Delta Q_{C_{t2}} = \int_{t_1}^{T/2-t_1} i_L(t)dt \tag{3}$$

$$\Delta Q_{C_f} = \int_{t_3}^{T/2-t_3} i_L(t)dt \tag{4}$$

$$\Delta Q_{C_m} = \int_{t_5}^{T/2-t_5} i_L(t)dt \tag{5}$$

where $i_L(t)$ is the instantaneous load current and it can be written as,

$$i_L(t) = i_m \sin(\omega t) \tag{6}$$

where i_m is the peak of the load current. From Equations (3) to (5), the values of the C_{t1}, C_{t2}, C_f, and C_m can be formulated as,

$$C_{t1} = C_{t2} = \frac{1}{\Delta V_{C_{t1}}} \int_{t_1}^{T/2-t_1} i_L(t)dt \tag{7}$$

$$C_f = \frac{1}{\Delta V_{C_f}} \int_{t_3}^{T/2-t_3} i_L(t)dt \tag{8}$$

$$C_m = \frac{1}{\Delta V_{C_m}} \int_{t_5}^{T/2-t_5} i_L(t)dt \tag{9}$$

where ΔV_{Ct1}, ΔV_{Cf}, and ΔV_{Cm} are the permissible voltage ripple of the capacitors C_{t1}, C_f, and C_m, respectively. By considering the value of V_{dc}=20v (to achieve the maximum output voltage level V_{omax}=120v), the capacitors C_{t1}, C_{t2}, C_f, and C_m are charged up to 20v, 20v, 40v, and 40v, respectively. Hence, the values of ΔV_{Ct1}, ΔV_{Cf}, and ΔV_{Cm}, which are usually considered as 10% of the corresponding capacitor voltage, can be obtained as:

$$\begin{cases} \Delta V_{Ct1} = \Delta V_{Ct2} = 2v \\ \Delta V_{Cf} = 4v \\ \Delta V_{Cm} = 4v \end{cases} \tag{10}$$

The solution of Equations (7), (8), and (9) leads to appear the values of C_{t1}=C_{t2}, C_f, and C_m which are expressed as:

$$C_{t1} = C_{t2} = \frac{2 \times i_m \cos(\omega t_1)}{2\pi f_s \times \Delta V_{C_{t1}}} \tag{11}$$

$$C_f = \frac{2 \times i_m \cos(\omega t_3)}{2\pi f_s \times \Delta V_{C_f}} \tag{12}$$

$$C_m = \frac{2 \times i_m \cos(\omega t_5)}{2\pi f_s \times \Delta V_{Cm}} \tag{13}$$

By using Equation (2), for N=13 and f_s=50Hz, the switching times are obtained as t_1=0.00026s, t_2=0.0008s, t_3=0.0014, t_4=0.002s, t_5=0.0027s, and t_6=0.0037s. Using these switching times and Equation (10), for i_m=2A, the final solution of C_{t1}, C_{t2}, C_f, and C_m come out to be 6300µF, 6300µF, 2900µF, 2100µF, respectively. The available values of the capacitors in the laboratory are 2200µF and 4700µF. For this reason, in the experimental setup, the capacitors C_{t1}, C_{t2}, C_f, and C_m are equally chosen as much as (3×2200µF), (3×2200µF), 4700µF, and 2200µF, respectively.

5. 2. Power Losses Calculation Generally, power losses in the proposed SC multilevel inverter are classified into three groups consisting of switching losses, conducting losses, and capacitor losses which are described as follows.

5. 2. 1. Switching Losses The switching losses are created due to delays in turning on and turning off the switches and reverse recovery time on the diodes. when the pulse reaches the gate of a switch, it takes a t_{on} of seconds for the collector-emitter voltage and collector current to reach their final values. In addition, when the pulse is removed from the gate, it takes a t_{off} of seconds for the switch to turn off. These delays t_{on} and t_{off} cause switching losses on the switches. The switching losses during the on ($P_{sw,on}$) and off ($P_{sw,off}$) states of a typical switch are calculated by Equations (1) and (2), respectively [30].

$$P_{sw,on} = \frac{1}{6} f_s \times V_{off} \times I_{on} \times t_{on} \quad (14)$$

$$P_{sw,off} = \frac{1}{6} f_s \times V_{off} \times I_{on} \times t_{off} \quad (15)$$

where t_{on} and t_{off} are turning on and off time of switches, f_s is the switching frequency, V_{off} is the voltage rating of the switch and I_{on} is the average load current. Moreover, the switching losses on the diodes are calculated as follows:

$$P_{sw,D} = \frac{1}{6} f_s \times V_{RM} \times I_{RM} \times t_B \quad (16)$$

Where V_{RM} and I_{RM} are the maximum voltage and current of the reverse recovery, respectively. In addition, t_B is the delay time of reverse current. The total switching losses are formulated as follows:

$$P_{sw,total} = \sum_{i=1}^{N_{sw}} \left(\sum_{j=1}^{N_{on}} \left(P_{sw,on,ij} \right) + \sum_{j=1}^{N_{off}} P_{sw,off,ij} \right) + \sum_{k=1}^{N_D} \left(\sum_{h=1}^{N_{off}} \left(P_{sw,D,kh} \right) \right) \quad (17)$$

Where N_{sw} and N_D are the numbers of the switch and diode, respectively. Moreover, N_{on} and N_{off} are the numbers of the on and off states of the switch and diode during a fundamental cycle (1/Ts).

5. 2. 2. Conducting Losses Conducting losses are created in the proposed SC topology due to the resistance and voltage drop on the switches and antiparallel diodes during turning on. The average conducting losses for the transistor (P_{cT}) and antiparallel diode (P_{cD}) can be expressed as [31]:

$$\begin{cases} P_{cT} = V_{CEO} I_{c,ave} + R_c I_{c,rms}^{\ 2} \\ P_{cD} = V_{DO} I_{D,ave} + R_d I_{D,rms}^{\ 2} \end{cases} \quad (18)$$

where I_{ave} and I_{rms} represent the average root-mean-square (RMS) values for the collector current. Moreover, V_{DO} and R_d are the forward voltage drop and on-state resistance of the antiparallel diode, respectively. Equation (18) elaborates on the conducting losses for each switch and diode. In another approach, it can be described by each output voltage level. For this purpose, consider Figure 6 in which there are six non-repetitive voltage levels (level 1: $\pm 1V_{dc}$, level 2: $\pm 2V_{dc,}$ level 3: $\pm 3V_{dc}$, level 4: $\pm 4V_{dc}$, level 5: $\pm 5V_{dc}$, and level 6: $\pm 6V_{dc}$) for a 13-level output. Here, the zero level is not considered because it does not produce the conducting losses. By assuming the pure resistive load, the average conducting losses in transistors (P_{cT}) and their antiparallel diodes (P_{cD}) for mentioned six non-repetitive voltage levels can be formulated as follows:

$$\begin{cases} P_{cT,leveli} = \left(k_{Ti} \right) \left[V_{CEO} I_{c,ave,leveli} + R_c I_{c,rms,leveli}^{\ 2} \right] \\ P_{cD,leveli} = \left(k_{Di} \right) \left[V_{DO} I_{D,ave,leveli} + R_d I_{D,rms,leveli}^{\ 2} \right] \end{cases} \quad (19)$$

K_T and K_D coefficients are the numbers of switches and diodes, respectively. For each voltage level, these coefficients have been shown in Table 4.

Eventually, the sum of the conducting losses can be formulated as follows:

$$P_{c,total} = \sum_{i=-6}^{6} \left(P_{cT,leveli} + P_{cD,leveli} \right) \quad (20)$$

5. 2. 3. Capacitor Losses In a capacitor, there are two types of losses. One is conduction losses ($P_{c,r}$) due to inner resistance (R_c) and another is voltage ripple losses ($P_{c,ripple}$). The capacitor voltage ripple losses are created by the difference between the DC bus voltage and the voltage across capacitors in charging mode. These losses are formulated as follows [32]:

$$P_{C,r} = \frac{2\pi f_{ref}}{\pi} \sum_{i=1}^{6} \left(\int_{t_{a,i}}^{t_{b,i}} R_c i_{Ci}^{\ 2} dt \right) \quad (21)$$

$$P_{C,ripple} = \frac{f_{ref}}{2} \sum_{i=1}^{6} \left(C_i \Delta V_{Ci}^{\ 2} \right) \quad (22)$$

where ($t_{a,i}$, $t_{b,i}$) are LDC intervals for the ith capacitor. Thus, capacitor losses are given as follows:

$$P_{loss,cap} = P_{c,r} + P_{C,ripple} \quad (23)$$

using Equations (18), (21), and (24), it can be written the efficiency of the proposed topology as:

TABLE 4. Coefficients of K_T and K_D in each voltage level for a 13-level output

Output level	K_T	K_D
$+1V_{dc}$	4	3
$+2V_{dc}$	6	2
$+3V_{dc}$	4	2
$+4V_{dc}$	6	1
$+5V_{dc}$	5	1
$+6V_{dc}$	7	0
$-1V_{dc}$	4	3
$-2V_{dc}$	4	2
$-3V_{dc}$	5	2
$-4V_{dc}$	5	1
$-5V_{dc}$	5	1
$-6V_{dc}$	5	0

$$\eta = \frac{Pout}{Pin} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + P_{sw,total} + P_{c,total} + P_{loss,cap}} \quad (24)$$

It should be noted that the switching losses in the proposed multilevel inverter can be ignored due to the use of the NLC switching technique. Therefore, for calculating the efficiency, it can be modeled a switch IGBT on the simulation environment which is shown in Figure 7.

Figure 8 depicts the efficiency curve in term of multiple load powers. To bring the results of simulation and experimental efficiency closer, three types of switches with specifications listed in Table 5 are considered.

According to Figure 8, the efficiency of the proposed multilevel inverter with the switch IRG4IBC30 is higher than the other two switches. This is because the V_{CEO} and R_C in the IRG4IBC30 are lower than others. For this reason, in this work, the switch IRG4IBC30 is used in the laboratory setup. Moreover, its model is applied to the simulation results.

6. SIMULATION AND EXPERIMENTAL RESULTS

To validate the proposed SC multilevel inverter topology, several simulations and experimental results are performed for a type 13-level inverter under various impedance loads and LF and HF conditions.

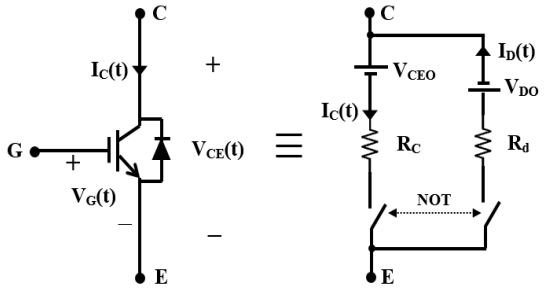


Figure 7. The equivalent circuit of a switch IGBT with an antiparallel diode to calculation of the efficiency

6. 1. Simulation Results In the simulation environment, the DC bus and capacitance parameters are set at (V_{dc}=20v) and (C_{t1}=6300µF, C_{t2}=6300µF, C_f=3300µF, C_m=3300µF), respectively. Moreover, the frequency of the reference signal is set at two values f_s=50Hz and 500Hz. To achieve high-precision processing, the sample time is regulated at 10µs. Figure 9 shows the output voltage and its harmonic spectrum under frequency f_s=50Hz. As shown in this figure, the THD of output voltage is 6.33%, which is less than 8% complying with the IEEE-519 standards. Figure 10 depicts the output parameters under pure resistive load (Z=60Ω) and f_s=50Hz. Firstly, considering that the voltage gain in the proposed topology is equal to 6, the maximum voltage level V_{omax} is close to (6×20=120) volts according to Figure 10(a). Secondly, as shown in Figure 10(b), the peak of load current agrees with ohm law (120v/60Ω=2A).

TABLE 5. The parameters values of the three types of switches IGBT for assessing the efficiency of the proposed topology

Switch IGBT	Antiparallel diode	External antiparallel diode	V_{CEO} (v)	R_C (Ω)	V_{DO} (v)	R_d (Ω)
STGH20N50FI	No	MBRF20100CT	2.5	0.125	0.85	0.085
IRGP35B60	Yes	------	1.85	0.084	2	0..075
IRG41BC30	No	MBRF20100CT	1.4	0.077	0.85	0.085

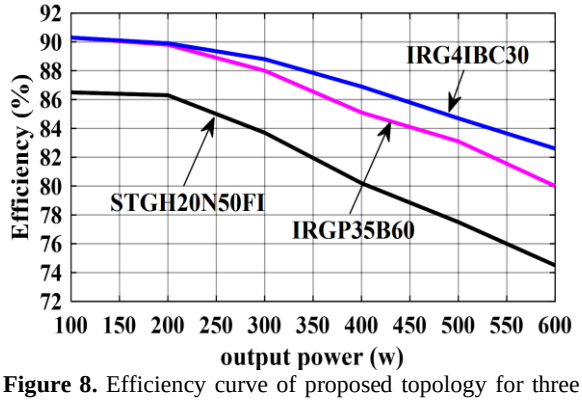


Figure 8. Efficiency curve of proposed topology for three types of IGBT switch

According to Figures 10(c), 10(d), 10(e), and 10(f), the voltage of capacitors C_{t1}, C_{t2}, C_f, and C_m are close to 20v, 20v, 40v, and 40v, respectively to product a 13-level output voltage. Figure 11 shows the output parameters of a 13-level inverter with a change in load impedance from Z=60Ω to Z=30Ω at t=1s under f_s=50Hz. As shown in this figure, the peak of output current has been increased approximately from i=2A to 4A with a fast dynamic behavior. From Figures 11(c), 11(d), 11(e), and 11f, it seems that, with increasing the load, the voltages of the capacitors have been slightly decreased. This is because of the increase in voltage drop on the IGBT switches. Figure 12 depicts the output parameters with a change in impedance load from Z=60Ω to Z=60Ω+100mH at t=1s

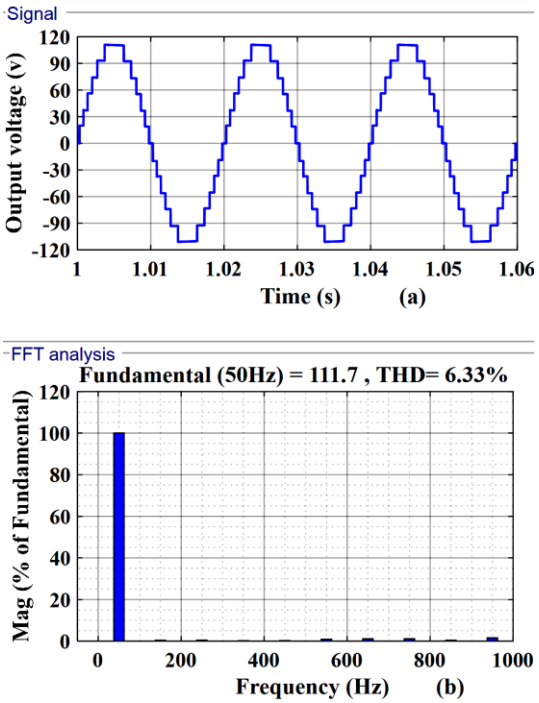


Figure 9. Simulation results for (a) output voltage, and (b) harmonic spectrum of output voltage with f_s=50Hz under NLC switching technique

under f_s=50Hz. For an inverter, the inductive load act as a low pass filter. So, it is expected that the output current is close to a pure sinusoidal waveform. This phenomenon has been clearly seen in Figure 12(b). To evaluate the proposed topology in HF conditions, a simulation result has been performed according to Figure 13 with f_s=500Hz. In this frequency, the output current is strongly diminished when the load is changed from pure resistive to induction case, as shown in Figure 13(b). This is because of the increasing the induction reactance from zero to $X_L=L\omega=(L\times2\times\pi\times500)$ Ω. In other words, in f_s=500Hz, the inductive load impedance is higher than the resistive load.

Moreover, in HF conditions, according to Figures 13(c), 13(d), 13(e), and 13(f), the voltage ripple of capacitors is less than the LF conditions. This issue is compatible with Equations (11), (12), and (13) by considering the capacitances as constant.

6. 2. Experimental Results According to Figure 14, a laboratory system has been provided to implement the proposed13-level inverter topology. The experimental setup contains a DSP, a gate driver circuit, several capacitor banks, the proposed multilevel inverter, multiple power supplies for gate driver circuit, several resistive loads, an inductive load, a current sensor and a

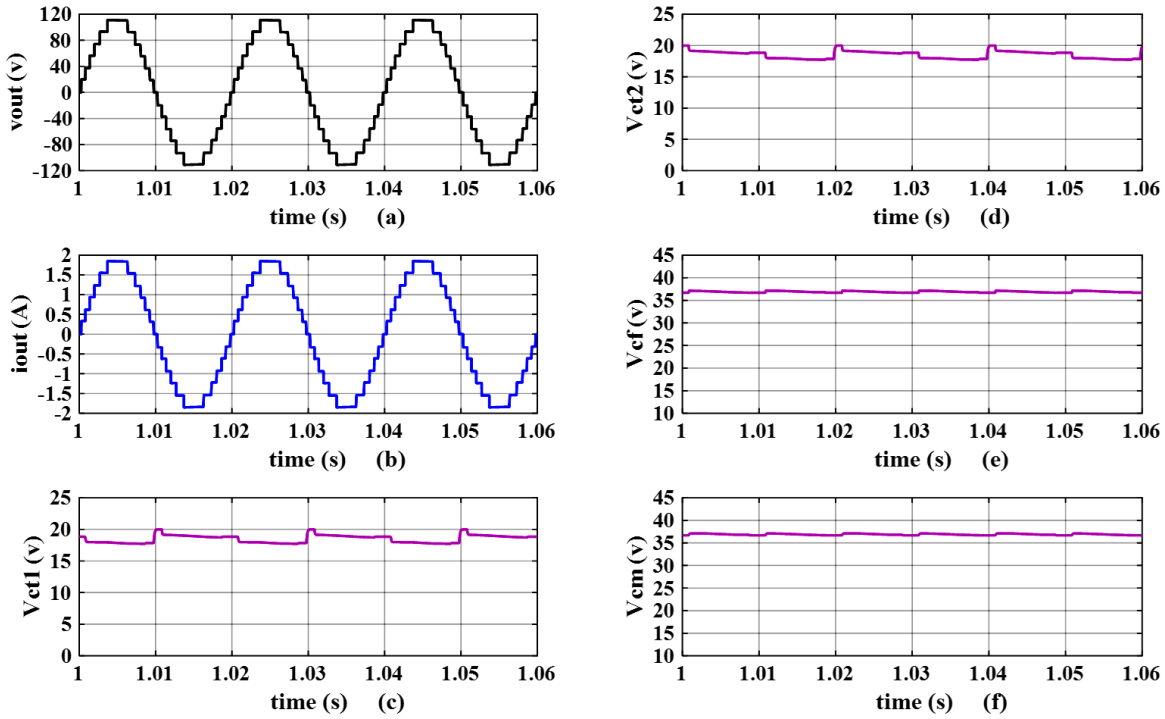


Figure 10. Simulation results for constant pure resistive load (Z=60Ω) under f_s=50Hz. (a) output voltage, (b) output current, (c) capacitor voltage C_{t1}, (d) capacitor voltage C_{t2}, (e) capacitor voltage C_f, and (f) capacitor voltage C_m

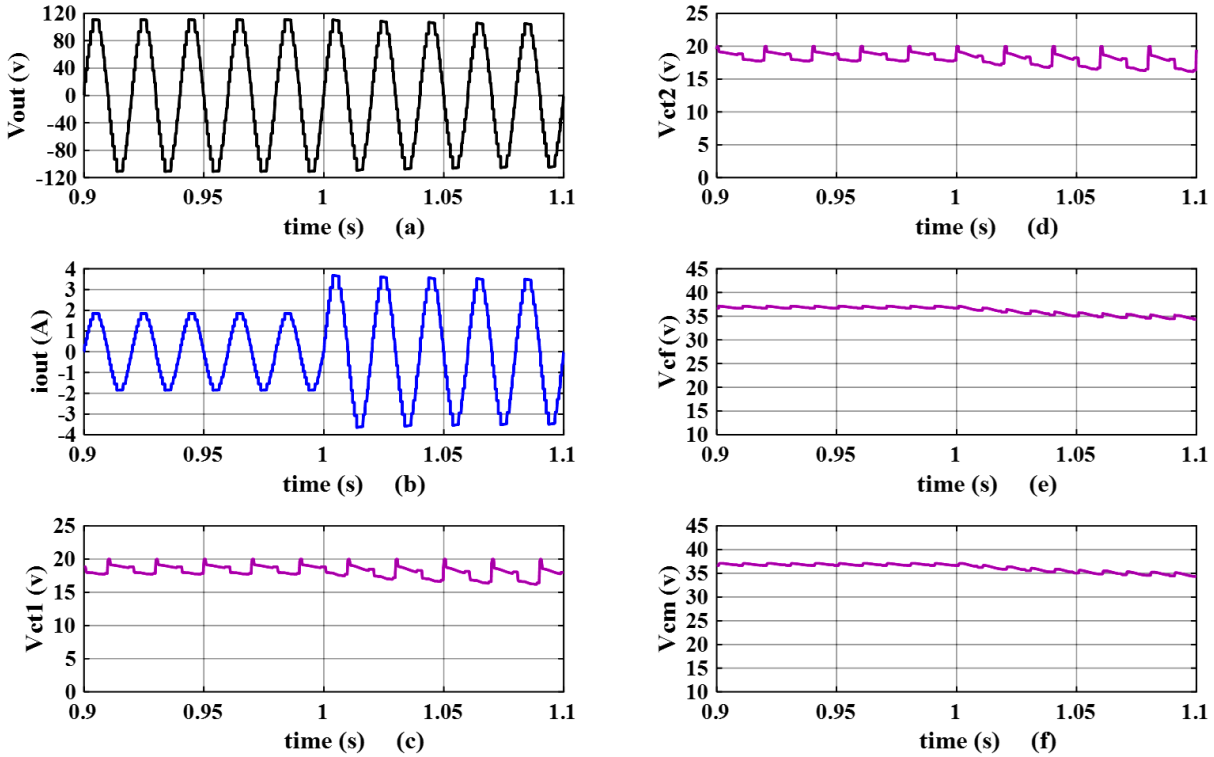


Figure 11. Simulation results under change in pure resistive load from Z=60Ω to Z=30Ω at t=1s under f_s=50Hz. (a) output voltage, (b) output current, (c) capacitor voltage C_{t1}, (d) capacitor voltage C_{t2}, (e) capacitor voltage C_f, and (f) capacitor voltage C_m

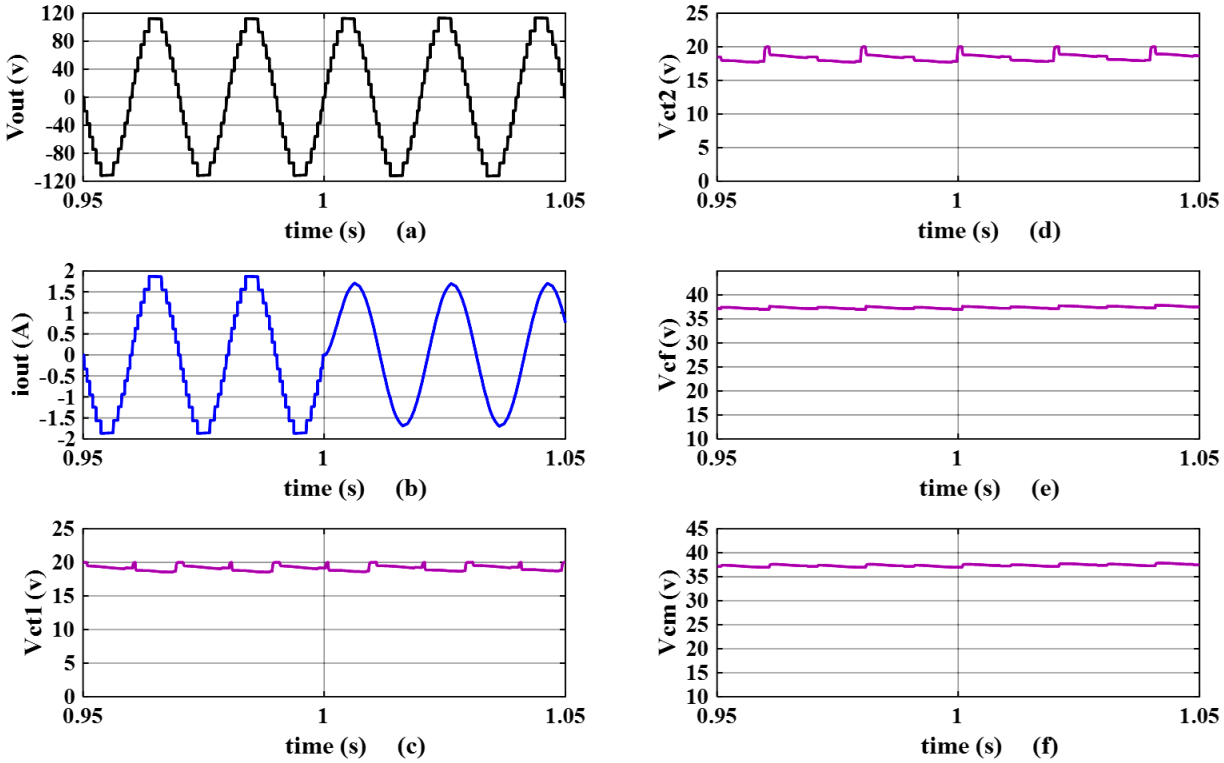


Figure 12. Simulation results under change in impedance load from Z=60Ω to Z=60Ω + 100mH at t=1s under f_s=50Hz. (a) output voltage, (b) output current, (c) capacitor voltage C_{t1}, (d) capacitor voltage C_{t2}, (e) capacitor voltage C_f, and (f) capacitor voltage C_m

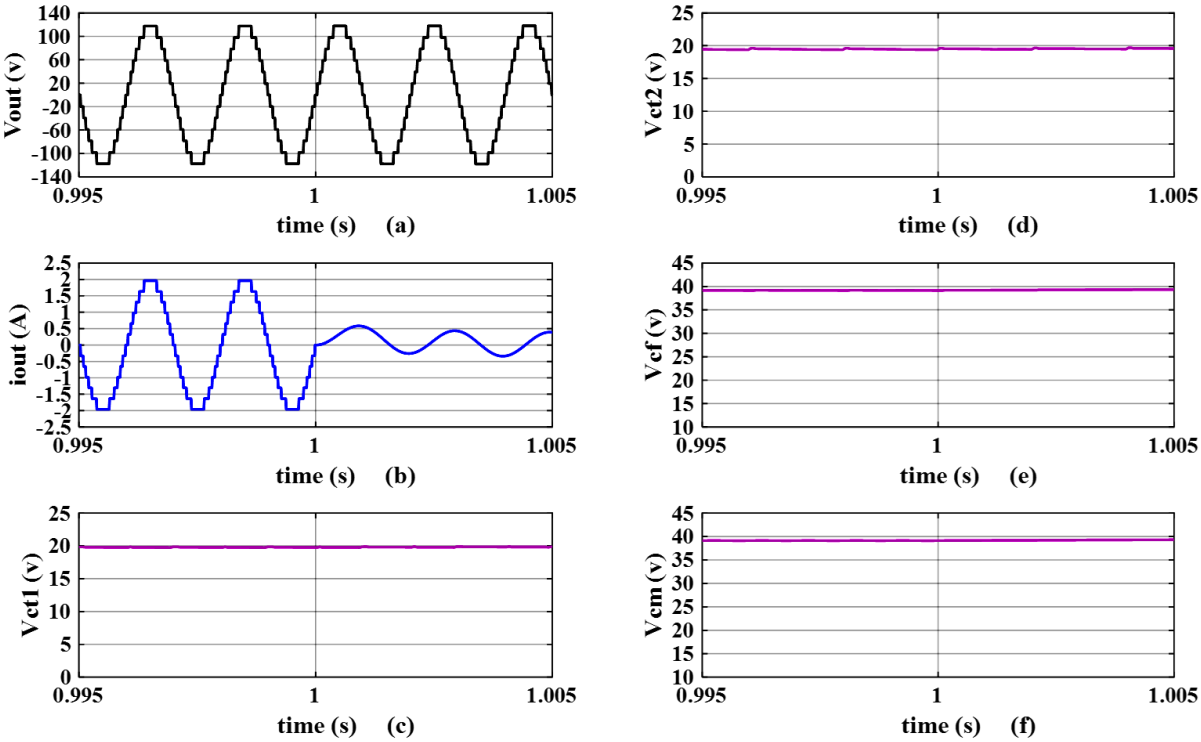


Figure 13. Simulation results under change in impedance load from Z=60Ω to Z=60Ω + 100mH at t=1s under f_s=500Hz. (a) output voltage, (b) output current, (c) capacitor voltage C_{t1}, (d) capacitor voltage C_{t2}, (e) capacitor voltage C_f, and (f) capacitor voltage C_m

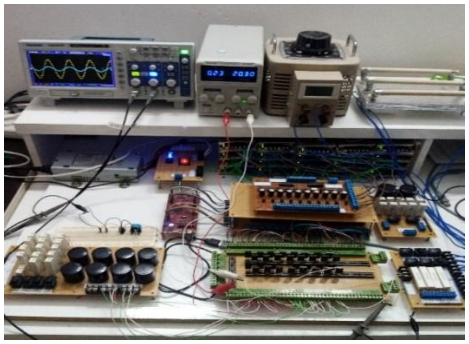


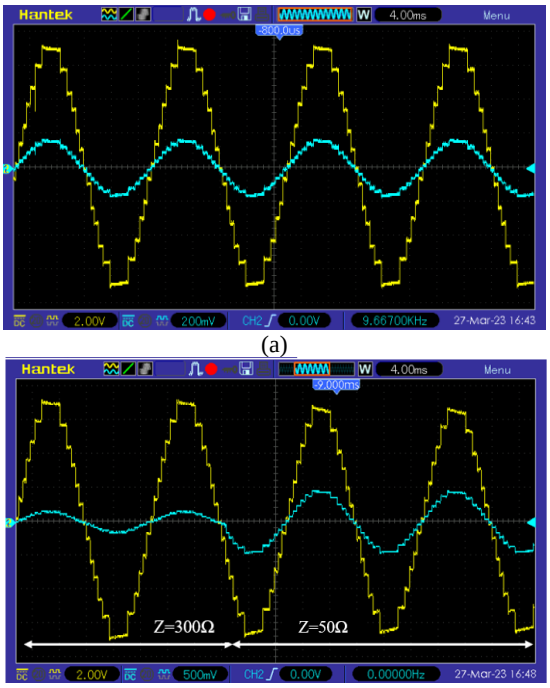
Figure 14. The experimental setup

resistive voltage sensor. The details of the whole system have been listed in Table 6. In the gate driver circuit, there are two groups ICs for transferred pulse gates from DSP to the multilevel inverter. One is 74HC245 buffer and another is HCPL-3120 as the main IGBT driver. The buffer IC is created an infinite impedance between DSP and multilevel inverter which prevents more currents from by the DSP. The most important of the HCPL-3120 is that it acts as isolator and driver, simultaneously. In this study, it has been used a ZMCT103C as the hall-effect current sensor. A prominent feature of this sensor is that its output is isolated from other parts of the setup.

Moreover, to measure the load current, it does not need any interface circuit. Figure 15 shows the experimental results for the output voltage and current under pure resistive load at f_s=50Hz. Generally, when a resistive load is used, the voltage and current have no

TABLE 6. The parameters and devices applied to the laboratory setup

Parameter/ Device	Value/ Type
DSP	TMS320F28379D
V_{dc}	20v
Maximum expected voltage level	120v
Output voltage frequency	50Hz and 500Hz
Capacitors	C_{t1}=C_{t2}=6300μF and C_f=C_m=3300μF
IGBT	IRG4IBC30
Antiparallel diode	MBRF20100CT
Driver	HCPL-3120
Buffer	74HC245
Resistive loads	50Ω and 300Ω
Inductive load	500mH
Current sensor	ZMCT103C (1:4)
Output voltage sensor	Resistive divider (1:15)
Capacitor voltage sensor for V_{cf} and V_{cm}	Resistive divider (1:1.5)



(a)

(b)

Figure 15. Experimental results for output voltage (yellow) and current (blue) with pure resistive load at f_s=50Hz. (a) with constant impedance Z=300Ω. (b) with changing the load impedance from Z=300Ω to 50Ω. To obtain the actual voltage and current values, the vertical axis must be multiplied by factors 15 and 4, respectively (see Table 6).

phase difference from each other and the waveform of the output current is a multilevel form same as the output voltage. Considering table 6, the peak value of the output voltage is about (3.5×2×15=105v).

However, this value is slightly different from the maximum expected voltage level (120v) because of the voltage drop on the IGBTs and diodes in the laboratory setup. As shown in Figure 15(b), the load impedance has increased six times. For this reason, the output current peak has been reached from (0.15×0.5×4=0.3A) to (0.9×0.5×4=1.8A).

Figure 16 depicts the experimental results with a purely inductive load as Z=500mH under f_s=50Hz. In relation to this figure, there are two outstanding points. First, the output current is close to a sinusoidal waveform same as in Figure 12(b). secondly, a 90-degree phase difference has been shown between the output voltage and current.

Figure 17 shows the capacitors voltage waveform of the C_{t1}, C_{t2}, C_m, and C_f under output frequency f=50Hz. According to Figure 6, because the discharging time of the capacitors C_{t1}, and C_{t2} is more than the capacitors C_f, and C_m, the voltage ripple of the capacitors C_{t1} and C_{t2} is more than others which can be seen in Figure 17. From the view of the voltage range, the capacitor's voltages of C_{t1} and C_{t2} are equal to V_1=15v as shown in Figure 17(a).

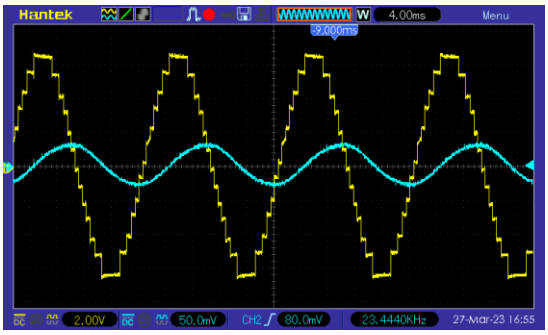
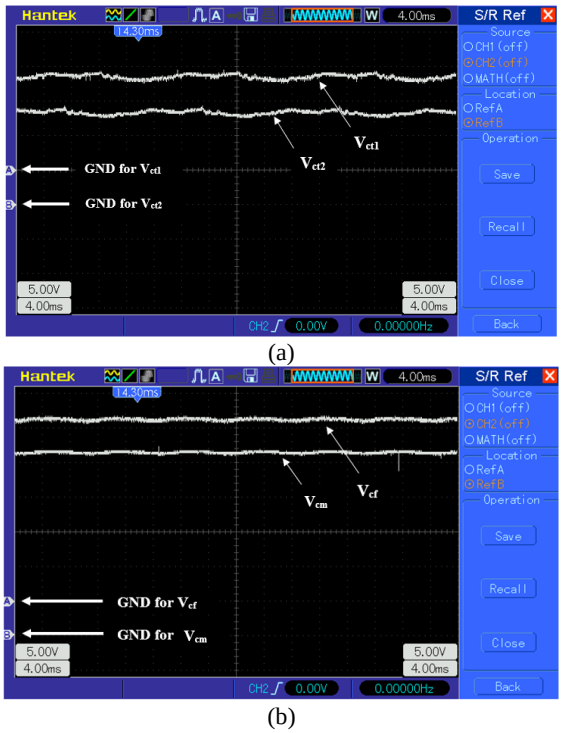


Figure 16. Experimental results for output voltage (yellow) and current (blue) with pure inductive load Z=500mH at f_s=50Hz. To obtain the actual voltage and current values, the vertical axis must be multiplied by factors 15 and 4, respectively (see Table 6)

Moreover, according to Figure 17(b), the capacitor's voltages of C_f and C_m are about V_2=37v. The V_1 and V_2 must be 20v, and 40v, respectively but the voltage drop of the switches and diodes has caused such an issue. For assessing the HF condition, an experimental result is performed at f_s=500Hz which is shown in Figure 18. In this figure, with horizontal zoom, it can be shown that the 13-level waveform is well produced at the output without the voltage levels going out of order.



(a)

(b)

Figure 17. Experimental results for capacitor voltages under pure resistive load at f_s=50Hz. (a) capacitors voltage V_{ct1} and V_{ct2} (b) capacitors voltage V_{cf} and V_{cm}. To obtain the actual voltage value of capacitors C_f and C_m, the vertical axis must be multiplied by factor 1.5 (see Table 6)

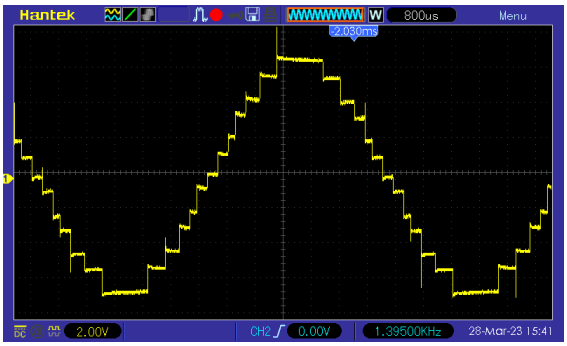


Figure 18. Experimental results for output voltage under pure resistive load at f_s=500Hz

7. CONCLUSION

A new switched-capacitor multilevel inverter based on combined T-type and cross modules without H-bridge was introduced in this work. The proposed topology has the ability to boost as well as modularity with only one DC-link source. In the case of 13-level conditions, the proposed multilevel inverter includes 20 switches and 4 capacitors to produce a voltage gain of 6. In modularity conditions, the PIV of switches remains constant as the number of cross-modules increases. Hence, the TSV and CF can be drastically decreased compared to other topologies. Under the NLC switching technique, the THD of output voltage in the proposed multilevel inverter is 6.33% which conforms to the IEEE standards. The simulation and experimental results confirm the validity of the proposed topology under steady state and transient conditions as well as performance in HF and LF domains.

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Persian Abstract

چکیده

این مقاله یک توپولوژی اینورتر چند سطحی متقارن نوع خازن سوئیچ شده ارائه می‌کند که می‌تواند ولتاژ DC ورودی را به شکل موج AC چند سطحی افزاینده بر روی بار تبدیل کند. این اینورتر چند سطحی پیشنهادی از یک ماژول نوع T و چندین ماژول خازن Cross تشکیل شده است. ساختار اینورتر چند سطحی تعمیم یافته به گونه ای است که ولتاژ پیک معکوس با افزایش تعداد ماژول های خازن ثابت می ماند که این موضوع منجر به کاهش ولتاژ استرس کلیدها و عملکرد هزینه در مقایسه با سایر توپولوژی های سنتی می شود. . ساختار معرفی شده به طور ذاتی می تواند سطوح ولتاژ مثبت، منفی و صفر را در خروجی بدون ساختار H-bridge ایجاد کند. ولتاژهای خازن در ماژول های نوع T و Cross ذاتاً متعادل هستند و سیستم کنترل را تحت استراتژی سوئیچینگ کنترل نزدیکترین سطح (NLC) ساده می کنند. برای تأیید عملکرد توپولوژی پیشنهادی، چندین شبیه‌سازی و نتایج آزمایشگاهی برای یک اینورتر ۱۳ سطحی به ترتیب توسط MATLAB و TMS320F28379D DSP ارائه شده‌اند.