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# Design and Qualitative Analysis of Hetero Dielectric Tunnel Field Effect Transistor Device

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*ABSTRACT*

A Hetero Dielectric Tunnel field effect transistor with the spacer on both sides of the gate is proposed in this paper. The performance and characteristics of Hetero Dielectric Tunnel field effect transistor using the ATLAS Technology Computer-Aided Design in 5nm regime were analyzed. The band-to-band tunneling leakage current will be reduced by introducing heterojunction and hetero dielectric spacer material in the proposed structure. In Hetero Dielectric Tunnel field effect transistor, double metal gate and high-k dielectric spacer improves high on the current and subthreshold swing. The high-k dielectric Hafnium oxide spacer is placed on both sides of the source and drains to import the tunneling mechanism. The proposed device in the 5nm node has improved DC characteristics such as a High ON-state current of 1.68 x 10-5 Amp & OFF-state Current reduced from 7. 83x $10^{-11}$ Amp to 5.13 x $10^{-12}$ Amp and ION / IOFF ratio has increased from 3.22 x $10^{5}$ to 3.27 x 10 compared to conventional dual gate Tunnel field effect transistor. Therefore, this device is suitable for low power applications

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## 1. INTRODUCTION

As the Semiconductor industry leads into nanoscale technology and the device dimensions are continuously downscaling, The Hetero Dielectric Tunnel field effect transistor is the alternative because of its tunneling mechanism, lower leakage current and reduced short channel effect. Several attempts have been made to improve the electrical properties and drain current characteristics of Tunnel Field Effect transistors [1]. Due to its band to band tunneling and vide variety of methods and strategies are developed in the Tunnel Field Effect transistors devices The gate-oxide semiconductor materials being low-k dielectric material such as Silicon Dioxide, high-k dielectric materials as Hafnium oxide and gate-electrodes play vital role in the improvement of electrical and drain current characteristics [2]. The source-side oxide regions of Tunnel Field Effect transistors device will improve on-current, and the drain-side oxide region reduces the off-current. Therefore, the tunneling mechanism occurs in the source-channel region during the on-state condition and same tunneling process will determine the ambipolar off-current [3].

The Nanoscale Tunnel Field Effect transistors is an advanced transistor suitable for digital circuit applications and Radio Frequency applications based on improved drain current characteristics [4]. In Tunnel Field Effect transistors the tunnel width is narrow, therefore electrons can tunnel from the p+ source to the channel for conduction and higher band to band tunneling generation rate. As a result, the channel has more carriers accessible for current conduction. Due to their lower power dissipation, tunnel field-effect transistors are widely used in nanoscale semiconductor devices and can operate at reduced bias voltages [5].

In the reverse bias structure, Tunnel Field Effect Transistor exhibits a miniaturized short channel effect, reduced leakage current, and decreased temperature dependency and has major issues correlated to lower drain current, and lacking in high-frequency applications. To overcome these issues, several techniques were introduced by the researchers as gate overlap and

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underlap engineering on the drain side, source extension engineering, drain extension engineering, gate work function engineering, pocket layer, and hetero dielectric materials to increase the on-current (Ion) [6]. To increase the drain current characteristics all the approaches depend on tunneling narrow width and a large electric field (E). In addition, different heterostructures come up for low band gap semiconductor materials Gallium arsenide, and Indium phosphide to achieve improved current. But due to the complexity of these structures hard to achieve a good on-state current. Due to the large band gap and effective mass, all the Tunnel Field Effect transistors devices provide a lower band-to-band tunneling rate. Therefore, heterostructure Tunneling Field Effect Transistor with low band gap material is preferable to enhance on-state performance characteristics [7].

We proposed a hetero dielectric Tunnel Field Effect transistors device made of Nanomaterial oxide with a spacer to combine all the low-k dielectric material such as Silicon Dioxide and high-k dielectric semiconductor materials such as Hafnium Oxide to achieve good tunneling mechanism and reduce leakage. The high-k dielectric material hafnium oxide and Titanium Dioxide are used as spacer material on both sides of dual metal gate to improve device drain current (Id) [8]. The lower bandgap should increase the device drain current characteristics whereas the higher band gap should reduce the ambipolar current in the device. Due to lower operating voltage, the Ion/Ioff ratio decreases. Therefore, we applied spacer material as high-k dielectric material being hafnium oxide on both sides of the dual metal gate and having smaller tunneling bandgap has been introduced in the proposed device [9].

In this paper, we have considered spacer engineering on both sides of a dual gate with a high-k dielectric material as hafnium oxide along with hetero dielectric and hetero junction engineering techniques and Nanomaterial oxide materials to improve Ion current and lower the ambipolar current. Due to the spacer engineering technique, the drain-channel interface could be suppressed because of increased depletion width. In the proposed device hetero dielectric material is used to modulate the tunneling barrier at source-channel and drain channel interfaces. High-k dielectric material Hafnium oxide is chosen for improved results. The drain current characteristics of the device have been carried out and compared with other models such as Conventional - Tunnel Field EffectTransistor, Dual Gate- Tunnel Field Effect, and Hetero junction Dual Gate - Tunnel Field Effect. The simulations have been performed and extracted using the Silvaco Technology Computer Aided Design simulator [10].

The organization of the paper is as follows: The proposed Nanoscale device, its models, methods, and device parameters are presented in second section. The third section presented results and discussion of drain current characteristics such as ion current, Ioff current, and Ion/Ioff ratio. The final section is presented as conclusion.

## 2. STRUCTURE

Figure 1 shows 2-Dimensional view of conventional Tunnel Field Effect transistor with Hafnium Oxide, Silicon Dioxide , and Nanomaterial oxide materials are utilized for the design. The device dimension (Wd) is 60 nanometers long and gate length (Lg) of 5 nanometers, a source length (Ls) of 27.5 nanometers, a drain length of 27.5 nanometers, and a channel length of 5 nanometers. The symmetric dual metal gate is connected on top and bottom with oxide material with Silicon Dioxide. 5nm channel length is connected equally from source and drain terminals [11].

Figure 2 shows the 2-Dimensional view of Dual Material Gate Tunnel Field Effect transistor where the materials such as Hafnium Oxide , Silicon Dioxide , and Nanomaterial oxide materials are used. An asymmetric dual metal gate is connected on top and bottom with oxide material with Silicon Dioxide. 5nm channel length is connected equally from source and drain terminals [12].

Figure 3 shows the 2-Dimensional view of view of High-k Dielectric material with Hafnium Oxide Spacer. The material utilized for the spacer in this Spacer Tunnel Field Effect Transistor is Hafnium Oxide [11, 12]. Spacers are used at the top and bottom gates of the source side and drain side. The spacers are 7nm long and 2nm wide, with a length of 7nm and a width of 2nm are utilized in Silvaco TCAD tool along with Nanomaterial oxides [13].

Figure 4 depicts the 2-Dimensional view of structure of the Hetero–Dielectric Tunnel Field Effect Transistor

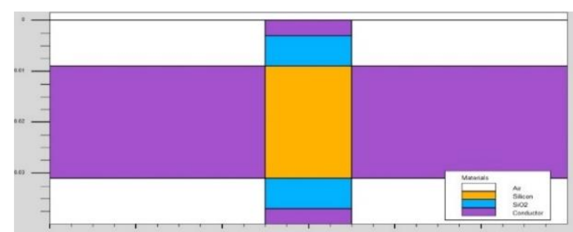


**Figure 1.** Structure of Conventional device

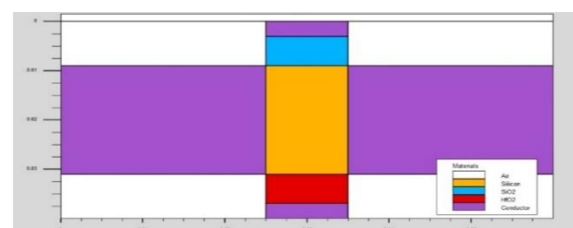


**Figure 2.** Structure of Dual Material Gate Tunnel Device

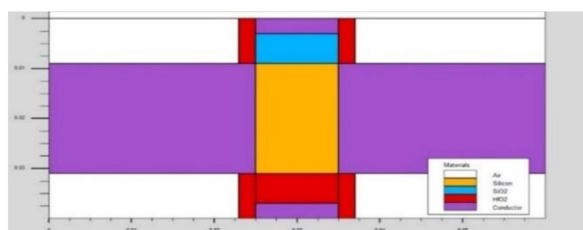

**Figure 3.** Structure of Spacer Tunnel Device

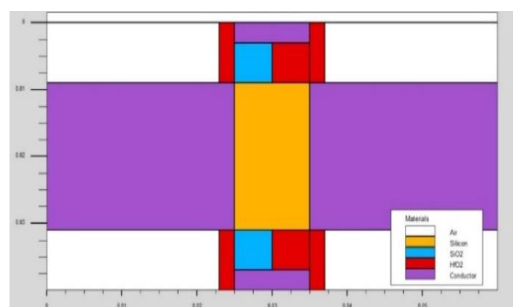


**Figure 4.** Proposed device

in this structure interface layer improves contact between the semiconductors [14]. The device dimension (Wd) is 60 nanometers long, with a gate length (Lg) of 5 nanometers, source length (Ls) of 27.5 nanometers, and drain length of 27.5 nanometers. The material utilized for the Spacer is Hafnium Oxide. Spacers are used at both sides of the source and the drain. The spacers are 7nm long and 2nm wide, with a length of 7nm and a width of 2nm [15].

In the above architectures, a lightly doped channel is employed with a $1\times 10^{16}$ $cm^{-3}$ doping concentration, and an increased doping concentration of $5\times 10^{19}$ $cm^{-3}$ is employed in the channel to introduce spacer at the end of the source side with the implantation method in the fabrication process for adopting channel engineering.

Table 1 shows the effective parameters used to simulate the Hetero Dielectric- Dual Material Gate Spacer Tunnel Field Effect Transistor device using the Silvaco tool. The on-state current and off-state current of various architectures and variations of channel length are shown in Tables 2, 3 and 4.

In Symmetrical Dual-k Hetero– Dielectric Tunnel Field Effect Transistor, the length ratio of Hafnium oxide and Low-k is varied from 1:14 to 14:1 over the total spacer length of 10nm. The spacer length of Hafnium oxide and Low-k plays a significant role in describing the electrostatics of a gate-S/D underlap in the device. For underlap architecture, high-permittivity (k) spacer material modulates the charge transport dynamics inside the channel and the underlap region.

The technical report of the proposed device is analyzed with a 2D simulation tool SILVACO for striving design. To obtain the optimum structure of the device, enhanced meshing is used to design the device.

**TABLE 1.** Used Parameters for the proposed structure

| Parameter | Proposed Values |
|---|---|
| Device Length($W_L$) | 60nm |
| Gate Length($L_G$) | 10nm |
| Source Length($L_S$) | 25nm |
| Drain Length($L_D$) | 25nm |
| Channel Length($L_C$) | 10nm |
| Doping of Source($D_S$) | $1x10^{17}$ $cm^{-3}$ |
| Doping of Drain($D_D$) | $1x10^{18}$ $cm^{-3}$ |
| Doping of Channel($D_C$) | $1x10^{20}$ $cm^{-3}$ |
| Metal Gate Work Function($W_F$) | 4.8eV |
| Thickness of $SiO_2$ | 2nm |
| Thickness of $HfO_2$ | 3nm |

The Two-Dimensional graphical representation of the proposed dielectric material Spacer Tunnel Field Effect Transistor is extensively used for low power digital applications due to its improved performance parameters.

The originality of the proposed structure is designed from one to one i.e conventional Tunnel Field Effect Transistor, dual material gate, symmetrical spacer material and hetero dielectric Tunnel Field Effect Transistor with length of dual gate is 5nm and thickness of each oxide layer 2nm, 3nm using Silvaco tool.

The future prospect of the proposed device could be designed with Low-k source side Asymmetric Spacer Halo doped Tunnel Field Effect Transistor, then there is a 74% reduction in gate capacitance and 31% reduction in intrinsic Delay

The proposed dual material hetero dielectric spacer Tunnel device is invented using Silvaco tool with gate length of 5nm. In this model both high-k and low-k materials are symmetrical. Therefore, the drain current characteristics of proposed model is higher than the existed models.

## 3. RESULTS AND DISCUSSION

**3. 1. Drain Current** The following equation is used to drain current of any conventional device:

I drain –sat= z b(x) q n(x) v(x)

where z is channel width, b(x) is effective depth of the channel, q is electron charge, n(x) is electron density, and v(x) is electron velocity.

The drain current and gate voltage characteristics of the proposed device Hetero– Dielectric -Dual Material Gate Tunnel Field Effect Transistor for varied Gate lengths of 5nm, 7nm, 10nm, and 15nm are shown in Figure 5. The drain current of the proposed device increased as the length of gate is reduced [16-18]. Figure

6 shows that the proposed device drain current Vs gate voltage, where the drain current of the device is higher than the conventional device and it has high drain current characteristics [19].

In Figure 7, the Hetero– Dielectric -Dual Material Gate –Tunnel Field Effect Transistor device's $I_{ON}$ to Ioff ratio rises with increasing high-k dielectric length up to 5 nm. Because of a significant increase in ON-state current, the current ratio has increased exponentially. However, as Ioff and saturated Ion increase above 5 nm, the ratio decreases significantly. As a result, the lengths of Hafnium dioxide and Silicon dioxide dielectric materials are 5 and 10 nanometers, respectively.

Figure 8 depicts the effect of Hafnium dioxide Spacer length variation on the suggested structure's transfer properties. As the Spacer length of Hafnium dioxide is increased, on current (Ion) increases to 5 nm, and then drain current (Id) increases at lengths of 7nm and10 nm. Because the tunneling barrier width at the channel-drain interface is reduced, the ambipolar current steadily increases. We chose 10 nm and 20 nm for the Hafnium dioxide and Silicon dioxide layers, respectively, to retain a greater Ion/Ioff ratio without impairing the Hetero–Dielectric –Dual Material Gate-Tunnel Field Effect Transistor structure's OFF current. The adjusted 5nm gate length is proposed for this structure, because of improved performance characteristics [20].

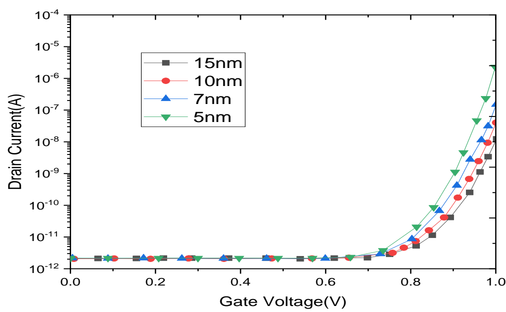


**Figure 5.** Drain current versus Gate voltage with different Gate length

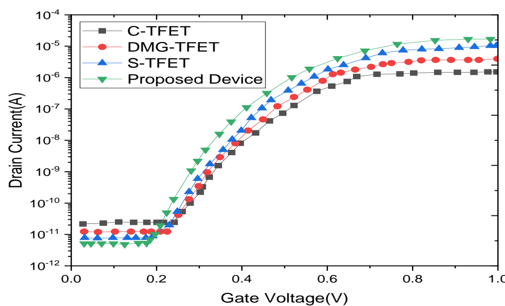


**Figure 6.** Drain current versus Gate voltage for different structures

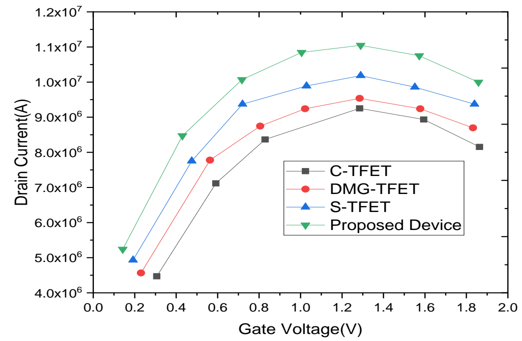


**Figure 7.** Variation of on current for different structures

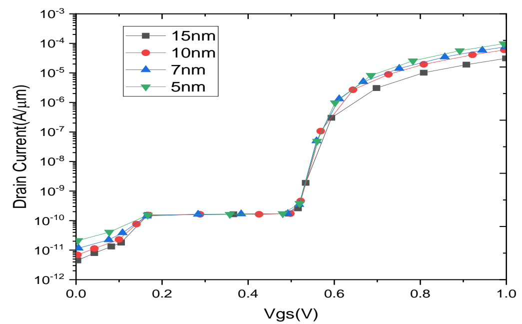


**Figure 8.** Drain current versus Gate voltage with Spacer material

Due to the applied narrow band gap material as silicon dioxide on the source side, the heterojunction Tunnel Field Effect Transistor demonstrates improved band bending is shown in Figure 9. Based on high-k dielectric materials such as Hafnium oxide at the tunneling side, the width of Hetero Dielectric-Dual Material Gate- Tunnel Field Effect Transistor is reduced when compared to other structures [21, 22]. As a result, a large number of carriers can tunnel from the source to the channel region, resulting in a greater on-state current. Because of an increase in depletion width in the drain area, both Dual Material Gate- Tunnel Field Effect Transistor and Spacer-Tunnel filed effect transistor exhibit reduced band bending. On the drain side of the Hetero– Dielectric -Dual Material Gate –Tunnel Field Effect Transistor, Silicon dioxide also reduced.

**3. 2. Electric Field** Figure 10 shows the electric field distribution of proposed device with device length in state condition (Vgs = 1.5V) and ambipolar voltage (Vgs = 1.5V) states. Due to the electric field crowding effect, the breakdown should be happening at the gate nearer the drain. Hence the electric field concentration has increased compared to conventional devices. Based proposed structure, the electric field concentration is more compared to the electric field distribution of other

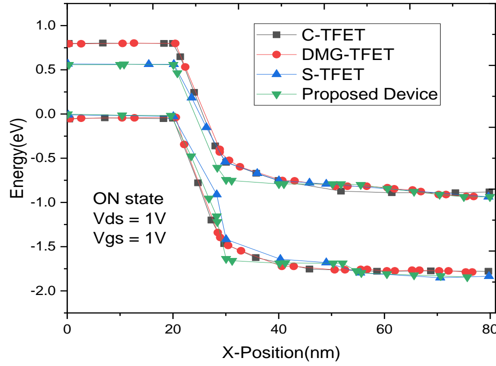


**Figure 9.** Energy band diagram of the proposed device

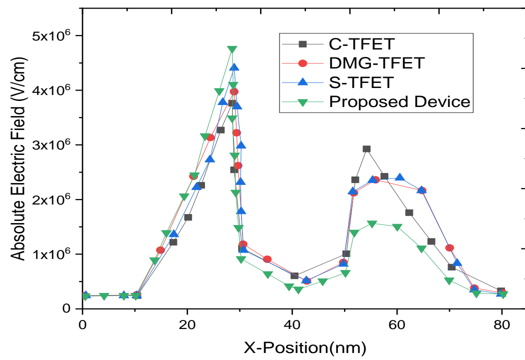


**Figure 10.** Absolute electric field of proposed device

devices [23]. The reduction in the tunneling barrier width in heterojunction Tunnel Field Effect Transistor s results in a greater electric field along the source-channel interfaces, as shown in the figure. The use of Hafnium oxide as a dielectric in the source channel when compared to previous simulated structures, the suggested Hetero– Dielectric –Dual Material Gate –Tunnel Field Effect Transistor has less ambipolar behavior [24, 25].

**3. 3. Transconductance** The Trans conductance versus Gtae voltage for different structures are shown in Figure 11. The proposed device attains the highest packing density due to better current flow in the device. Hence this structure provides more improvement in transcondutance. To achieve proper gain of device high transconductance is needed and calculated. Using the Silvaco tool transistor characteristics simulations are performed dielectric is used, resulting in less band-to-band tunneling process will exist [26].

The higher drain current driving power of charge carriers, gm increases exponentially with an increase in gate bias. Because of higher drain current (Id), heterojunction Tunnel Field Effect Transistor has a higher gm value than Dual Material Gate-TFET and Spacer-Tunnel Field Effect Transistor. However, due to mobility degradation, it decreases with a bigger magnitude of gate bias. Another essential measure for estimating device efficiency is the transconductance generation factor [27, 28]. Transconductance generation factor demonstrates the efficiency with which current can be converted into transconductance (speed).

$$Transconductance\ (G_m) = \frac{\partial I_{ds}}{\partial V_{gs}} \quad (1)$$

The performance Improvements of proposed hetero dielectric structure compared with on current, leakage current and its ratio for three different devices are shown in Table 2. Based on comparison on current is increases, leakage current reduces and its ratio is increases. Therefore, the proposed device performance parameters are improved compared to previous devices (Tables 3 and 4) [29, 30].

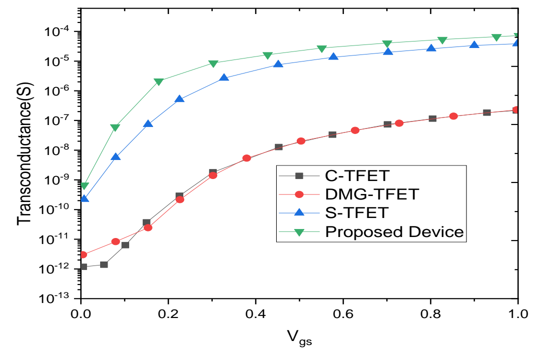


**Figure 11.** Comparison of Transconductance for the proposed device

**TABLE 1.** On current and off current for different Structures

| Architecture | IOFF | ION | ION/IOFF |
|---|---|---|---|
| C-TFET | 2.17E-11 | 1.51E-6 | 6.95E+4 |
| DMG-TFET | 1.23E-11 | 3.97E-6 | 3.22E+5 |
| S-TFET | 7.83E-12 | 1.03E-5 | 1.31E+6 |
| Proposed Device | 5.13E-12 | 1.68E-5 | 3.27E+6 |

**TABLE 2.** Comparison of on current and off current for the hetero structure

| Architecture | IOFF | ION | ION/IOFF |
|---|---|---|---|
| C-TFET | 1.00E-9 | 7.44E-8 | 7.44E+1 |
| DMG-TFET | 6.25E-11 | 7.65E-8 | 1.22E+3 |
| S-TFET | 1.23E-11 | 1.90E-5 | 1.54E+6 |
| Proposed Device | 7.03E-12 | 3.52E-5 | 5.00E+6 |

**TABLE 4.** On current and off current for the proposed device with the variation of Gate Length

| Gate Length | IOFF | ION | ION/IOFF |
|---|---|---|---|
| 15nm | 2.05E-12 | 1.23E-8 | 6.00E+3 |
| 10nm | 2.05E-12 | 4.02E-8 | 1.96E+4 |
| 7nm | 2.15E-12 | 1.49E-7 | 6.93E+4 |
| 5nm | 2.15E-12 | 2.27E-6 | 1.03E+6 |

## 4. CONCLUSION

In this paper, we have designed and analyzed the DC performance analysis of Hetero– Dielectric Tunnel Field Effect Transistor (Hetero Dielectric -Nanowire-Tunnel Field Effect Transistor) with spacer using Silvaco tool in sub 5nm node. The high-k dielectric material hafnium oxide as spacer material is placed on both sides of the dual metal gates. The impact of the proposed device is to reduce the ambipolar current and significantly increase the drain current compared to dual gate Tunnel Field Effect Transistor. The proposed structure with potential high-k dielectric material being hafnium oxide, as a spacer on both sides of the gate has improved better performance over conventional Dual gate Tunnel Field Effect Transistor. Due to maximum drain currents (Id), less sub-threshold swing (SS), lower leakage current (Ioff), greater trans conductance (gm), and larger drain conductance (℧) the proposed Hetero Dielectric-Nanowire –Tunnel Field Effect Transistor is useful in low power applications

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Persian Abstract

**چکیده**

در این مقاله یک ترانزیستور اثر تونل دی تریک هترو با اسپیزر در دو طرف دروازه پیشنهاد شده و ویژگی های عملکرد آن را با استفاده از طراحی به کمک کامپیوتر فناوری اطلس در رژیم 5nm مورد تجزیه و تحلیل قرار داده است .جریان نشت تونل زنی باند به باند با معرفی مواد هتروجکشن و اسپیزر دی هترو دی تریک در ساختار پیشنهادی کاهش خواهد یافت .در ترانزیستور اثر میدان تونل دی هترو دی تریک، دروازه فلزی مضاعف و اسپیزر دی لوکتریک با k بالا بر روی نوسان جریان و زیرمدارندگی بهبود می یابد .اسپیزر اکسید دی تریک بالا K هافنیوم (IV) در دو طرف منبع قرار می گیرد و تخلیه می شود تا مکانیسم تونل زنی وارد شود .دستگاه پیشنهادی در گره 5nm ویژگی های DC مانند جریان حالت ON بالا Amp & OFF-state Current $1.68 \times 10^{-5}$ را از 7 کاهش داده است $83 \times 10^{-11}$ .آمپر به $5.13 \times 10^{-12}$ آمپر و ION / IOFF نسبت از $3.22 \times 10^{5}$ به $3.27 \times 10^{6}$ نسبت به ترانزیستور میدان تونل دروازه دوگانه معمولی افزایش یافته است .بنابراین این دستگاه برای کاربردهای کم توان مناسب است.