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A Novel 19-Level Boost Type Switched-capacitor Inverter with Two DC Sources and Reduced Semiconductor Devices

F. Sagvand, J. Siahbalaee*, A. Koochaki

Department of Electrical Engineering, Aliabad Katoul Branch, Islamic Azad University, Aliabad Katoul, Iran

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ABSTRACT

In this paper, a novel voltage-boosting switched-capacitor multilevel inverter (SCMLI) capable of producing 19 voltage levels using a combination of only 10 switches, 4 diodes, 2 capacitors, and 2 DC sources has been proposed. The main features of the proposed topology are 1) utilization of a very low number of devices, 2) very low Total Standing Voltage (TSV) equal to 6.55 and 3) self-balance property of the capacitors' voltages. In order to provide the IGBTs of the circuit with the desired switching signals, the Nearest Level Control (NLC) method has been adopted. To clarify the benefits of the designed topology as to the total quantity of switches, DC sources, capacitors as well as the total standing voltage (TSV), and converter boosting, a thorough comparison has been carried out versus the recently published 19-level topologies. Also, for the purpose of performance evaluation and validation, the suggested topology has been tested against various loads through an experimental setup in the laboratory using TMS320F28379D DSP as the processor. The comparative, simulation, and experimental results all imply the superiority of the proposed topology against its predecessor counterparts.

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1. INTRODUCTION

In recent years, multilevel inverters (MLIs) have been developed in form of DC to AC converters for numerous applications including renewable energy conversion systems, electric vehicles, AC tractions, high-voltage direct current (HVDC) transmission systems, distributed power generation systems, etc. [1-3]. Compared to two-level inverters, the primary benefits of MLIs are smaller dv/dt tensions, larger operational voltage using devices of a lower rating, reduced total harmonic distortion (THD), low switching frequency, and improved efficiency [4]. For powers of medium and higher ranges, the conventional two-level inverters are now substituted by such elementary MLIs as the flying capacitor (FC) inverters, neutral point clamped (NPC) inverters, modular multilevel converters (MMC), and cascaded H-bridge (CHB) inverters. Nevertheless, in order to attain a high number of output voltage levels, these conventional MLIs require more semiconductors (switches and diodes), capacitors, and DC sources [5-7]. To overcome these issues, researchers have proposed several switched-source (SSMLI) and switched capacitor multilevel inverters (SCMLI) which need a lower quantity of devices to provide more voltage levels [8-14]. Although SSMLI topologies can give rise to structures consisting of only a few devices they are not able to provide a voltage boost on the output inverter. Lately, designs founded on the SCMLI technology, in which serial/ parallel arrangements of electrical and electronic modules are utilized, have been the focus of attention, especially where voltage boost is a necessary feature. Naik et al. [13] designed a 7-level inverter using ten switches and one capacitor which could raise the output voltage up to 1.5 times. Khoun Jahan et al. [15] considered a CHB and substituted several of its DC sources with capacitors which led to the usage of only one DC source in the inverter's structure. Hussan et al. [16] came up with a boost inverter of gain 6, however, it cost 29 switches and a Total Standing Voltage (TSV) equal to 34. As an improvement, Taghvaie et al. [17] lowered this number to 19 switches for the same voltage

*Corresponding Author Institutional Email: ja_siah@yahoo.com
(J. Siahbalaee)

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gain at the cost of a TSV equal to 39. A new inverter design with 55 voltage levels using 7 capacitors and 3 asymmetrical DC sources was suggested by Taghvaie et al. [18]. However, the existence of many modules, in this case, means risking the circuit reliability. Samadaei et al. [14] introduced a 7-level voltage inverter of high voltage gain using 2 capacitors along with 12 switches. More examples of SCMLI topologies with a low number of devices and self-balancing capabilities can be found in literature [19-23]. This article proposes an SCMLI design based upon fewer number of components which provides a quite low TSV. Here, 10 switches are combined to keep the TSV of the circuit as low as 6.55. A modest version of the Nearest Level Control (NLC) method is adopted for switching signals provisioning of the IGBTs. The primary findings of the suggested inverter design can be summarized as,

a) 19 voltage levels using only 10 switches and two DC sources.
b) A 19-level voltage on load gives a multilevel inverter with high-power quality and low cost function.
c) A voltage gain of 2.25 at the output.
d) Self-balance of the two capacitor voltages which makes the control circuitry as simple as possible.

The rest of the paper is as follows. The suggested topology along with its different operational modes have been presented in section 2. The charge and discharge modes of the capacitors, which are to be maintained in balance, suitable measures for choosing the capacitors, and power losses study will be brought in section 3. In section 4, the NLC technique as the intended switching method for IGBTs will be explained. A comparison of the suggested topology against a number of recently published MLIs has been conducted in section 5, regarding the utilized components, voltage gain, TSV, and cost function. Simulation as well as experimental results, aimed to provide illustrations of the suggested topology's feasibility and performance under different loading conditions, will be given in section 6. Finally, section 7 concludes the paper.

2. THE SUGGESTED INVERTER TOPOLOGY

Figure 1 illustrates the suggested scheme. This structure is combined of two capacitors (C_1, C_2), two DC voltage sources (u_1, u_2), ten switches (S_1, S_2, S_3, S_4, S_5, S_6, T_1, T_2, T_3, T_4) and four power diodes (D_1, D_2, D_3, D_4). The capacitors maintain their balance against each other. They will be charged up to the intended level for numerous instances of a fundamental cycle according to the series-shunt balancing rule of voltage. Here, electric charges of C_1 and C_2 must be Vdc and 4Vdc, respectively to achieve 19 levels of voltage from -9Vdc to +9Vdc. The projected turning on/off order of switches as well as the charge and discharge states of the capacitors' are summarized in Table 1.

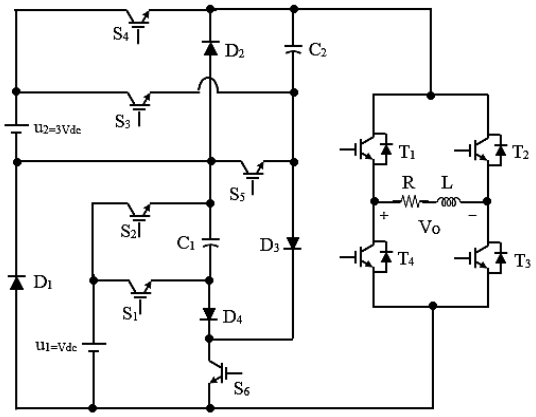


Figure 1. The suggested topology for the 19-level inverter

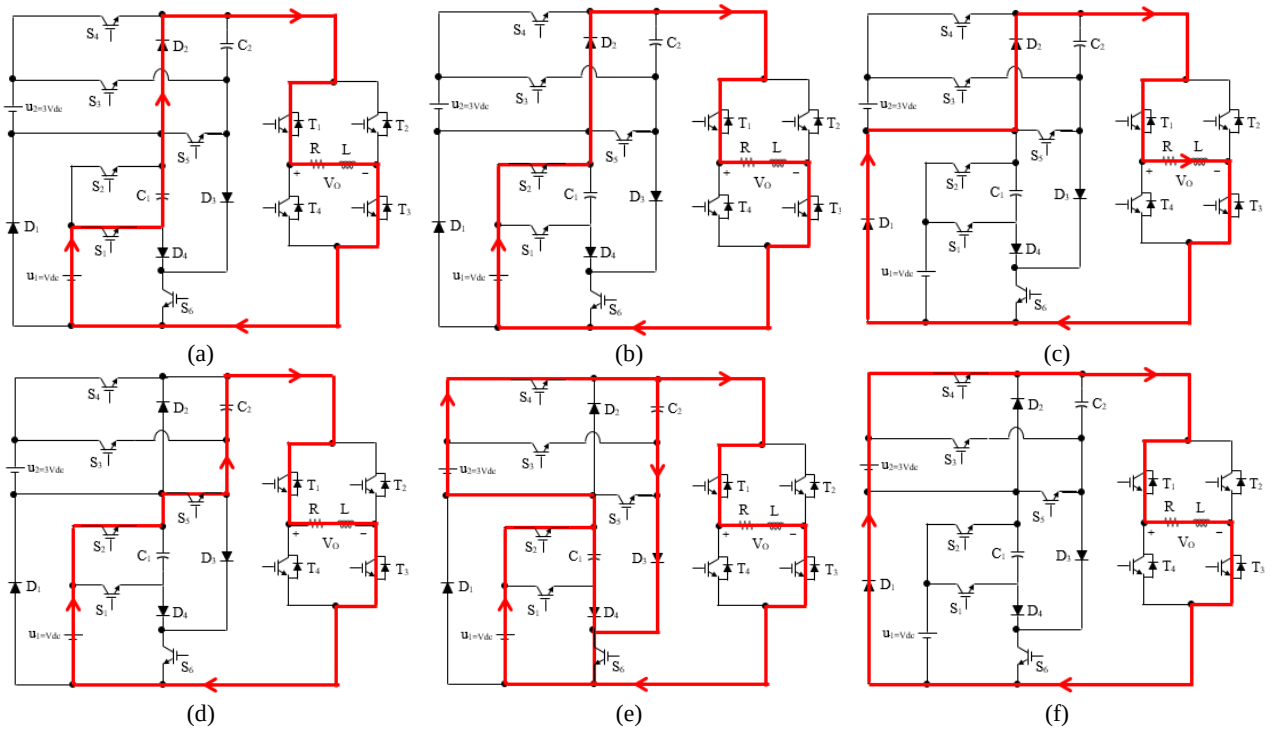
The current flow path towards load (red lines) throughout the positive half cycle and level zero are given in Figure 2. The voltage of level zero would be resulted by switching D_1, D_2, T_1, and T_3 on, as depicted in Figure 2(a). The level +Vdc is formed by turning on the S_2, T_1, and T_3 through diode D_2; at this moment, tuning the S6 on will raise the C1's voltage by Vdc, as shown in Figure 2(b). According to Figure 2(e), when the voltage of level +4Vdc is transferred to the load, the capacitor C2 will be charged to the sum voltage of the DC sources (+4Vdc) through S_2, S_4, D_3, and S_6. The remaining states will be analyzed in a similar way. In order to create the negative levels, switches T_2 and T_4 must be turned on instead of T_1 and T_3. It should be noted that, while diodes D_3 and D_4 maintain the capacitors' charges through a closed loop path, diodes D_1 and D_2 will transfer the voltage levels over to the output.

3. CAPACITOR SIZING AND POWER LOSSES ANALYSIS

3. 1. Capacitor Sizing Within the suggested SCMLI, there are two capacitors as well as two DC sources to provide 19 levels of voltages. As maintained before, the capacitors' voltages are leveled up with each other to the intended potential via the parallel linkage of the voltage source and capacitor over the interval of a fundamental cycle of switching. While C_1 maintains the same potential as the source u_1 (V_{dc}), C_2's potential will raise to the sum of the sources' voltages (4Vdc). The charge and discharge stages of C_1 and C_2 are depicted in Figure 3. The ideal capacitor sizing, then, is determined by their Largest Discharge Cycle (LDC) and load current (i_L). Over the duration of LDC, the charge variations of C_1 and C_2 are as:

TABLE 1. The Switching Orders and Capacitors States in the Suggested 19-level designed inverter

State	S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	D_1	D_2	D_3	D_4	C_1	C_2	V_{out}
1	0	0	0	0	0	0	1	0	1	0	on	on	off	off	---	---	0
2	0	1	0	0	0	0	1	0	1	0	off	on	off	on	---	---	$+V_{dc}$
3	1	0	0	0	0	0	1	0	1	0	off	on	off	off	D	---	$+2V_{dc}$
4	0	0	0	1	0	0	1	0	1	0	on	off	off	off	---	---	$+3V_{dc}$
5	0	1	0	1	0	1	1	0	1	0	off	off	on	off	C	C	$+4V_{dc}$
6	0	1	0	0	0	0	1	0	1	0	off	off	off	off	---	D	$+5V_{dc}$
7	1	0	0	0	1	0	1	0	1	0	off	off	off	off	D	D	$+6V_{dc}$
8	0	0	1	0	0	0	1	0	1	0	on	off	off	off	---	D	$+7V_{dc}$
9	0	1	1	0	0	0	1	0	1	0	off	off	off	off	---	D	$+8V_{dc}$
10	1	0	1	0	0	0	1	0	1	0	off	off	off	off	D	D	$+9V_{dc}$
11	0	1	0	0	0	0	0	1	0	1	off	on	off	on	---	---	$-V_{dc}$
12	1	0	0	0	0	0	0	1	0	1	off	on	off	off	D	---	$-2V_{dc}$
13	0	0	0	1	0	0	0	1	0	1	on	off	off	off	---	---	$-3V_{dc}$
14	0	1	0	1	0	1	0	1	0	1	off	off	on	off	C	C	$-4V_{dc}$
15	0	1	0	0	0	0	0	1	0	1	off	off	off	off	---	D	$-5V_{dc}$
16	1	0	0	0	1	0	0	1	0	1	off	off	off	off	D	D	$-6V_{dc}$
17	0	0	1	0	0	0	0	1	0	1	on	off	off	off	---	D	$-7V_{dc}$
18	0	1	1	0	0	0	0	1	0	1	off	off	off	off	---	D	$-8V_{dc}$
19	1	0	1	0	0	0	0	1	0	1	off	off	off	off	D	D	$-9V_{dc}$



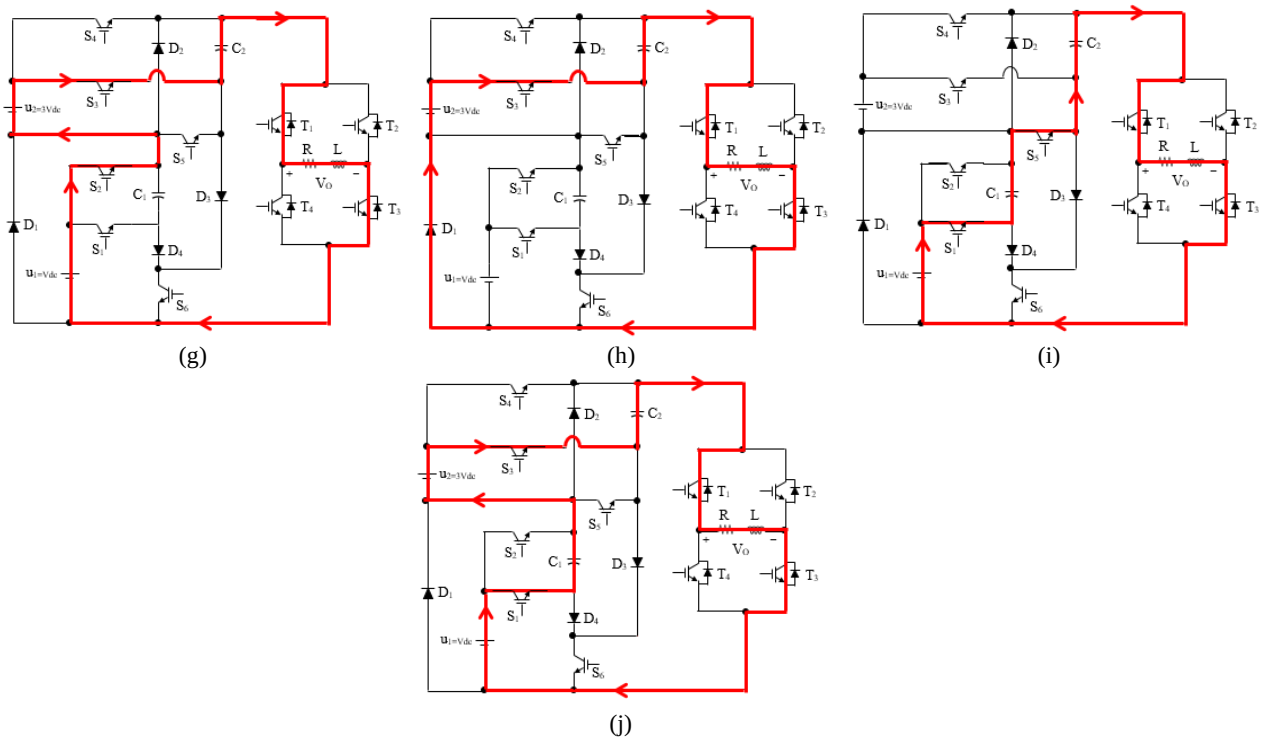


Figure 2. Schematic of switching states for generating different positive and zero levels on the load. (see Table 1): (a) state 1 for $V_O = 0V_{dc}$, (b) state 2 for $V_O = +V_{dc}$, (c) state 3 for $V_O = +2V_{dc}$, (d) state 4 for $V_O = +3V_{dc}$, (e) state 5 for $V_O = +4V_{dc}$, (f) state 6 for $V_O = +5V_{dc}$, (g) state 7 for $V_O = +6V_{dc}$, (h) state 8 for $V_O = +7V_{dc}$, (i) state 9 for $V_O = +8V_{dc}$, (j) state 10 for $V_O = +9V_{dc}$

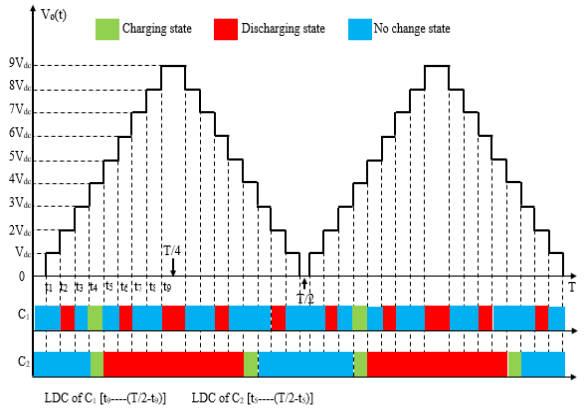


Figure 3. The Charge and Discharge Sequence of Capacitors

$$\Delta Q_{C_1} = \int_{t_9}^{T/2-t_9} i_L(t)dt \quad (1)$$

$$\Delta Q_{C_2} = \int_{t_5}^{T/2-t_5} i_L(t)dt \quad (2)$$

Using Equtions (1) and (2), sizes of C_1 and C_2 can be calculated by:

$$C_1 = \frac{1}{\Delta V_{C_1}} \int_{t_9}^{T/2-t_9} i_L(t)dt \quad (3)$$

$$C_2 = \frac{1}{\Delta V_{C_2}} \int_{t_5}^{T/2-t_5} i_L(t)dt \quad (4)$$

Considering the value of u_1= 20v and u_2=60v (to obtain the maximum output voltage V_{out} = 180V), the C_1 and C_2 voltages will be raised up to 20v and 60v, respectively. Therefore, the voltage differences ΔV_{C1} and ΔV_{C2}, usually considered as 10% of the corresponding capacitor voltage, will be equal to 2V and 8V, respectively. The time instances t_1-t_9 can also be found as:

$$v(t) = v_m \sin(\omega t) \quad (5)$$

$$t_i = \frac{1}{\omega}\sin^{-1}\left(\frac{2i-1}{N-1}\right) \quad ,i = 1,2,3,...,9 \quad (6)$$

in which, N is the dimension of the output levels. Using Equation (6), then t_is, i = 1, .. ,9 are calculated as 0.17 ms, 0.53 ms, 0.89 ms, 1.3 ms, 1.7 ms, 2.1 ms, 2.6 ms, 3.1 ms, and 3.9 ms, respectively. For a load of strict resistance, the current would be:

$$i_L(t) = i_m \sin(\omega t) \tag{7}$$

For a maximum load current im = 2A, the solution of Equation (3) gives the optimal size of C1,

$$C_1 = \frac{2 \times i_m \cos(\omega t_9)}{2\pi f \times \Delta V_{C_1}} \tag{8}$$

Similarly, the precise size of C_2 can be obtained from Equation (4) as:

$$C_2 = \frac{2 \times i_m \cos(\omega t_5)}{2\pi f \times \Delta V_{C_2}} \tag{9}$$

Combining Equations (8) and (9), the ultimate sizes of C_1 and C_2 would be 2156 µF and 1369 µF, respectively. For these capacitors, the closest existing size in the lab is 4700 µF. For this reason, in the experimental setup, they are both chosen equal to $C_1 = C_2 = 4700\mu F$.

3. 2. Power Losses Analysis There are three types of power losses in the proposed SCMLI topology. These are switching loss, conduction loss, and ripple losses of capacitors.

3. 2. 1. Switching Losses The switching losses are caused by delays during the turning on/off of switches and the reverse recovery time of the diodes. As shown in Figure 4, when the pulse reaches the gate terminal of the switch at α_1, it takes a t_{on} for the collector-emitter voltage and collector current to reach their final values. Moreover, when the pulse is removed from the gate terminal at α_3, the switching-off process will take t_{off} seconds. These delays are the source of the switching losses.

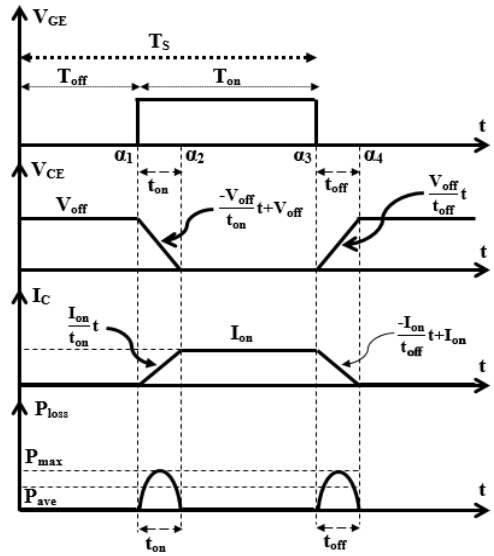


Figure 4. Instantaneous changes of voltage, current, and power on the switches

The switching losses during the ON ($P_{sw,on}$) and OFF ($P_{sw,off}$) states of a typical switch can be calculated by inferred from Equations (10) and (11), respectively, as:

$$P_{sw,on} = \frac{f_s.V_{off}.I_{on}.t_{on}}{6} \tag{10}$$

$$P_{sw,off} = \frac{f_s.V_{off}.I_{on}.t_{off}}{6} \tag{11}$$

where f_s is the frequency of switching, V_{off} , the switch's nominal voltage, and I_{on}, the average load current. Additionally, the switching losses on the diodes will be:

$$P_{sw,D} = \frac{f_s.V_{RM}.I_{RM}.t_B}{6} \tag{12}$$

where V_{RM} and I_{RM} are, respectively, the maximum voltage and current of reverse recovery and t_B, the time delay of the reverse current. The total switching losses can be calculated by:

$$P_{sw,total} = \sum_{i=1}^{N_{sw}} \left(\sum_{j=1}^{N_{on}} \left(P_{sw,on,ij} \right) + \sum_{j=1}^{N_{off}} P_{sw,off,ij} \right) + \sum_{k=1}^{N_D} \left(\sum_{h=1}^{N_{off}} \left(P_{sw,D,kh} \right) \right) \tag{13}$$

where N_{sw} and N_D denote the numbers of switches and diodes, respectively; N_{on} and N_{off} are also the number of ON and OFF states of the switches and diodes during a fundamental cycle (1/Ts).

3. 3. 2. Conduction Losses Conduction losses are due to the resistances and voltage drops across the switches and diodes during turning-ON states. In multilevel inverters, each voltage level contributes to the conduction losses since there is a different current path for each voltage level. The conduction losses of a switch ($P_{cond,sw}$) and a diode ($P_{cond,D}$) can be written as:

$$P_{cond,sw} = V_{on,sw}.I_{sw,ave} + R_{on,sw}.I_{sw,rms}^{\ 2} \tag{14}$$

$$P_{cond,D} = V_{on,D}.I_{D,ave} + R_{on,D}.I_{D,rms}^{\ 2} \tag{15}$$

in which, R_{on} and V_{on} denote, respectively, the resistance of the switch and diode and their voltages during the turning-ON state; I_{rms} and I_{ave}, are also the RMS and average currents of semiconductors, respectively. According to Figure 2, for voltage levels of 0 to $\pm 9V_{dc}$, the conduction losses will be:

$$
\begin{aligned}
&P_{cond,(+9V_{dc})} = (4V_{on,sw}.I_{load,ave} + 4R_{on,sw}.I_{load,rms}{}^{2}) \\
&+(0\times V_{on,D}.I_{load,ave} + 0\times R_{on,D}.I_{load,rms}{}^{2}) \\
&P_{cond,(+8V_{dc})} = (4V_{on,sw}.I_{load,ave} + 4R_{on,sw}.I_{load,rms}{}^{2}) \\
&+(0\times V_{on,D}.I_{load,ave} + 0\times R_{on,D}.I_{load,rms}{}^{2}) \\
&\vdots \\
&\vdots \\
&P_{cond,(-8V_{dc})} = (4V_{on,sw}.I_{load,ave} + 4R_{on,sw}.I_{load,rms}{}^{2}) \\
&+(0\times V_{on,D}.I_{load,ave} + 0\times R_{on,D}.I_{load,rms}{}^{2}) \\
&P_{cond,(-9V_{dc})} = (4V_{on,sw}.I_{load,ave} + 4R_{on,sw}.I_{load,rms}{}^{2}) \\
&+(0\times V_{on,D}.I_{load,ave} + 0\times R_{on,D}.I_{load,rms}{}^{2})
\end{aligned}
\tag{16}
$$

For example, for the level $+9V_{dc}$, according to Figure 2(j), there are 4 switches and 0 diode in the current commutation path; thus, a correct relationship of the conduction loss must take care of the individual number of switches and diodes for each possible path. The total conduction loss, then, will be the sum of losses overall voltage levels,

$$
\begin{aligned}
P_{cond,total} &= P_{cond,(+9V_{dc})} + P_{cond,(+8V_{dc})} + \cdots\cdots \\
&+ P_{cond,(-8V_{dc})} + P_{cond,(-9V_{dc})}
\end{aligned}
\tag{17}
$$

3. 3. 3. Ripple Losses of Capacitors When capacitors are in charging mode, the potential difference between the DC sources and capacitors results in ripples of capacitor voltages. This, in turn, creates ripple losses, which can be calculated as follows:

$$
P_{loss,cap} = \frac{f_{ref}}{2}\sum_{i=1}^{N_C} C_i \Delta V_{Ci}{}^{2} \tag{18}
$$

where NC denotes the number of capacitors. Taking all the losses into account, then, the efficiency of the proposed 19-level topology can be calculated as:

$$
\begin{aligned}
\eta &= \left(\frac{P_{out}}{P_{out} + P_{loss}}\right)\times 100 \\
&= \left(\frac{\frac{\left(V_{out(rms)}\right)^2}{R_{load}}}{\frac{\left(V_{out(rms)}\right)^2}{R_{load}} + P_{sw,total} + P_{cond,total} + P_{loss,cap}}\right)\times 100
\end{aligned}
\tag{19}
$$

4. NEAREST LEVEL CONTROL (NLC)

The suggested topology of the inverter is well suited to work at a couple of switching frequencies including the fundamental as well as higher ones. Among the available modulation schemes for the switching operation, PWM has many advantages such as lower power loss with respect to switching and snubber while maintaining the dv/dt rating quite small. As for the fundamental frequency, there are two well-known switching techniques, one is Selective Harmonic Elimination (SHE) [24] and the other is NLC [25-30]. In the SHE technique, increasing the number of output levels creates a large volume of offline computational costs with respect to switching angles and their storage. Therefore, here, the NLC has been adopted as the switching control technique. For the purpose of switching, a sampled and quantized waveform is needed. In NLC, this waveform is obtained through the comparison of two waveforms: the reference sinusoidal and the desired output. In order to provide the desired switching signals for IGBTs switches, the resulting waveform of this comparator must be quantized to the nearest level and subsequently compared with the given switching plan in Table 1. Figure 5 illustrates the operating principle of the NLC method.

5. COMPARATIVE ASSESSMENT

In this section, the suggested inverter topology will be compared with those of the recent studies which have the same number of output levels. The comparison will be accomplished based upon such measures as the number of (semiconductor) power switches (N_{sw}), diodes (N_d), capacitors (N_C), gate drivers (N_{gd}), voltage gain (V_G), total standing voltage (TSV) and cost function (CF).

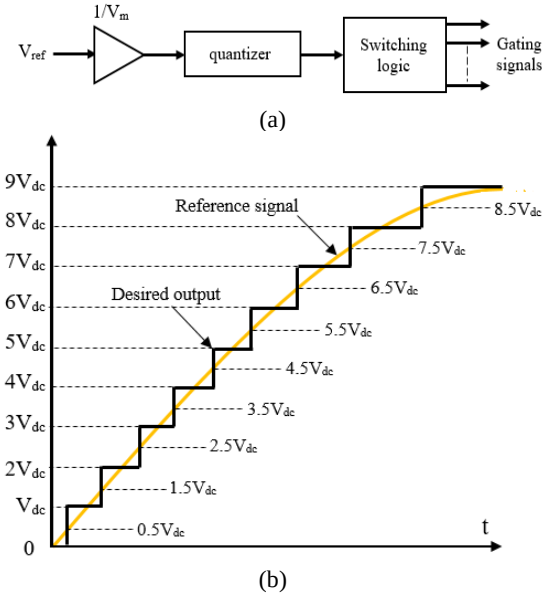


Figure 5. The NLC Switching Method: (a) Schematic Block Diagram (b) Graph-Based Functional Illustration

The total standing voltage is defined as the total peak inverse voltage (PIV) across the semiconductor devices when they are turned off. In the case of TSV per-unit, the total TSV will be divided by the maximum voltage level on the output. Table 2 illustrates the results of this comparison. As it can be seen, the suggested topology is evidently more successful than its other predecessors as to the number of components used per level, especially compared to topologies of the same number of levels.
For the monetary comparison of the given inverter topologies, here, the following cost function (CF) has been considered,

$$CF = \left(N_{sw} + N_{gd} + N_d + N_C + \alpha \times TSV^{pu}\right) \quad (20)$$

$$NCF = \frac{CF}{N_L} \quad (21)$$

According to Table 2, the suggested SCMLI topology gives an acceptable NCF, especially for α = 0.5, which implies the cost-related effectivity of the suggested design when a large number of voltage levels can be produced using very a low number of components.

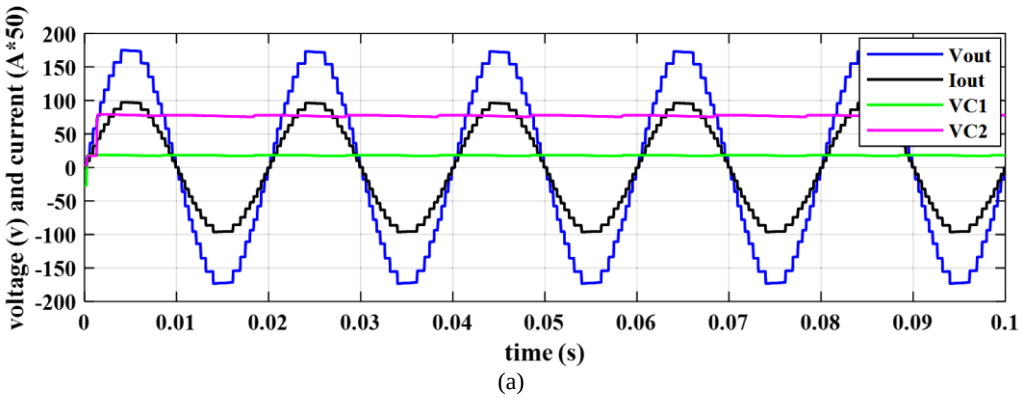
TABLE 2. Comparison of the Suggested MLI with its Latest Counterparts

Top.	N_L	N_{sw}	N_d	N_C	N_{gd}	V_G	TSV^{pu}	NCF
[18]	11	11	0	1	11	1.6	4.4	4.66
[19]	13	14	0	2	11	2	5.33	4.56
[20]	17	10	2	2	10	2	5.5	3.14
[21]	17	10	2	2	10	2	5.5	3.14
[22]	13	11	1	1	10	1.5	6.3	4.18
[23]	13	18	0	2	15	2	5	5.76
[31]	17	18	2	4	14	2	6	4.82
[32]	19	12	6	4	12	2.2	5.8	3.85
[24]	19	12	1	2	10	1.8	6.66	3.02
Pro.	19	10	4	2	10	2.2	6.55	3.08

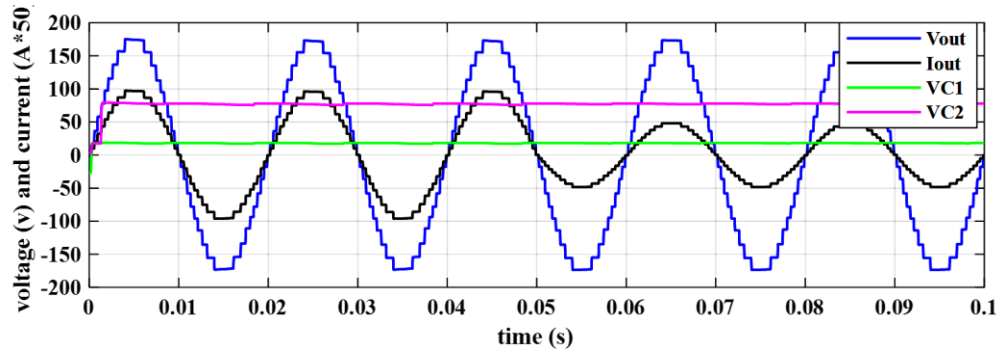
6. RESULTS AND DISCUSSION

6. 1. Simulation Results Simulations are done for the suggested topology and the corresponding results are shown in Figure 6. The simulation parameters are given in Table 3. The voltage waveforms of the output, capacitor C_1 (V_{C1}), capacitor C_2 (V_{C2}) as well as the load current waveform of the suggested design are shown in Figure 6(a) for a load of an exclusive resistance (R = 90 Ω). For the sake of clarity, the vertical axis of the currents are all multiplied by 50. According to Figure 6(a), for a load R=90 Ω, the peak of the current reaches 2A (180v/90Ω). Figure 6(b) illustrates the output waveforms for a variable load between Z=90 Ω at 0 < t < 0.05s and Z=180 Ω at 0.05 < t < 0.1s. For this load, the peak current is equal to 1A. In Figure 6(c), the load has changed from a pure resistance into a mixed impedance, respectively equal to Z=90 Ω at 0 < t < 0.05s and Z=90 Ω + 100 mH at 0.05 < t < 0.1s. As can be seen, here, the output current is nearly sinusoidal due to the filtering nature of the inductor. For all the cases, the output voltage has maintained its steady state while voltages of the capacitors C1 and C2 are in balance with acceptable ripple. According to Table 3, the mean value of capacitors C1 and C2 voltages are approximately equal to 20v and 60v, respectively. Figure 7, also, illustrates the harmonic spectrum analysis of the suggested scheme. As this figure shows, the voltage THD at the inverter output is 4.39%, which is less than 8% complying with the IEEE-519 standards.

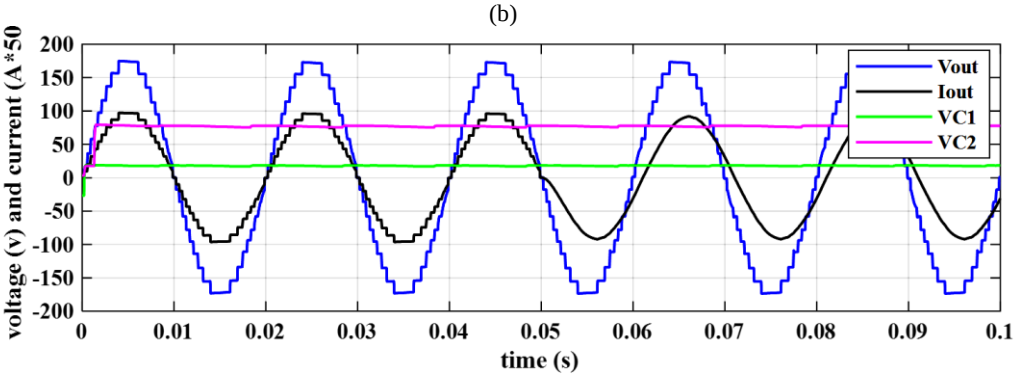
6. 2. Results of Experimental Setup In order to back up the theoretical results as well as those of simulations for the proposed 19-level inverter, as shown in Figure 8, an experimental setup corresponding to a single-phase, low-power version of the inverter, was provided. Using a TMS320F28379D DSP, the NLC switching control method was digitally programmed with code composer studio 8.1.0. For the IGBTs switches and SCHOTTKY diodes, IRG4IBC30S and MBRF20100C are used, respectively. In order to isolate the power circuit



(a)



(b)



(c)

Figure 6. Simulation results with various loads. (a) Z=90 Ω. (b) Z=90Ω at 0<t<0.05s and Z=180 Ω at 0.05<t<0.1s. (c) Z=90 Ω at 0<t<0.05s and Z=90Ω + 100mH at 0.05<t<0.1s. In all figures, for more clear observation, the current wave has been multiplied by 50

TABLE 3. Components of the 19-Level inverter in the experimental setup

First input DC-source	**u_1= 20 v**
Second input DC-source	u_2= 60 v
Peak output voltage	180 v
Processor	DSP TMS320F28379D
Capacitors	C_1=C_2= 4700 µF
IGBT	IRG4IBC30S
Diode	MBRF20100CT
Driver/optocoupler	HCPL-3120
Current sensor	Resistive divider (1/7 Ω, 40 w)
Voltage sensor	Resistive divider (15×100 kΩ)
Sample time	10 µs
Output frequency	50 Hz
Resistive load	R= 180 Ω, 90 Ω
Resistive-Inductive load	R= 180 Ω, L= 22 mH

from the rest, the HCPL3120 driver was used, which aside from isolation, provides the necessary amplifications, too. The resulting setup was tested against several loads, both resistive and inductive using the following components: R=90 Ω, R=180Ω, and L=22mH.

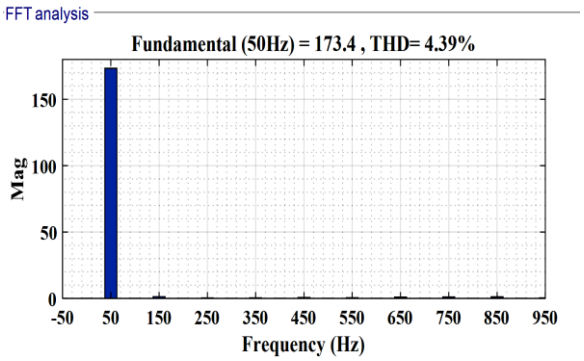


Figure 7. Harmonic Spectrum of Output Voltage of the Proposed 19-level Topology for a Pure Resistive Load (Z=90 Ω)

For the practical implementation, the following must be taken into account,

a) To avoid electrical interference, all gate driver power supplies should be isolated from each other.
b) A high-power resistor should be placed parallel with each capacitor for discharging and safety upon the completion of the test.
c) It is better off to use a PNP- type IGBT for switch S3 (see Figure 1) since S3 and S5 have a common emitter. The parameters related to the laboratory implementation are listed in Table 3.

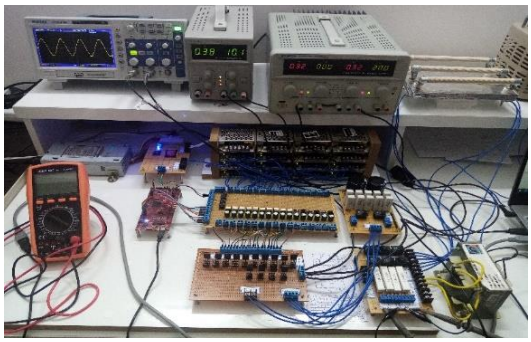


Figure 8. Experimental Set-up in the laboratory

Figure 9 depicts the output voltage of the 19-level inverter (150V). According to the smallest selected voltage level, i.e., 20V, the maximum voltage level must be 180V, however, due to the voltage drop across the switches and diodes, it was reduced to 150V. Figure 10 displays the voltage and current of the inverter's output for a load combined of an exclusive resistance equal to 180Ω. For this load, the current peak is equal to 0.8 A. In Figure 11, the scenario of Figure 10 has been repeated except that, here, the load changes from 180Ω to 90Ω. As shown in this figure, the current amplitude has changed from 0.8A to 1.6A. Figure 12 displays the load's voltage and current when its value changes from 180 Ω to 180 Ω+22mH. According to Figure 12, the current approximately mimics a sinusoidal with a peak of 0.8 A. Figure 13 depicts the capacitors' voltages. In order to measure the capacitors' voltages, a voltage divider with a factor of 1/3 has been considered. From Figure 13, capacitors C_1 and C_2 are charged up to about 15.6V and 65V, respectively. Given the values of the DC sources as u_1=20v and u_2=60v, the capacitors C_1 and C_2 were expected to be charged up to 20V and 80V, respectively. The difference between the two, again, is due to the voltage drop across the switches and diodes. In the laboratory results, according to Figure 13 below, the

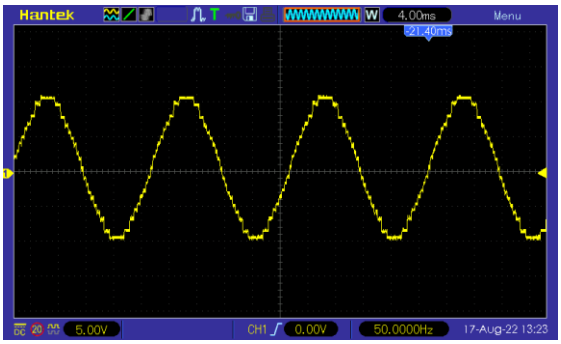


Figure 9. Output Voltage of the 19-Level Inverter (To obtain the actual values, the vertical axis must be multiplied by 15 factor)

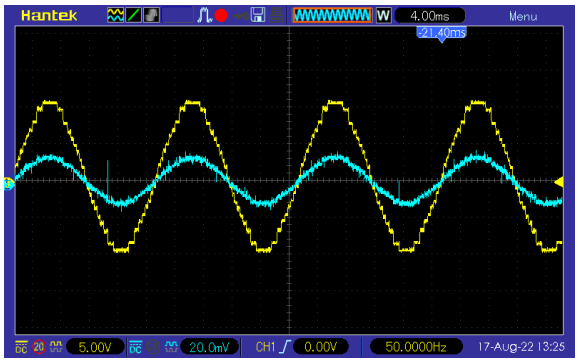


Figure 10. Output Voltage (yellow wave) and Current (blue wave) of the 19-Level Inverter for a Constant Pure Resistive Load of 180Ω. For actual values of voltage and current, the vertical axes must be multiplied by 15 and 7, respectively (see Table 3). The Corresponding oscilloscope probes for voltage and current are set on the ×1 and ×10, respectively

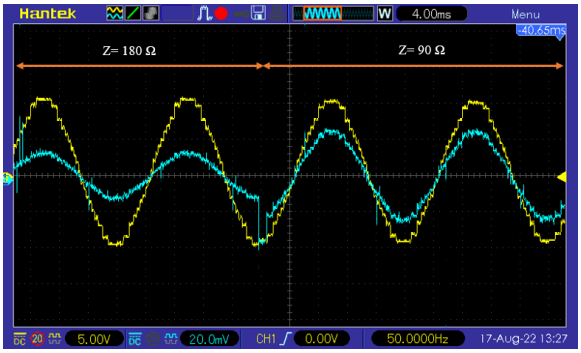


Figure 11. Voltage (yellow wave) and current (blue wave) of the 19-level inverter's output when its load changes from R=180 Ω to R=90 Ω. For the actual voltage and current, the vertical axes must be multiplied by 15 and 7, respectively (see Table 3). (The oscilloscope probes for voltage and current are set to ×1 and ×10, respectively)

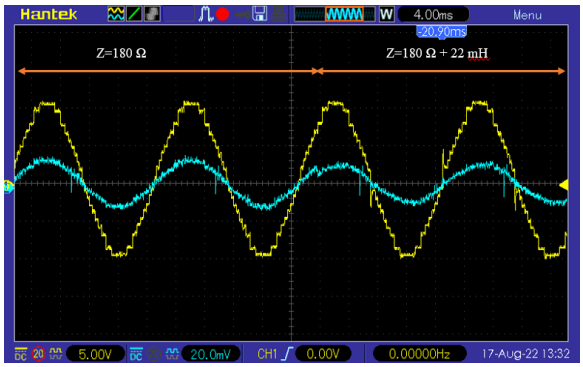


Figure 12. Output voltage (yellow wave) and current (blue wave) of the 19-level inverter when its load changes from Z=300 Ω to Z=300 Ω + 22mH. For actual voltage and current, the vertical axes must be multiplied by 15 and 7, respectively. (Probes of the oscilloscope for voltage and current are set to ×1 and ×10, respectively)

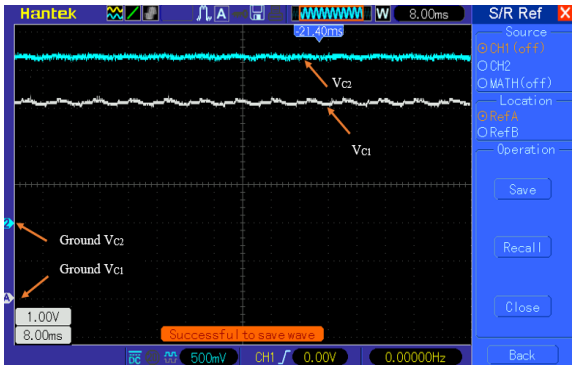


Figure 13. (a) Voltages of Capacitors C1 and C2. (For the actual values of the capacitors' voltage, the vertical axis must be multiplied by 8 for the V_{c2}. The probes of the oscilloscope for capacitors voltage C1 and C2 are set to ×1 and ×10, respectively)

voltage ripple of the first capacitor is equal to $\Delta V_{C1}=0.1\times0.5\times8=0.4V$, where 0.1 is the ripple voltage on the oscilloscope page, 0.5 is the channel2 scale and 0.8 is the resistor divider in the hardware experimental. Moreover, the voltage ripple of the second capacitor is equal to $\Delta V_{C2}=0.2\times1\times10=2V$, where 0.2 is the ripple voltage on the oscilloscope page, 1 is the channel1 scale and 10 is the probe factor of channel1. The capacitor voltage of C_1 and C_2 have been obtained as 15.6 and 65v, respectively. It means that the percent of ripple voltage on the capacitors C_1 and C_2 is 2.5% and 3%, respectively. So, we expect that a 19-level voltage is produced on the output with very low distortion harmonics.

7. CONCLUSIONS

This paper suggested a novel topology for a 19-level inverter, consisting of 10 switches, two DC sources, four diodes, and two capacitors. Besides the low number of components in the inverter circuit, it was designed in a way so that its capacitors are naturally in balance with respect to the voltage without further need for auxiliary circuits. Detailed simulation backed up by an experimental set-up against numerous constant as well as variable resistive and mixed resistive-inductive loads verified the performance of the suggested design. The TSV and NCF of the suggested inverter were, respectively, 6.55 and 3.08, which is comparable to its recent counterparts. The voltage gain was 2.25 with an output THD equal to 4.39%, from which, the latter is within the acceptable limit of IEEE-519 standard. As a suggestion for future research, the proposed inverter can be upgraded to a bi-directional inverter to eliminate the H-bridge. We can also mention the research to find new applications, especially in low voltage photovoltaic systems connected to the grid.

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Persian Abstract

چکیده

در این مقاله ، یک اینورتر چند سطحی جدید افزاینده نوع خازن سوئیچ شده که قادر به تولید ۱۹ سطح ولتاژ با استفاده از تنها ۱۰ سوئیچ ، ٤ دیود ، ۲ خازن و ۲ منبع DC است ارائه شده است. ویژگی های اصلی توپولوژی پیشنهادی عبارتند از: ۱) استفاده از تعداد بسیار کمی ازعناصر نیمه هادی ، ۲) ولتاژ ایستایی (تحمل) بسیار پایین برابر با ٦.٥٥ و ۳) خاصیت خود متعادلی ولتاژهای خازن‌ها. به منظور ارائه سیگنال‌های سوئیچینگ مورد نظر به سوئیچ ها ، روش کنترل نزدیکترین سطح بکارگرفته شده است. برای ارزیابی مزایای توپولوژی طراحی شده اینورتر ۱۹ سطحی جدید، از دیدگاه تعداد سوئیچ ها ، تعداد منابع DC ، تعداد خازن ها و همچنین ولتاژ ایستایی ، یک مقایسه در مقابل آخرین توپولوژی های ارائه شده انجام شده است. همچنین ، به منظور ارزیابی عملکرد اینورتر پیشنهاد شده و اعتبار سنجی آن ، چندین آزمایش در بارهای مختلف با استفاده از پردازشگر TMS320F28379D DSP مورد آزمایش قرار گرفته است. نتایج شبیه سازی و آزمایشگاهی همگی حاکی از برتری توپولوژی پیشنهادی در برابر ساختارهای قبلی خود است.