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Ultra Low Power Temperature Compensated Complementary Metal Oxide Semiconductor Ring Oscillator in Subthreshold

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ABSTRACT

Low power consumption, low chip area and fabrication in the standard complementary metal oxide semiconductor (CMOS) process are vital requirements for oscillators used in low-cost bio-implantable and wearable devices. Conventional ring oscillators (ROs) are good candidates for using in biomedical applications. However, their oscillation frequency strongly depends on the temperature. In this study, a temperature compensated ring oscillator with low power consumption is proposed. The transistors of the proposed ring oscillator operate in the subthreshold region to achieve a low power and low voltage performance. Since, in the subthreshold region, the oscillation frequency of a conventional ring oscillator increases with increase in the temperature, two current sources are used to power the proposed subthreshold ring oscillator: a temperature independent current source and a complementary to absolute temperature (CTAT) current source. In the proposed circuit, the CTAT current forms a small part of the total supplied current and its duty is to compensate for the oscillation frequency deviation. Two prototypes of the subthreshold ring oscillator were designed and simulated for a target frequency of 1MHz using commercially available 0.18µm RF-CMOS technology. The thermal coefficient (TC) of the uncompensated ring oscillator was 2400 ppm/ºC from -40ºC to 85ºC, though applying the proposed technique reduces the TC of the ring oscillator to 80.4 ppm/ºC with total power consumption as low as 14.5µW.

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1. INTRODUCTION

Synthesizing a stabilized clock signal is essential for different analog and digital systems such as RFID and wireless sensor networks (WSNs). The most usual clock references are based on quartz crystal oscillators [1]. Despite excellent stability of crystal oscillators against temperature and process variation, crystal resonators cannot be integrated on a chip by using standard CMOS process; that increases the area and cost of the system. Hence, CMOS oscillators are appropriate candidates for producing clock in various low power and low cost applications such as implantable and wearable biomedical devices, cubic millimetre WSN applications [2] and FRID tags [3]. Different types of CMOS oscillators include LC oscillators, RC relaxation, and ring oscillators (ROs). The oscillation frequency in CMOS oscillators suffers from poor thermal stability. The thermal instability of the oscillation frequency in CMOS oscillators is due to the dependency of different parameters, such as electron/hole mobility (µ) and threshold voltage (V_{TH}) to the temperature and process variations. So, in order to achieve desirable frequency stability, using compensation techniques [4, 5] is mandatory. Thus, several researches have been devoted to effective compensation of the CMOS oscillators [4, 6-13]. Considering the type of application that oscillator is designed for, the appropriate compensation technique is developed. For example, as reported by Katebi et al. [10] the main challenges in the military fields are the precision of the oscillation frequency as well as its thermal stability. To combat these challenges a hybrid cross-

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coupled Colpitts VCO is presented by Katebi et al. [10], in which the varactors are driven by CTAT voltages. Although the temperature coefficient (TC) of the VCO and its phase noise are acceptable, its high-power consumption and chip area (due to use of inductors) are not appropriate for biomedical devices. An LC VCO used in an RFID system is also thermally compensated with using an auxiliary varactor loop in a PLL configuration [11]. The proposed method provides adequate frequency stability, but occupies more area because of using several inductors.

Using a frequency to voltage (FV) converter in a feedback loop the TC of a current-reused stacked ring oscillator has been improved by Rodrigues et al. [12]; however, the circuit suffers from the high complexity and nonlinearity of the FV. In order to reduce the TC nonlinearity of an RC oscillator in a wired-communication system a frequency locked loop (FLL) is used by Park et al. [13] that locks the period of the oscillator to a reference time constant. The accuracy of the output frequency of this oscillator over temperature variation is largely depends on the behaviour of the reference resistor used in this configuration; however, this technique provides a low power RC oscillator with moderate TC.

In biomedical and RFID applications, some problems such as low power consumption, low chip area and cost, are the main design considerations [14, 15]. Among different types of the CMOS oscillators, the ring oscillators has the capability of high integration that makes them as an area efficient option for clock generation. However, the main drawback of the ring oscillators is the dependency of their oscillation frequency on the temperature and process variations.

Oscillation frequency in the relaxation oscillators is determined by the RC time constant. The most important result of this dependency is that the frequency of oscillation is affected by the high thermal coefficient of a typical resistance. A technique to compensate the frequency fluctuations in a relaxation oscillator is combination of two polysilicon resistors with positive and negative thermal coefficients in parallel and series. Ueno et al. [6], used two polysilicon resistors with positive and negative thermal coefficients, the frequency temperature coefficient of a relaxation oscillator is reduced to 90 ppm/ºC in a temperature range of -20ºC to 100ºC. This method provides a suitable temperature coefficient and reduces the phase noise by filtering the noise. However, the capacitors and resistors used in this design increase the die area significantly, and the circuit suffers from leakage current of the capacitors in high frequencies. A current mode relaxation oscillator is presented by Chiang and Liu [16] in which a proportional to absolute temperature (PTAT) and a CTAT current source are combined to supply the oscillator with a temperature independent current reference. The main privilege of the proposed technique is the frequency variations as low as 64 ppm/ºC with low power consumption and low chip area. Operation of the transistors in subthreshold can supply a reliable margin for power consumption in long life applications. However, the main drawback of this design is the need for special features like trimming for implementation of precise resistors.

Another technique that improves the stability of the oscillation frequency in a ring oscillator has been proposed by Wang et al. [17]. In this method, the Brokaw's voltage reference with transistors operating in the subthreshold region generate a PTAT voltage source. Since the temperature coefficient of the gate-source voltage of transistors in the ring oscillator is negative [18] (i.e. CTAT), using the PTAT voltage reference provides a temperature independent bias current for the ring oscillator. The main advantages of the method presented by Wang et al. [17] are low jitter and wide temperature operation range with small temperature drift. The main drawback of the circuit introduced by Wang et al. [17] is its high-power consumption and the need for high supply voltage.

Due to the diversity of the thermal compensation techniques, only a conceptual diagram is shown in Figure 1 to demonstrate the idea behind of all thermally compensated ROs.

Chang and Liu. [8] proposed a method to compensate thermal dependency of a bandgap reference (BGR) which is used for analog feature extraction of ECG signals in the sub-blocks of an RFID tag. The PTAT and CTAT voltage generators of the proposed BGR use a cascode structure to reduce frequency dependency on the supply voltage and temperature. However, due to the stack of transistors, this technique is not suitable for low voltage designs.

As reported by Tang and Tang [9], providing a stable bias voltage for a ring VCO can mitigate the frequency instability caused by the process and temperature variations. Tang and Tang [9] stated that the bias voltage which was produced by an external off-chip LDO (Figure 2) along with a compensation circuit; that has provided a reference voltage for the ring oscillator. Using off-chip

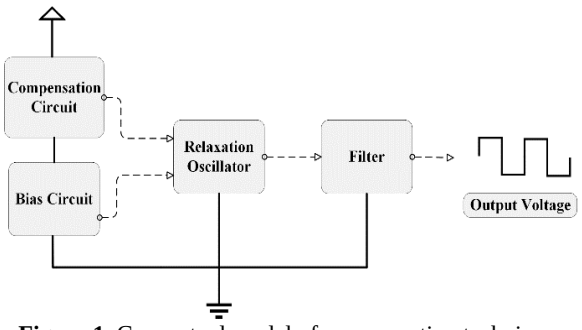


Figure 1. Conceptual model of compensation technique

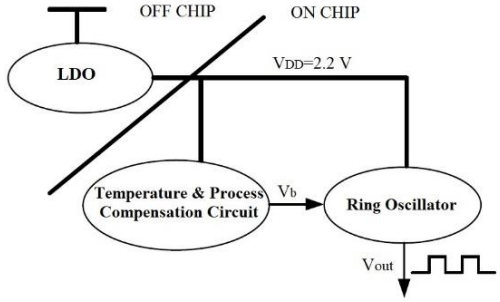


Figure 2. Use of off-chip LDO and compensation circuit in [9]

components can be an obstacle for building an area-efficient biomedical system. Besides, using an LDO increase the power consumption and results in higher total power dissipation and lower battery life in the mobile applications. It is worth mentioning that the frequency variation of the circuit reported by Tang and Tang [9] is 2% while the power consumption is as high as 200µW.

A modified RC network has been proposed by Huang. and Wentzloff [19] for frequency compensation of a relaxation oscillator. The RC network adds an additional zero to the transfer function of the oscillator that enables temperature compensation of the step response of the oscillator. Due to the temperature dependency of the oscillator time constant (i.e. RC), two different polysilicon and diffusion resistors are used for temperature compensation. In fact, the use of two resistors with negative and positive TC neutralizes the effect of temperature variation on the oscillation frequency. Although very low power consumption and small chip area are achieved by the aforesaid method, its temperature coefficient is not very low.

While different compensated oscillators are introduced in prior works, our work aims to present a new compensation technique for a low power and area efficient ring oscillator operating in the subthreshold region. The rest of the paper organized as follows. The proposed compensation techniques and behaviour of the ring oscillator in the subthreshold region are described in section 2. In section 3, the simulation results are presented, and finally, the conclusion is defined in section 4.

2. PROPOSED TECHNIQUE AND CIRCUIT

2. 1. Thermal Behavior of a MOSFET in Subthreshold In the low power circuits, MOS devices usually are biased in weak inversion (subthreshold). A MOS transistor can operate in weak inversion with very low supply voltage and low power consumption. The drain current I_D of a transistor in subthreshold is an exponential function of the gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) given by Equation (1) [20]:

$$I_D=kI_0\exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)\times\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (1)$$

in which $I_0=\mu_0 C_{ox}(\eta-1)V_T^2$, k is the aspect ratio of the transistor, µ is the carrier mobility, C_{ox} is the gate oxide capacitance, V_T is the thermal voltage, V_{TH} is the threshold voltage of the MOSFET and η is the subthreshold slope factor. For $V_{DS}>0.1V$ the current I_D is almost independent of V_{DS} and is given by Equation (2) [21]:

$$I_D=k\mu_0 C_{ox}(\eta-1)V_T\exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \quad (2)$$

The carrier mobility, thermal and threshold voltages in Equation (2) are the parameters that depend on the temperature. Therefore, Equation (2) shows that the drain current of a MOS device in subthreshold region extremely depends on the temperature. As discussed by Tajalli and Leblebici [22], the subthreshold current I_D is proportional to the temperature, and an increase in temperature results in an increase in drain current [23].

2. 2. CMOS Ring Oscillator in Subthreshold A conventional ring oscillator is comprised of an odd number of inverters in a loop. Figure 3 demonstrates a typical ring oscillator with five stages.

Each stage includes a CMOS inverter operating as a delay element and is shown in Figure 4. While ring oscillators occupy very small chip area, their high power consumption and temperature dependency of oscillation frequency are the main issues addressed by prior works [17].

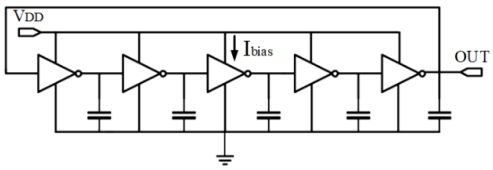


Figure 3. Structure of a five-stage conventional ring oscillator

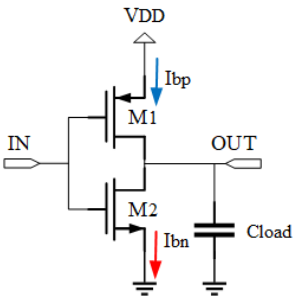


Figure 4. Single-stage inverter

In a single stage inverter, the low to high (T_{PLH}) and high to low (T_{PHL}) propagation delays are controlled by the bias currents of transistors and are given as below:

$$\begin{cases} T_{PHL}=C_{eff}(V_{DD}-V_{trp})/I_{bn} \\ T_{PLH}=C_{eff}V_{trp}/I_{bp} \end{cases} \quad (3)$$

in which I_{bp} is the source current through PMOS transistor, I_{bn} is the sink current through NMOS transistor, C_{eff} is the effective load capacitance of each inverter, and V_{trp} is the inverter trip voltage. The oscillation frequency of a ring oscillator with N stage is given by Equation (4).

$$f_{osc}=1/(N(T_{PHL}+T_{PLH})) \quad (4)$$

So the number of inverters (N) and their propagation delays (T_{PHL} and T_{PLH}) define the oscillation frequency of a ring oscillator [24]. According to Equations (3) and (4), the oscillation frequency of a ring oscillator is a function of the bias current, the supply voltage, and V_{trp}. Since the threshold voltage and carrier mobility of a transistor are modulated by the temperature, the bias current and V_{trp} are also varied by the temperature. In the design of an inverter the source (I_{bp}) and sink (I_{bn}) currents are typically chosen identical by proper sizing of the inverters' PMOS and NMOS transistors. Thus, supposing $I_{bn}=I_{bp}=I_{bias}$ and replacing T_{PHL} and T_{PLH} from Equation (3) to Equation (4), the oscillation frequency can be written as Equation (5). Apparently, Equation (5) indicates that the oscillation frequency of the RO is linearly controlled by the NMOS and PMOS drain currents.

$$f_{osc}=I_{bias}/(N(C_{eff}V_{DD})) \quad (5)$$

The transistors of an inverter in a ring oscillator can be designed to operate in subthreshold (weak inversion) or above threshold (strong inversion). In the strong inversion region, the current of each inverter decreases with an increase in the temperature, that results in reduction of the oscillation frequency [25]. On the other hand, due to the diffusion nature of the subthreshold current in MOS transistors, an increase in temperature results in increase in the transistor current and, according to Equation (5), leads to an increase in the oscillation frequency in subthreshold region [18, 20]. Thus, the temperature behaviour of an RO in subthreshold region is the opposite of that of in the above threshold.

In this study, a conventional 5-stage ring oscillator with 1 MHz oscillation frequency is designed in the subthreshold region with 1.44 µW power consumption (without bias circuitry). The variation of the oscillation frequency of the oscillator with temperature is simulated and depicted in Figure 5. As shown in this figure, the uncompensated oscillator has 2400 ppm/ºC frequency variation (about 30% frequency deviation) in the temperature range of -40 ºC to 85 ºC. In order to use such a low-power subthreshold ring oscillator as a reference frequency in an area efficient application such as RFIDs and biomedical devices, using some compensation techniques are mandatory. Therefore, a new compensation technique for the ring oscillators that operate in weak inversion is presented as follows.

2. 3. Concept of the Proposed Compensation Technique As discussed above and illustrated in Figure 5, the oscillation frequency of a subthreshold RO is almost proportional to the absolute temperature (PTAT). To alleviate this issue a conceptual model of the proposed compensation technique is illustrated in Figure 6. In this technique, a constant current source as well as a CTAT current source are used to supply the ring oscillator. The constant current source provides the main portion of the required current and the CTAT current source only compensate the PTAT behaviour of the frequency variation. In other word, while the frequency of the subthreshold oscillator increases with the temperature, the CTAT current source reduces supplied current source in such a way that a minimum frequency variation is achieved. The exact value of the CTAT current can be obtained through simulations.

2. 3. 1. CTAT and Constant Current Sources To verify the proposed concept, two prototypes of the low-power thermally compensated ring oscillators with different CTAT current sources were designed and

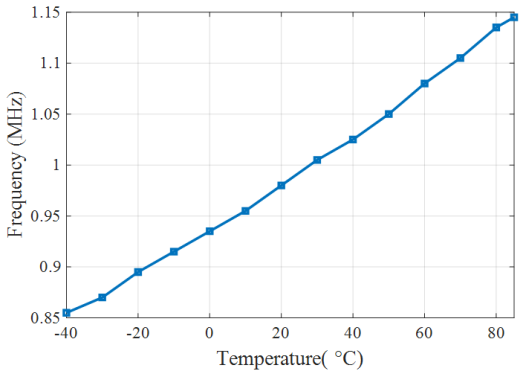


Figure 5. Frequency variation of a typical uncompensated subthreshold RO

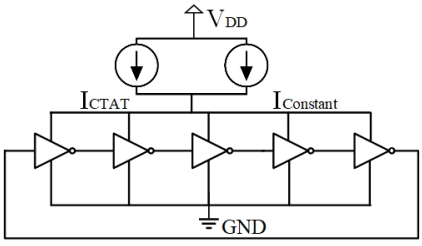


Figure 6. Concept of the proposed compensation technique

simulated in a standard 0.18µm RF CMOS technology. The first CTAT current generator is based on the thermal behaviour of the PN junction potential in a lateral BJT and the other is based on the threshold voltage of a MOS device. The circuits used for CTAT and constant current sources in this work are explained as follows.

2. 3. 1. 1. Generating CTAT current using Base-Emitter voltage of a BJT As we know, the base emitter voltage (V_{BE}) of a bipolar junction transistor (BJT) is inversely proportional to the temperature. The first order approximation of temperature dependency of the base emitter voltage is expressed as Equation (6):

$$V_{BE}(T)=V_{BE}(T)\frac{T}{T_r}+V_{g0}\left(1-\frac{T}{T_r}\right) \quad (6)$$

where the V_{g0} is the bandgap voltage of silicon at 0 *K*, T and T_r are the designed and reference temperatures in Kelvin respectively. Since $\partial V_{BE}/\partial T \approx$-1.5 mV/K at room temperature, V_{BE} is a traditional solution for CTAT current generation [26]. Figure 7 illustrates the suggested structure which employs a diode-connected BJT to generate the required CTAT current [27] in this circuit. The operational amplifier in a negative feedback loop guarantees identical potentials for nodes A and B such that the current of resistor R_1 will be V_{EB1}/R_1. Consequently, the output CTAT current is obtained through the current mirror transistors M_2 and M_3 as stated in Equation (7).

$$I_{CTAT}=\frac{V_{EB1}}{R_1} \quad (7)$$

2. 3. 1. 2. CTAT Current Generator Using Threshold Voltage of a MOSFET The absolute value of the threshold voltage of a MOS devices decreases with an increase in temperature and has an almost linear relation with the temperature in the range of 200 K to 400 K [28]. As a first order approximation, the temperature dependency of the threshold voltage is expressed by Equation (8):

$$V_{TH}(T)=V_{TH}(T_0)+\alpha_{VTH}(T-T_0) \quad (8)$$

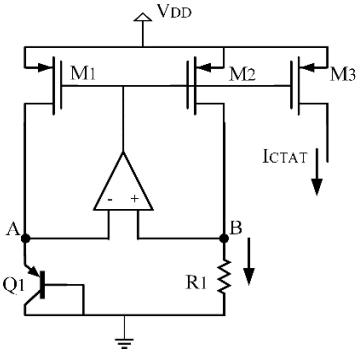


Figure 6. CTAT current generator using V_{EB}

in which $V_{TH}(T_0)$ is the threshold voltage at temperature T_0, and α_{VTH} is a negative temperature coefficient in a standard CMOS technology [25, 26]. Hence, absolute threshold voltage has a negative slope and can be utilized for generating a CTAT current. The circuit that used as a CTAT current source is shown in Figure 8. This circuit extracts V_{TH} and generates a CTAT current that is directly proportional to the threshold voltage of a PMOS transistor [29].

In Figure 8, M_3 and M_4 play the role of threshold voltage extractor. Supposing identical $|V_{THp}|$ for all PMOS transistors, one can write:

$$V_{SD1}=V_{SG1}-V_{SD2} \quad (9)$$

In this circuit, M_3 operates in the saturation region and M_2 operates in the linear region permanently. So V_{SD2} can be expressed as follows:

$$V_{SD2}=\sqrt{2I}\left(\sqrt{\frac{1}{K_3}+\frac{3}{K_2}}-\sqrt{\frac{1}{K_3}}\right) \quad (10)$$

in which $K_i=\mu_p C_{ox}(w/l)_i$. Assuming $K_2=K_3=K_1/3$, the drain source voltage of M_3 is given below:

$$V_{SD1}=|V_{THp}|+\sqrt{\frac{6I}{3K_3}}-\sqrt{\frac{2I}{K_3}+\frac{6I}{K_3}}+\sqrt{\frac{2I}{K_3}}\approx|V_{THp}| \quad (11)$$

The operational amplifier puts the voltageV_{SD1} across a resistor with low TC to provide required I_{CTAT} that is given by Equation (12).

$$I_{CTAT}=\frac{|V_{THp}|}{R} \quad (12)$$

2. 3. 2. Constant current source ($I_{Constant}$) To implement the required constant current in Figure 6 (i.e. $I_{Constant}$), a PTAT and a CTAT current are combined in such a way that a temperature independent current is generated by the circuit in Figure 9 [27]. Supposing identical aspect ratios for $M_{1\text{-}4}$ and emitter area ratio A_{E1}/A_{E2} equals to *n* for Q_1 and Q_2, and writing KVL for

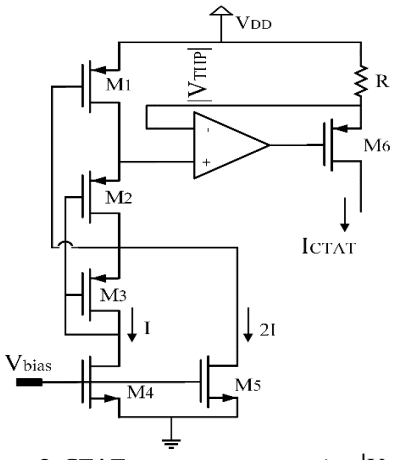


Figure 8. CTAT current generator using $|V_{THp}|$

the loop including Q_1 and Q_2 and R_1, the current I_{PTAT} is obtained as Equation (13).

$$I_{PTAT}=\frac{\Delta V_{BE}}{R_1}=\frac{V_T}{R_1}\ln(n) \quad (13)$$

The CTAT current I_{CTAT} is also given by Equation (14):

$$I_{CTAT}=\frac{V_{BE3}}{R_2} \quad (14)$$

The sum of PTAT and CTAT currents is mirrored in M_4 and I_{ref} is obtained as follows:

$$I_{ref}=I_{PTAT}+I_{CTAT}=\frac{V_T}{R_1}\ln(n)+\frac{V_{BE3}}{R_2} \quad (15)$$

In order to find appropriate R_1 and R_2 for the thermal compensation of I_{ref}, one should solve the derivative of the reference current with respect to the temperature in Equation (16).

$$\frac{\partial I_{ref}}{\partial T}=\frac{k}{qR_1}\ln(n)+\frac{\partial V_{BE3}}{\partial T}\frac{1}{R_2}=0 \quad (16)$$

2. 4. Proposed Compensated RO: Transistor Level

Using CTAT current generators discussed in sections 2.3.1.1 and 2.3.1.2, and the constant current generator in Figure 9, two prototypes of the proposed compensated RO are shown in Figures 10 and 11. According to Figure 10, the CTAT current source in Figure 7 is applied to a conventional ring oscillator to compensate PTAT behaviour of the oscillation frequency of the RO in subthreshold region. In this circuit, the constant current source, which is in parallel to the CTAT current source, provides the major part of the required current for supplying the oscillator.

As shown in Figure 11, the second prototype of the proposed technique is realized by using the CTAT generator depicted in Figure 8. In this circuit, like previous prototype, the constant current generator has also the duty of supplying most of the total power required by RO.

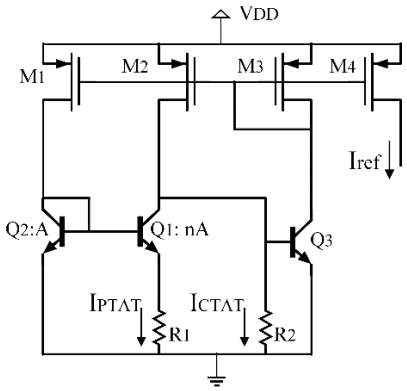


Figure 9. Constant current generator

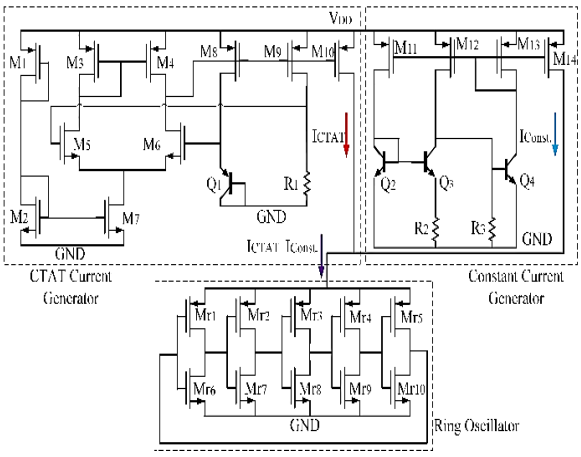


Figure 10. First circuit implementation of the proposed compensation technique

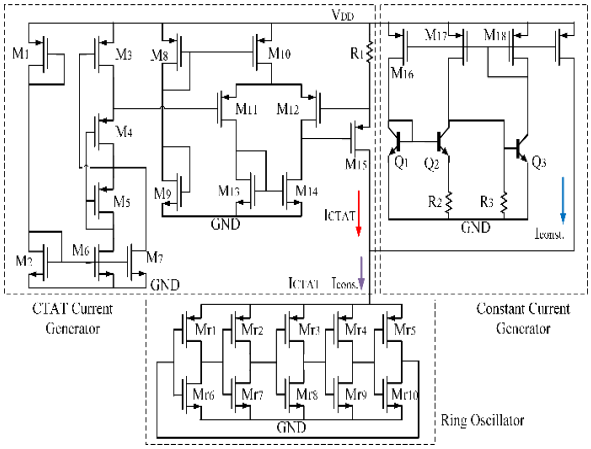


Figure 11. Second circuit implementation of the proposed compensated ring oscillator

3. SIMULATION RESULTS

To verify the performance of the proposed technique, both circuits depicted in Figures 10 and 11 are designed and simulated in an available commercial 0.18µm RF CMOS process. Tables 1 and 2 represent the circuit parameter values of the designed circuits of Figures 10 and 11, respectively. It is worth noting that the aspect ratio of NMOS (Mr1-Mr5) and PMOS (Mr6-Mr10) transistors for the RO core are chosen 23µm/1µm and 69µm/1µm, respectively.

Both circuits are designed for 1MHz oscillation frequency with a 1.8-V power supply and total current consumption of 800 nA. In this case study the constant current source with 700 nA has the major contribution to the total power consumption, though the CTAT current source generates only 100 nA to compensate the frequency deviation. The simulated total supply current, i.e. $I_{CTAT}+I_{Const}$, of the first and second prototypes is

depicted in Figure 12. The slope of the total current in both cases is negative and almost equal to -2.2 nA/ºC.

The output waveforms of the compensated ring oscillators for different temperature values are illustrated in Figure 13. While the amplitude of output waveforms of the ROs varies by temperature, the oscillation frequency is nearly constant for both prototypes.

TABLE 1. Circuit parameter values for the first proposed compensated RO

Device	Size	Device	Size
M_1	0.23/4.3 µm	M_{11}	0.28/8 µm
M_2	0.22/0.75µm	M_{12}	0.28/8 µm
M_3 & M_4	3.6/4 µm	M_{13}	0.28/8 µm
M_5 & M_6	4.4/8 µm	M_{14}	0.22/14 µm
M_7	0.6/0.35 µm	R_1	5.5 MΩ
M_8	0.22/10 µm	R_2	104 kΩ
M_9	0.22/10 µm	R_3	3.2 MΩ
M10	0.22/16 µm		

TABLE 2. Circuit parameter values for the second proposed compensated RO

Device	Size	Device	Size
M_1	0.22/0.44µm	M_{11} & M_{12}	18.9/8 µm
M_2	0.42/0.2 µm	M_{13} & M_{14}	1.54/20 µm
M_3	0.6/0.18 µm	M_{15}	0.32/4 µm
M_4	0.22/0.2 µm	M_{16}	0.28/8 µm
M_5	0.22/0.2 µm	M_{17}	0.28/8 µm
M_6	0.42/0.85µm	M_{18}	0.28/8 µm
M_7	0.23/1.6 µm	M_{19}	0.22/13.8µm
M_8	0.26/18 µm	R_1	6.6 MΩ
M_9	0.26/10 µm	R_2	104 kΩ
M_{10}	1.05/0.18µm	R_3	3.2 MΩ

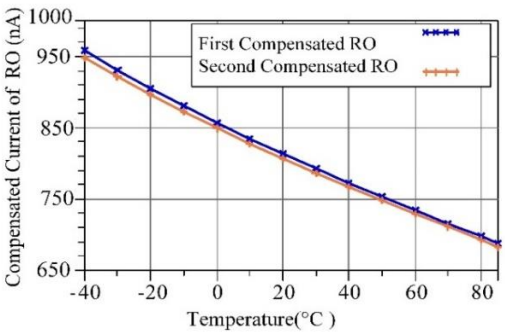


Figure 12. Total supply current $I_{CTAT}+I_{Const}$

For more precise investigation of the frequency variation with temperature, Harmonic Balance (HB) analysis is performed for the proposed compensated and uncompensated ROs and their oscillation frequencies are depicted in Figure 14 for -40 °C to 85 °C temperature range. Simulation results show that the temperature coefficient of the oscillation frequency for the first compensated RO is 80.4 ppm/ºC, while the total power consumption (including bias circuitry) is only 14.5µW. The temperature coefficient of the oscillation frequency for the second prototype is 80.4 ppm/ºC as well and the total power consumption (including bias circuitry) is 34.1µW. It is worth noting that the temperature coefficient of the uncompensated RO in Figure 14 is as high as 2400 ppm/ºC. Hence, the comparison of the temperature coefficients between compensated and uncompensated ROs in Figure 14 explicitly reveals the efficacy of the proposed technique for compensation of the subthreshold ROs.

The sensitivity of the oscillation frequency to the supply fluctuation is also shown in Figure 15. As seen in this figure the proposed circuits have less than 10% frequency variation, though the uncompensated RO has more than 100% frequency variation.

In order to examine the behavior of the compensation method against process variations, the simulated oscillation frequency versus temperature for different process corners is depicted in Figure 16. According to Figure 16, both prototypes of the compensated RO are robust against process variations.

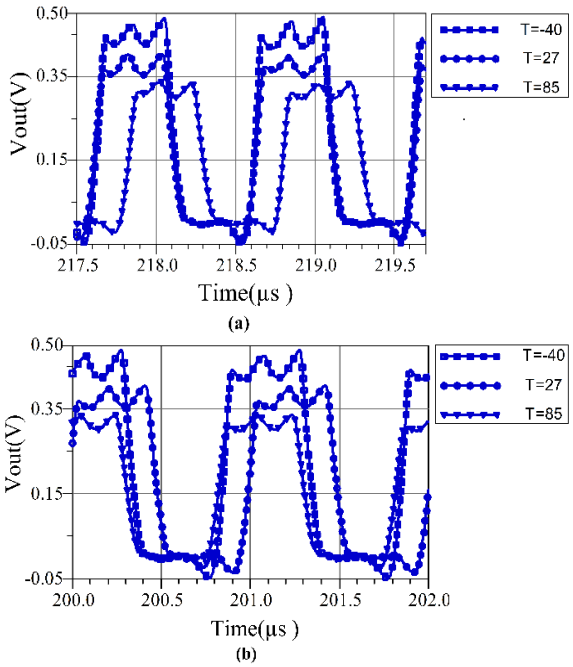


Figure 13. Output waveforms of the (a) first and (b) second compensated ring oscillator at different temperatures

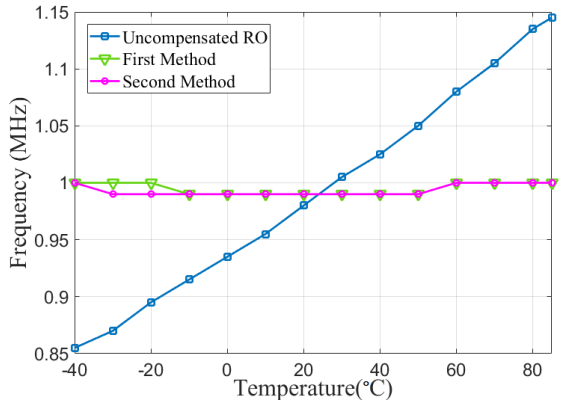


Figure 14. Simulated frequency versus temperature for subthreshold compensated and uncompensated ring oscillators

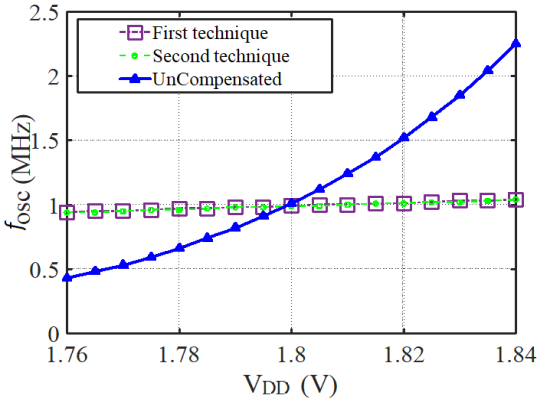


Figure 15. Frequency variation versus supply voltage fluctuation of the oscillators

To estimate the total active area, the layouts of both proposed circuits in Cadence are shown in Figure 17. The total die area of the first and second compensated ROs are 296µmx293µm and 287µmx292µm, respectively.

The performance of the proposed compensated ROs and some previous state of the art works are summarized in Table 3. Since, the different works may be designed at different frequencies with different power consumptions, the following figure of merit (FOM) is used to compare the overall performance of the circuits: The FOM is defined as $(TC\times P_{total})/f_{osc}$ in which P_{Total} is the total power consumption in µW, f_{osc} is the oscillation frequency in MHz and TC is the temperature coefficient of the compensated oscillator in ppm/ºC. Apparently the FOM of the proposed compensated ring oscillator is among the best FOMs in Table 3. That is, using an appropriate compensation technique and operating in subthreshold, an excellent frequency stability has been achieved with a very low power consumption; that results in an excellent FOM in Table 3. The proposed compensated RO provides a low TC clock signal without need for any

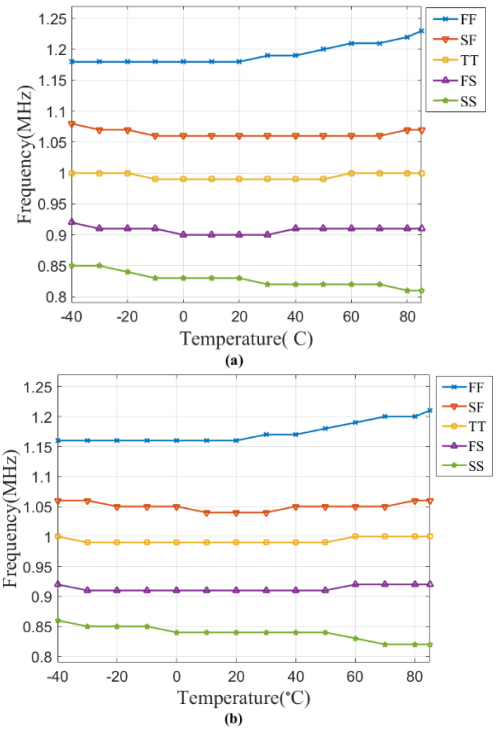
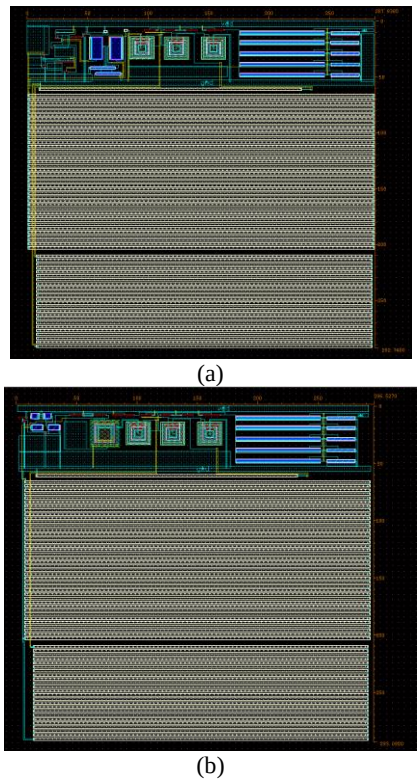


Figure 16. Oscillation frequency at different process corners for (a) first and (b) second compensated circuits. (FF is fast NMOS and fast PMOS, SF is slow NMOS and fast PMOS, FS is fast NMOS and slow PMOS, and SS is slow NMOS and slow PMOS corner)



(a)

(b)

Figure 17. The layout of (a) the first and (b) second compensated ROs

TABLE 3. Performance summary of the proposed and previously reported works

Reference	[8]	[29]	[30]	[7]	[31]	[6]	1st Proposed RO	2nd Proposed RO
Year	2019	2016	2014	2013	2009	2009		
Process (nm)	180	180	130	130	130	350	180	180
V_{DD} (V)	1.2	3	1	2.5	1.5	3	1.8	1.8
f (MHz)	13.4	1.9	1.2	1	3.2	30	1	1
P (µW)	157.8	390	5.8	428	38.4	180	14.5	34.1
$\Delta f/f_c$ %	N/A	1.16	±1.8	N/A	N/A	N/A	1.005	1.005
TC (ppm/˚C)	193.15	92.8	296	108	125	90	80.4	80.4
Temp. (˚C)	[-20–100]	[-40 – 85]	[-40 – 80]	[-20 – 200]	[-20 – 60]	[-20 – 100]	[-40 – 85]	[-40 – 85]
Area (mm^2)	0.12	0.22	0.016	0.007	0.15	0.08	0.087	0.084
FOM	2274	19048	1420	46224	1500	540	1165	2741

precise resistor, capacitor or off-chip component, and needs no special feature like trimming that makes it compatible with cost-efficient standard CMOS technology. It is worth mentioning that the most of the prior researches are devoted to compensation of RC relaxation oscillators or above-threshold ring oscillators, though here the compensation of the subthreshold RO has been targeted.

3. CONCLUSION

A low power thermally compensated CMOS ring oscillator is developed in which the RO core operates in subthreshold region. Since the oscillation frequency of a ring oscillator in subthreshold is proportional to the absolute value of the temperature, the proposed technique suggests combining a CTAT and a constant current source for powering up the RO. In the proposed technique, the constant current source provides the major part of biasing current and the CTAT current source has the duty of frequency compensation. To verify the performance of the technique, two different implementations of the circuit are designed and simulated in a standard 0.18µm RF-CMOS process. In one prototype of the circuit, required CTAT current is developed by utilizing the CTAT nature of the threshold voltage, though the other circuit exploits a diode-connected BJT. Simulation results showed that the TC of an uncompensated RO was dramatically reduced from 2400ppm/ºC to 80.4ppm/ºC while the total power consumptions of the first and second configurations were 34.1µW and 14.5µW respectively. Sensitivity analysis for the circuits regarding to the process variations and V_{DD} fluctuations showed the robust behavior of the compensated ROs.

The main novelty of the proposed compensated RO is use of the ring oscillator in subthreshold for achieving low power dissipation, and use of two new low power circuits for biasing and compensation. Since the thermal behavior of the RO in subthreshold is different from that of in above threshold region, therefore the required compensation technique in this paper is completely different from previous works.

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Persian Abstract

چکیده

مصرف توان کم، اندازه کوچک سطح مورد استفاده و ساخت در فرآیند CMOS از الزامات حیاتی در طراحی نوسان سازهای حلقوی است که در افزاره ها و دستگاه‌های قابل کاشت زیستی و پوشیدنی استفاده می‌شود. اما فرکانس نوسان سازهای حلقوی به شدت به دما وابسته است. در این مطالعه یک نوسان ساز حلقوی جبران سازی شده نسبت به دما با توان مصرفی کم پیشنهاد شده است. ترانزیستورهای نوسان‌ساز حلقوی پیشنهادی برای دستیابی به عملکرد با مصرف توان کم و ولتاژ پایین در ناحیه زیرآستانه بایاس شده‌اند. از آنجایی که فرکانس نوسان یک نوسانگر حلقوی معمولی در ناحیه زیرآستانه با افزایش دما افزایش می‌یابد، در تکنیک پیشنهادی، از دو منبع جریان برای تغذیه نوسان ساز حلقوی استفاده می‌شود: یک مرجع جریان مستقل از دما(جریان با افزایش دما ثابت است) و یک مرجع جریان مکملCTAT که با افزایش دما جریان آن کاهش می یابد. در مدار پیشنهادی، جریان CTAT بخش کوچکی از کل جریان مورد نیاز نوسان ساز را تشکیل می‌دهد و وظیفه آن فقط جبران میزان انحراف فرکانس نوسان نسبت به دما است. دو نمونه اولیه از نوسان ساز حلقوی زیرآستانه برای فرکانس هدف ۱ مگاهرتز با استفاده از فناوری0.18 RF CMOS میکرومتر طراحی و شبیه سازی شد. ضریب حرارتی (TC) نوسان ساز حلقوی جبران سازی نشده در محدوده دمایی^{o}C۸۵+ تا ^{o}C٤٠- برابربا ppm/^{o}C۲٤۰۰می باشد، در حالیکه به کارگیری روش پیشنهادی ضریب حرارتی نوسانگر حلقوی را به ppm/^{o}C ۸۰/٤ با مصرف کل توان به اندازه ۵/١٤ میکروووات کاهش داد.