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A New Multi-valued Logic Buffer and Inverter using Metal Oxide Semiconductor Field Effect Transistor Based Differential Amplifier

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ABSTRACT

The aim of this work is to assist the design of decenary Multi-Valued Logic (MVL) circuits. This paper reports a work, in which, analog voltage-based circuitry is used to design MVL circuits. In this paper, some analog circuits are reported as elements that can be used in Multi-Valued Logic (MVL) circuitry. This article reported a Metal Oxide Semiconductor Field Effect Transistor (MOSFET)-Based Differential Amplifier (MBDA) as a key element in designing decenary MVL arithmetic unit. Operating voltage range and linearity of the gain are two important characteristics of this element. The operating voltage range for the MBDA is 0V to 5.5V as a output voltage.The achieved linear gain is within the range of 0.1V to 5.3V. Analog inverter and correction buffer circuits are reported based on MBDA. Analog inverter will be used in computational and logical decenary MVL circuits. The correction buffer is designed as an element to eliminate noises and signal drift at the output of the MVL gates and throughout data transfer.

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1. INTRODUCTION

Silicon is now almost at its maximum speed and efforts are underway to find a suitable way to increase its speed even further. Some researchers believe in speeding up the technology by means of increasing number of processing cores and parallel processing. Other researchers are trying to use other materials, such as GaNi, to speed up digital circuits. However, one of the best ways to increase speed use of multi-valued logic circuits can be a desired solution. Using this method, more each digit can hold more data and, the trope of the circuit and consequently the speed of the circuit is increased. Additionally, increased data density can reduce the area of the circuit, and dependent on the type of design, it is possible to reduce the power consumption of the circuit as well. In other words, by using multi-value circuits, in addition to increasing the circuit speed, it is possible to reduce the area and power consumption simultaneously.

This research is a part of a larger project aimed to build arithmetic and logic units based on decenary Multi-Valued Logic (MVL). Since arithmetic circuitry was designed using voltage-based analog circuits, a differential amplifier with linear gain was required in the design. Linearity of the gain within the maximum possible voltage range was important for the design to be able to provide uniform voltage levels within the most part of the power supply voltage range.

Initially, reported work on similar technologies as the one used in the reported work, i.e., TSMC 180nm, was studied. Hence, a number of reported amplifier designs using 180nm technology were studied. Since none of the reported designs matched the required specifications needed, it was decided to design a new differential amplifier to satisfy the decenary MVL circuits design requirements.

Based on this differential amplifier, an analog inverter was designed to support designed for the decenary MVL arithmetic and logic circuitry, as well as in designing a correction buffer to eliminate noises and signal drift at the output of the MVL gates and throughout data transfer.

In this paper, a MOSFET-Based Differential Amplifier

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(MBDA) circuit with a new composition is presented. MVL circuits are also provided using analog instead of logic switches. This method reduces the complexity of the circuit, the number of transistors and the number of power supplies required in the circuit design. The reported circuits that are presented operate in 10 levels and are designed with uniform levels in terms of voltage. The goal is to design an amplifier with the following specifications:

1. Operating range 0V to 4.5V (decenary levels with 0.5V distance between two levels).
2. Linear gain close to the voltage range between 0V to 4.5V.
3. Amplifier with the lowest number of transistors (9 transistors are used in the reported design)
4. Amplifier with the minimum delay (higher than 100MHz)

The reported inverter and correction buffer are designed based on MBDA.

It is era of rapid change for the computing technology. Digital circuits, such as other parts of the computing technology, need fundamental changes.

2. RELATED WORKS

Many researchers are trying to make these changes in a variety of ways. Multi-Valued Logic (MVL) is an attractive research method in this area. In recent years, many researches were engaged in the field of MVL circuit design. Researchers have used various methods and technologies to implement MVL circuits. However, the main point in the reported researches demonstrated the use of switch logic. In the following, some of these articles and reported methods will be discussed. The reported works are presented in 5 categories.

1. Organic material
2. CNTFET
3. 180nm CMOS
4. Single electron transistor
5. Other technologies

In a reported work by Kim et al. [1], a ternary inverter based on a p-n lateral hetero structure is proposed. In this research, the logical values attributed to the inverter include $(0, {}^{1}/_{2}, 1)$. Length of this inverter is 550μm and the power supply voltage is 10V. Having unequal input/output voltages is a disadvantage for this inverter. As an advantage, the designed circuit uses different silicon layer arrangements to produce a 3-level inverter. In this research, 2D finite-element numerical simulator software was used to simulate the gate. As an example for a new technology, Jeon et al. [2], reported ternary logic circuit based on organic material. In this paper, negative differential resistance/transconductance is the key to the circuit design. Introduced circuits are based on Ambipolar Organic FET (AOFET). The main drawback of this design is the difference between the input and output voltage ranges of the circuit. The input voltage variation is between 0 and 200V while the output voltage variation is between 0 and 50V. Davari Shalamzari et al. [3], reported new quaternary multiplexer, half adder and multiplier using CNTFET. In this paper, designed circuits are compared against similar technologies in terms of power consumption and latency. Results show improvement in terms of circuit delay but power consumption has increased instead. The simulation was performed using HSPICE software and 32nm CNTFET library. In a reported work by Hosseini and Etezadi [4], a novel ternary MVL comparator was introduced that is expandable to a quaternary one. Using CNTFET, the reported MVL comparator was designed and simulated in both ternary and quaternary modes. Later on, Uternary function was extended in to a quaternary function using only 4 transistors. This design was simulated using Stanford 32nm CNTFET library in HSPICE. In a reported work by Jaber et al. [5], a ternary half adder and multiplexer was introduced. These circuits were designed based on 32nm CNTFET and they were simulated in HSPICE simulator. In the reported work, the ternary multiplexer's output current was supplied by one of the inputs. The cascaded number of gates would cause problems such as false voltage levels. Jaber et al. [5], proposed a half-adder where designed based on these multiplexers.

In a reported work by Hosseini and Roosta [6], ternary buffer, inverter, STNOR and STNAND circuits are introduced. In this paper, using HSPICE's CNTFET Stanford 32nm model and 0.9V power supply; they have reached to an operational frequency of 500MHz. In addition, Hosseini and Roosta [6] have compared reported results against similar reported works showing that power and latency were reduced. Chowdhury et al. [7], reported voltage mode NOR and MAX operators. The Max operator was designed using only 3 transistors. Using 2 more transistors, Chowdhury et al. [7] built a NOR operator. Designed circuits were simulated in HSPICE using 180nm library.

In other reported work by Saha and Pal [8], a circuit is proposed to convert ternary logic to binary logic. This circuit consists of 3 parts: Trit-to-Unary Decoder (TUD), Complete Unary Decoder (CUD) and Unary-to-Binary Converter (UBC). These 3 sections are arranged in series; therefore, the circuit delay is equal to the total delay of these sections. The proposed circuit was designed using TSMC 180nm model. Layout design and simulation is done using T-Spice. Simulation results showed that the circuit delay is 0.72ns and the power consumption of the

circuit at 500MTPS was 177.74µW. The circuit area was $13.77x10^2µm^2$ and 280 transistors were used in designing this circuit.

The Single Electron Transistor (SET) has low power consumption [9-11]. As an example, in a work reported by Gope et al. [12] a ternary Flip-Flop (FF) was designed. In this work, a completely different set of FF models were reported where the only problem was the use of large number of transistors in the design.

Sandhie et al. [13], reported ternary logic circuits based on GNRFET. In this reported work, the supply voltage was 1V and the distance between the 2 levels was 0.5V. Simulation is performed using HSPICE-GNRFET 16nm where STI and PTI gate circuits were built. STI and PTI gates were designed using 6 transistors and 2 transistors respectively. The STI gate was compared against a similar CNTFET model in terms of power consumption and latency. In both cases the proposed circuit showed improvement.

Other methods have been used to design and implement multi-valued circuits. For example, in the paper presented by Karmakar [14], a ternary inverter is built using quantum dot gate. The circuit model is designed based on Barkley Short Channel IGFET Model (BSIM) in VHDL. This paper presents 3 standard inverters Negative Ternary Inverter (NTI), Positive Ternary Inverter (PTI) and Standard Ternary Inverter (STI). Charjee et al. [15], reported a novel Random Access Memory (RAM) using MVL and fuzzy logic operators. In this paper, fuzzy interface system used with a limited number of logical steps and a 1x3 memristive crossbar array to develop a MVL-based RAM (MVLRAM). In the paper presented by Sharma and Kumre [16], a ternary arithmetic logic unit is presented. HSPICE's Stanford 32nm CNTFET model is used to design the circuits. The proposed operators include MUX, Adder, Subtractor, Multiplier and comparator. This article presents one of the most complete sets for logic and calculus operations.

Since the most important part of the article is about differential amplifiers, a number of the amplifiers provided will be also reviewed. An important feature of the amplifier in this paper is the linearity of the Voltage Transfer Characteristics (VTC).

In a reported work by Dvornikov et al. [17], a novel operational amplifier (Op-Amp) is reported. Reported Op-Amp designed based on 2 technological routes, "Inch-R/NJFET" and "Inch-P/PJFET" and simulated in LT spice CAD.

The simulation results at -197°C indicate the Op-Amp operates perfectly. Circuit power supply was 5V and current consumption was about 360µA. VTC simulated at -197°C and the linear part of graph is between -3V to 3V at the output.

In another work reported by Kuzmicz [18], a simple ultra-low power Op-Amp described. The reported Op-Amp designed in 22nm CMOS FDSOI technology with very low current consumption about 1.1µA at 0.8V power supply. In this research, 49 prototype chips tested at 0.8V supply and room temperature. Test results show the VTC graph is linear in whole power supply (0V to 0.8V).

In a research reported by Alam et al. [19], a capacitance to voltage converter is presented. This circuit was simulated using PSPICE model parameters based on standard 0.13µm CMOS process. Circuit power supply was 1.2V and the circuit combined capacitor network to the Op-Amp. VTC graph show the linear response from about -1V to 0.8V at the output.

In the paper presented by Raut et al. [20], a two-stage Op-Amp is designed using 180nm CMOS technology. The proposed Op-Amp gain is about 74.9dB and its bandwidth is 7.26 MHz. The reported Op-Amp has a classic design structure.

In another work presented by Dash et al. [21], an Op-Amp with 180nm CMOS technology is presented. One of the positive points of this Op-Amp is the low number of transistors used in this design. This Op-Amp is designed using only 8 transistors. The power supply of the circuit is 1.8V and the gain of the circuit is about 60dB.

Circuits and results presented in this paper are part of the design and results of a larger project. The main project consists of 3 main parts.

1. Designing a complete decenary (10-valued) logic with related circuits
2. Decenary memory circuit design
3. Decenary arithmetic circuits

The logic and memory sections are currently completed. For the computational part, it is necessary to design 3 basic circuits that are introduced in this article. This article is a continuation of previous research where novel decenary logic was presented. In the proposed logic, the voltage distance between 2 logic levels is considered to be 0.5V.

This paper presents elements for designing decenary MVL circuits. The reported elements designed and implemented using Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistors. In section 2, general characteristics of the proposed circuits will be explained. In section 3, the MBDA circuit will be presented which is a simplified differential amplifier design suitable for use in decenary MVL circuits. Later on, the introduction of the proposed analog inverter will be reported in section 4. In section 5, correction buffer circuit will be followed. The inverter is designed to be

analog and based on decenary MVL. Correction buffer is designed and provided to correct noise and drift errors in analog circuits within the designed circuitry. In the final section, conclusions and future work conclude the paper.

3. CIRCUIT SPECIFICATIONS

The proposed circuits are designed and simulated using the PSPICE's TSMC 180nm model [22]. The circuits have 2 supply voltages of 5.5V and -0.5V. These supply voltages are far from the transistor breakdown voltage.

For 180nm transistors, the breakdown voltage is approximately equal to 10V [23-25]. All the proposed circuits operate in analog mode and only the correction buffer circuit has a switching logic at its output. The voltage distance between the 2 levels is 0.5V. Logic level 0 is indicated by 0V and logic level 9 is indicated by 4.5V.

4. MOSFET BASED DIFFERENTIAL AMPLIFIER

A differential amplifier is a requirement for many analog operations. A number of reported differential amplifier designs with 180nm technology were tested; however, none of them satisfied specifications needed in the required decenary MVL circuit design [26-28].

Satisfying needed design requirements, a suitable amplifier had to have two necessary characteristics. Firstly, it should be able to operate in the whole range of 0V to 4.5V. Secondly, within this interval, the gain should be linear. In this application, the size of the gain is not as important as its linearity.

The reported works in this area either did not cover the voltage range required in the reported decenary MVL circuit designs [20, 21], or their gain was not linear enough [17-19].

For example, in an article submitted by Raut et al. [20], the gain circuit is excellent in terms of linearity, However, in terms of operating voltage range, the required voltage range is not provided. The operating voltage range in the provided amplifier is from -1.8V to 1.75V. In another reported work by Alam et al. [19], linear interval size of the amplifier gain is not enough. The reported linear interval is a little over 1.5V.

In decenary MVL circuits, linear gain ensures equal distances between logical levels at the output of the circuit.

Several logical conditions are required to define a differential amplifier behavior. The proposed circuit must have 2 inputs and 1 output. One of the inputs will be named positive and the other negative. Dealing with special operational conditions, operation of the proposed MBDA is set to the following special conditions. If the positive input voltage is greater than the negative input voltage, the output will be equal to the positive supply voltage. If the negative input voltage is greater than the positive input voltage, the output will be equal to the negative supply voltage. In other words, the output voltage is limited by the power supply.

The proposed MBDA circuit consists of 2 stages. Figure 1 shows the MBDA input stage, i.e., stage 1. The input stage is quite similar to other differential amplifiers. This stage is designed based on the current mirror circuit. Since gates Q1 and Q2 have the same voltages, the current passing through both transistors is the same. A small difference between the voltages of gates Q3 and Q4 causes the output voltage of the circuit to be switched high or low. These high and low signals are not strong enough and similar to the other differential amplifiers, there is a need for another circuitry stage to amplify weak high and low. In digital circuitry, weak signal is defined as a signal that is not a full swing. The same thing happens at the output of this circuit.

The easiest way to amplify these weak signals is to use a binary inverter. Stage 2 of the circuit is shown in Figure 2. The stage 2 of the circuit consists of 2 inverters and a capacitor. There are 2 reasons for using 2 inverters. First, an inverter is incapable of sharply switching to power supply voltage or ground. Second, increasing the W/L ratio requires a 2 layered circuit (to increase amplifier output current). Finally, the reason for the presence of capacitor C in the circuit is due to the destructive effect of the feedback. Differential amplifiers are usually biased with feedback. A feedback resistor is usually used to connect the output to the input. Due to the resistance path of the feedback and gate capacitor at the input, there is a delay in applying the feedback loop. This delay will cause the output of the Differential amplifier to oscillate. Capacitor C on the second stage of the circuit suffocates this oscillation. Figure 3 shows the complete MBDA circuit.

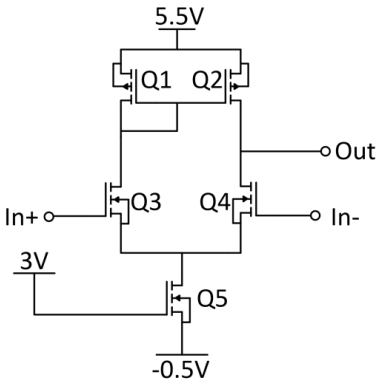

Figure 1. First stage of MBDA

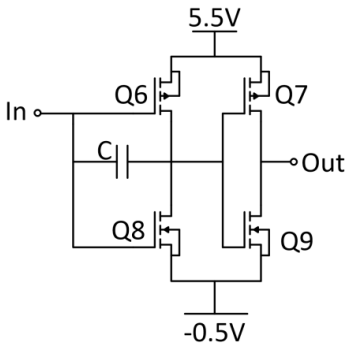

Figure 2. Second stage of MBDA

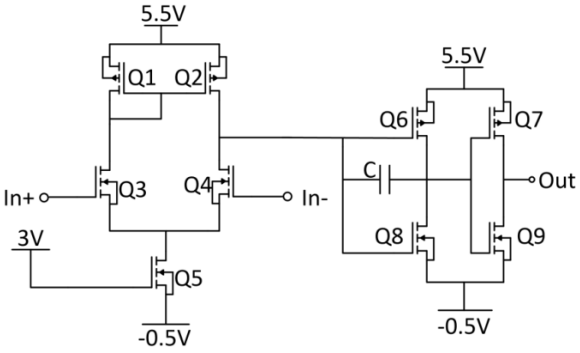

Figure 3. MBDA complete circuit

Validating functionality of the proposed MBDA, the MBDA circuit was simulated using 2 different input signals, i.e., non-inverting amplifier, Figure 4 and non-inverting summing amplifier Figure 5. In the non-inverting amplifier circuit, the circuit gain is 1. The simulation for the circuit is performed using 2 types of sinusoidal and stepped signal inputs.

Figure 6 shows the simulation results for these 2 types of input signals. In Figure 6 part (a) MVL signal sample is applied to the MBDA. In Figure 6 part (b), the sinusoidal signal is applied to the MBDA at 300 MHz (as its maximum frequency, the phase shift in it is quite clear). Figure 6 part (c), a sinusoidal signal, with an appropriate frequency (30 MHz) for the design is applied to the MBDA.

Figure 5 is an extended version of Figure 4 with 2 inputs. The algebraic sum of the 2 input voltages will appear at the output of the circuit. Simulation results for these 2 types of inputs are presented in Figure 7. Simulation results show that the pseudo MBDA circuit behaves close to the performance of a normal MBDA. The output of a normal differential amplifier circuit with non-inverting amplifier bias is obtained using Equation (1).

The open-loop gain is also calculated from Equations (2) to (5).

$$V_{in} = \frac{R_2}{R_2+R_F} \times V_{out} \quad (1)$$

$$V_o = \frac{-jX_c}{R_o-jX_c} AV_{id} \quad (2)$$

$$-jX_c = \frac{1}{j2\pi fc} \quad (3)$$

$$V_o = \frac{AV_{id}}{1+j2\pi fR_oc} \quad (4)$$

$$A_{ol} = \frac{V_o}{V_{id}} \quad (5)$$

In the reported work, the open-loop gain is measured by means of simulation.

Simulation results closely follow Equation (1). Table 1 shows the W/L ratio of each transistor.

The static power consumption of a MBDA is 38.32µW and the MBDA latency at its worst is 3.28ns. MBDA Voltage Transfer Characteristics (VTC) open-loop is given in Figure 8. VTC graph is given in -40°C, 25°C and 80°C temperature.

4. 1. MBDA Specifications Since the reported MBDA circuit cannot be considered a normal differential amplifier, it cannot be easily compared against other

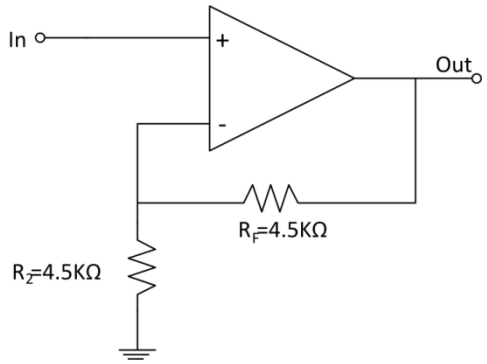

Figure 4. Non-inverting amplifier schematic

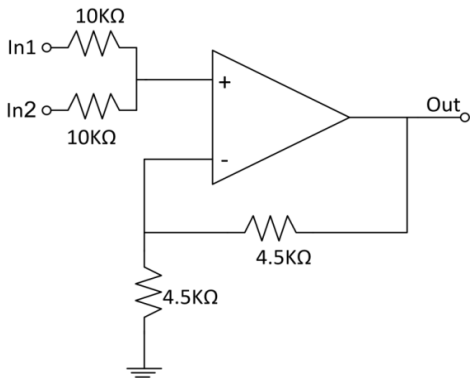

Figure 5. Non-inverting summing amplifier schematic

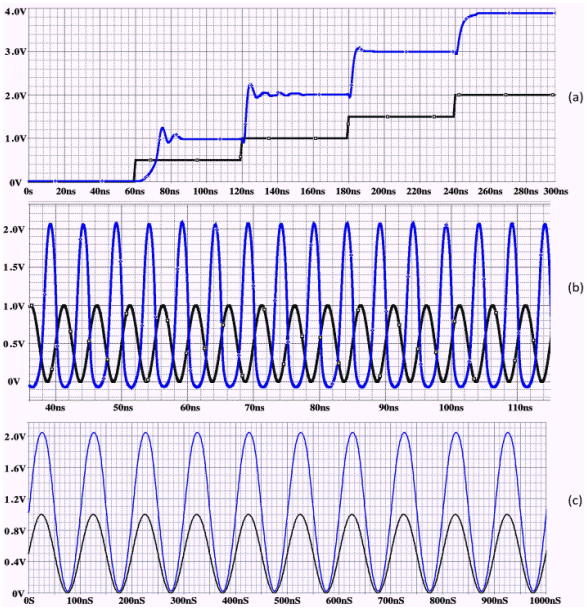

Figure 6. Non-inverting amplifier results (black: input, blue: output)

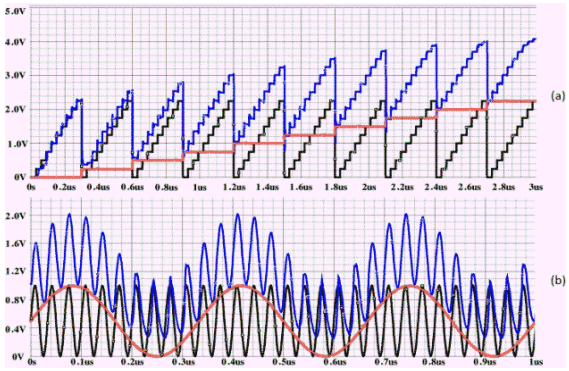

Figure 7. Non-inverting summing amplifier results (red & black: inputs, blue: output)

TABLE 1. Value of the W/L ratio of MBDA circuit transistors

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9
W/L	1.5	1.5	1.5	1.5	1.5	6	6	6	4.5

differential amplifiers. Difference between this MBDA and other similar differential amplifiers lays in the main purpose of its design. This element was not designed to produce power gain or for any other typical uses of a differential amplifier. The reported MBDA circuit specially designed for use in multi-valued circuits. However, as for comparison its analog specifications can be addressed.

The analog characteristics obtained from the simulation are presented in Table 2. Slew Rate (SR) and Unity Gain Bandwidth (UGB) values are reported in Table 2.

Although it will be very difficult to compare the reported MBDA against other reported ones, some of its specifications have been compared against 2 regular differential amps. Table 3 summarized the Open-loop characteristics of proposed MBDA. The comparison at 25 °C is given in Table 4 [17-20].

According to the linear gain of the MBDA, in Table 4, a series of comparisons with similar circuits are also provided. Table 4 compares variouus characteristics of the MBDA circuit provided against the other 4 differential amplifier designs. The proposed MBDA circuit performs better than other compared differential amplifiers in terms of UGB characteristics and linearity ratio along with linearity amplitude. In this research, amplitude and linearity ratio are very important for designing MVL circuits.

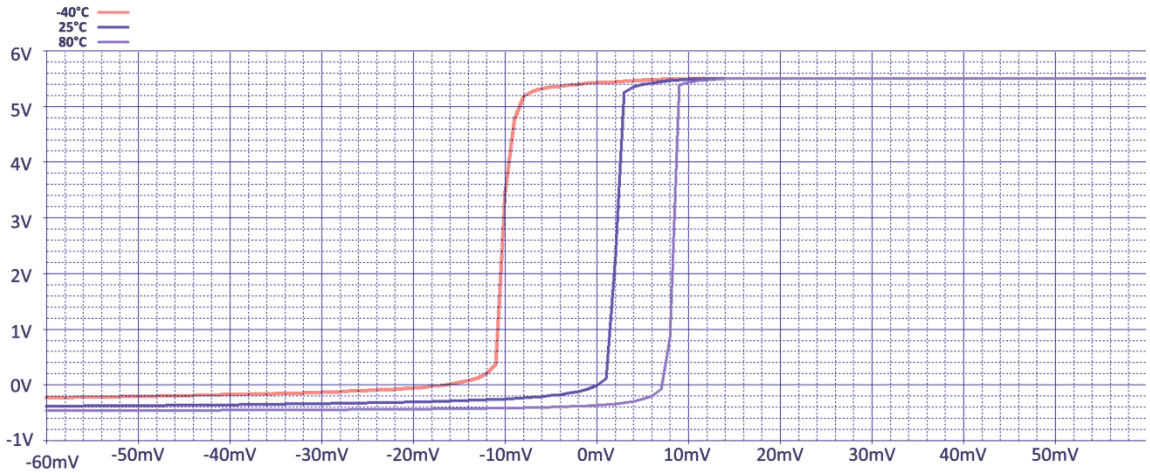

Figure 8. MBDA's open-loop VTC chart

TABLE 2. MBDA specifications

Temperature (°C)	Voltage (V)	Power Gain (dB)	SR (V/ns)	Settling time (ns)	Output swing (V)	UGB (MHz)
	2	40.53	0.33	5.9	1.96	330
-40	1.2	43.22	0.15	8	1.201	230
	1	45.38	0.1	9.9	1.01	200
	2	40.2	0.22	9	1.95	220
25	1.2	43.28	0.09	12.9	1.199	151
	1	44.68	0.07	14.95	1.02	140
	2	40.07	0.2	9	1.96	202
80	1.2	43.01	0.09	13.1	1.203	148
	1	44.17	0.06	16.15ns	1.01	121

TABLE 3. Open-loop characteristics of proposed MBDA

Supply Voltage (V)	5.5
Current Consumption (µA)	44
Power Consumption (µW)	242
Open-Loop Gain ratio – (dB)	423 – (52.528)
Process	TSMC 180 nm

4. 2. Experimental Results Designing the differential amplifier started with 4 aforementioned goals in section 4. The first objective was to have the MBDA to operate within the range of 0V to 4.5V. Given the ability to produce output from about -0.5V to 5.5V, the first goal has been achieved.

The second goal was to have a linear gain within the range of 0V to 4.5V. This goal has also been met by achieving a linear gain of about 0.1V to 5.3V. Two measurements were used to compare Gain's linearity in amplifiers. The first measurement is called the Linearity Gain Region (LGR). LGR is the area between start and end voltage points of the linear gain region of the open-loop VTC curve. LG measured in this circuit from is between 0.1V to 5.3V. This means that the voltage ranges for the linearity of the gain in the reported differential amplifier covers %86.66 of the power supply's voltage, i.e. Linearity Ratio or LR. The second measurement is the Maximum Difference (MD) from the straight line connecting the two LG points (Figure 9). In the reported MDBA, measured MD is about 400µV.

The third measurement is the number of transistors used in the circuit. Compared versus other reported circuits for the differential amplifier, the reported work uses 9 transistors are suitable.

TABLE 4. Comparing the proposed MBDA against two other reported differential amplifier designs

	Gain (dB)	UGB (MHz)	Technology (nm)	Linearity Gain Region (LGR)	Power Supply	Linearity Ratio (LR)	Number of Transistors
Reported MBDA	52.528	220	180 (CMOS)	0.1V to 5.3V	-0.5V to 5.5V	%86.66	9
[20]	40	0.114	180 (CMOS)	Not specified.	-1.8V to 1.8V	Not specified.	8
[17]	97.1	Not specified.	6 (JFET)	-2.79V to 2.79V	-5V to 5V	%55.8	20
[18]	73.8	0.14	22 (CMOS)	0V to 0.8V	0V to 0.8V	%100	9
[19]	29.948	1.8	130 (CMOS)	-1V to 0.8V	-1.2V to 1.2V	%75	18

Finally, the circuit delay is given in detail in Table 2. The delay is greater than expected, but does not rule out circuit design and delay is within acceptable limits, i.e., less than 100ns.

5. ANALOG INVERTER

Having built a MBDA circuit, design of an analog multi-valued inverter would be simplified. It is enough to implement the circuit in Figure 10, which is very similar to an inverting amplifier with a gain of 1. Inversion to the positive input voltage is done in MBDA. Figure 11 shows simulation results for the inverter with 3 input types. A decenary low-frequency input signal simulation result is presented in Figure 11 (a). Figure 11 (b) shows simulation results for the same input at 100 MHz (as high

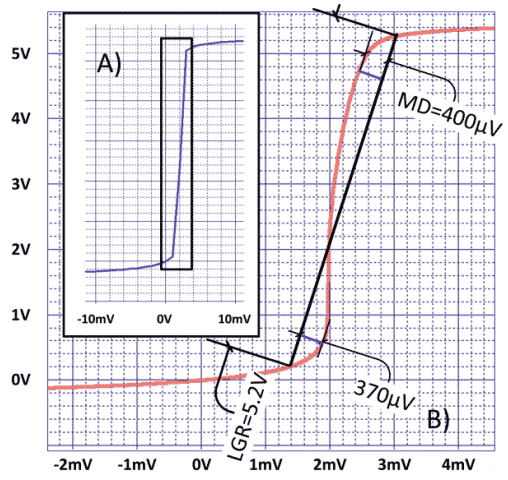

Figure 9. Gain linearity comparison A) zoom out, B) zoom in

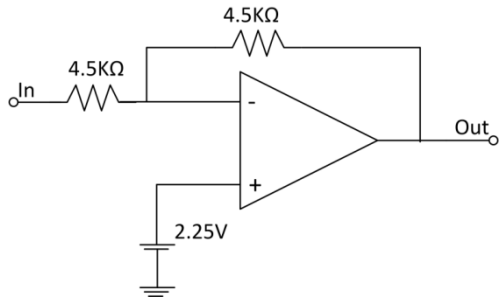

Figure 10. Analog inverter

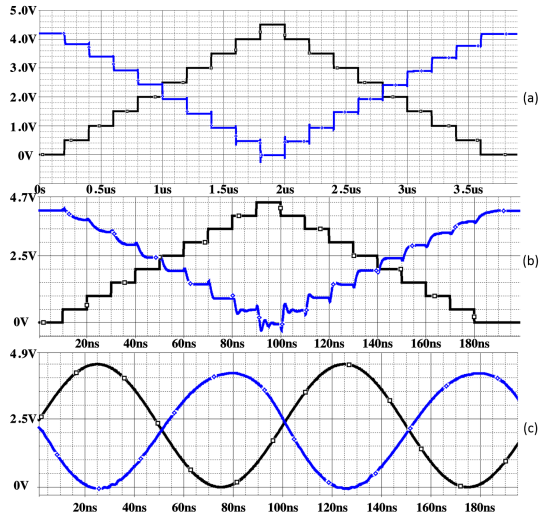

Figure 11. Analog inverter simulation results (black: input, blue: output)

frequency). Finally, Figure 11 (c) shows simulation results for a sinusoidal input signal, at 10 MHz (as low frequency). It should be noted that analog input is provided only to show its performance as an analog circuitry.

The proposed analog inverter, with decenary logic input, is equivalent to a standard inverter in ternary logic. The proposed inverter will be used in computational circuits in a similar way to a differential amplifier. In the proposed circuit, the power consumption is greater than 70µW, and it is dependent on the circuit bias. The worst case delay is 10ns.

6. CORRECTION BUFFER

In the reported circuits, since the circuits are analog, effects of noise and drift are major drawbacks in the design. It is not possible to cascade the circuits due to the noise and drift effects. Noise effect occurs due to the absence of marginal noise and with high sensitivity. Drift means the displacement of the circuit's output voltage from the desired voltage. Inaccuracy of the physical values that determine circuit operation, such as, values of the resistors is the main reason for the drift. Correcting this problem, a correction buffer is required at the output of the circuit.

By means of this correction buffer, the possible voltage drift can be removed from the output. The correction buffer circuitry is designed based on the proposed MBDA. In the MBDA used for the correction buffer, the dumping C capacitor in Figure 2 is removed. Since these comparators do not have feedbacks and their outputs will not fluctuate due to capacitance-resistance delay. Figure 12 shows the correction buffer circuit in general.

On the output stage, the proposed correction buffer circuit behaves similar to an analog buffer. However, output of the circuit cannot reach -0.5V or 5.5V. This is due to the threshold voltage of the transistors that can vary in the maximum range of 0V to 5V. Threshold voltage is not an issue for the output of the proposed decenary circuitry, because the voltage range of the decenary circuit is 0 to 4.5V. Different types of input signals were applied to the circuit to demonstrate its performance. 3 types of input signals were applied to the proposed correction buffer circuit and simulation results are reported in Figure 13.

A Triangular signal, 2 sinusoidal signals and a decenary logic signal with a drift are applied to the circuit. The simulation results are reported. The output of each comparator is either 0V or 4.5V (dependent on the comparison situation sometimes it will be 4.5V and sometimes 0V).

Similar to a resistor ladder, due to the wired summing voltage resistance, each 4.5V adds 0.5V to the main output of the circuit. For every 0.5V increase in input voltage, the output of the comparator will change from

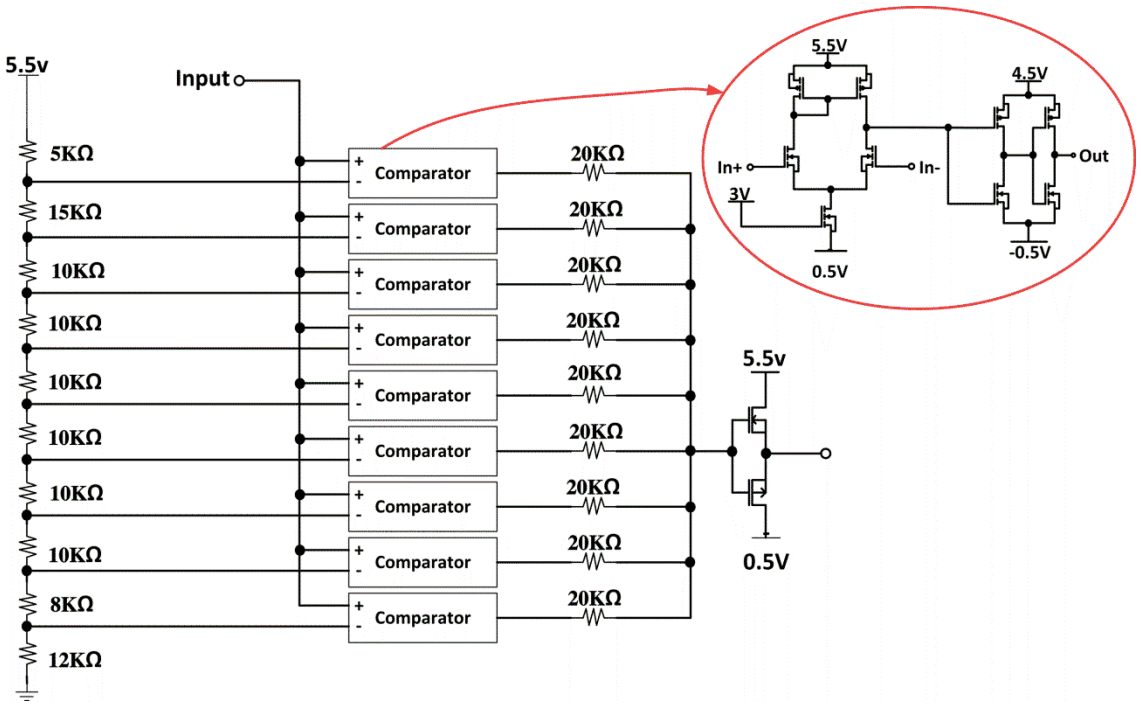

Figure 12. Correction buffer

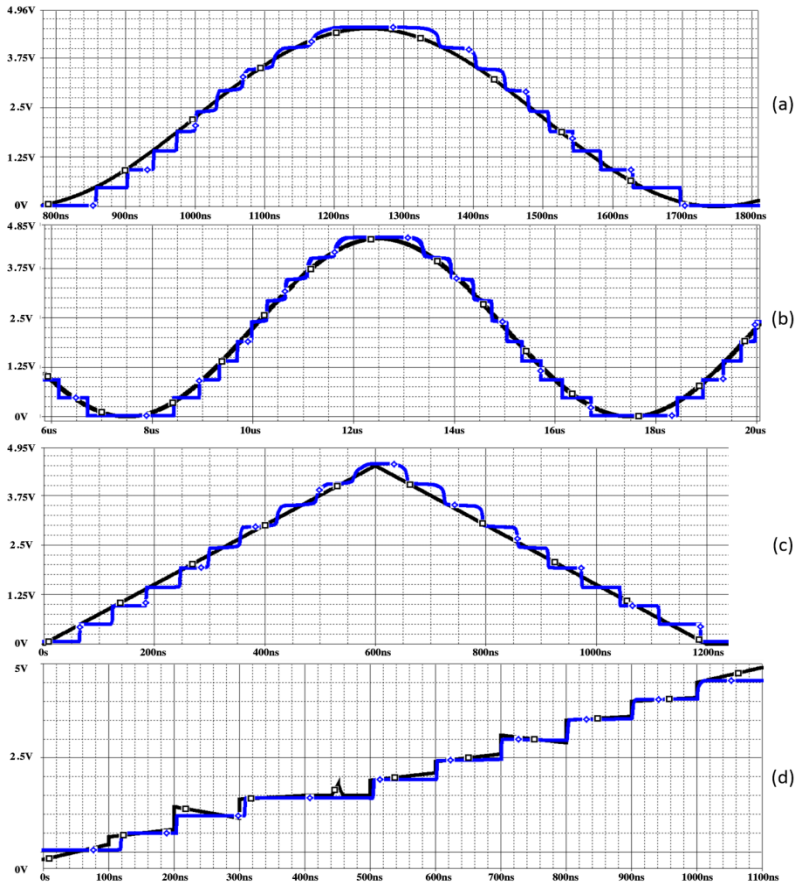

Figure 13. (a) High frequency sinusoidal signal (b) Low frequency sinusoidal signal (c) Triangular signal (d) Decenary signal results (black: input, blue: output)

0V to 4.5V. According to the simulations performed, this circuit functions as a quantizer in ADCs. The static power consumption of the circuit is about 272µW and is dependent on the resistors used in the circuit. Delay of the circuit is 20ns at its worst.

7. CONCLUSION AND FUTURE WORK

This article reports an ongoing work on the design of decenary logic circuits based on analog circuits. The goal of this research is to provide the elements needed to design MVL computational circuits. A MBDA was introduced in this paper. Contributions in MBDA circuit include the operational voltage range suitable for the application of a decenary circuit, and a differential amplifier with linear gain, i.e., MBDA.

Since the voltage distance between each level and the next level is 0.5v, the MBDA should be able to operate from 0V to 4.5V (Input voltage range and output voltage range). The proposed MBDA is capable of operating from 0V to 5.5V.

In MDBA, the linearity of the gain in the whole range of the operating voltage helps to ensure that the voltage value of each level is correct (without the need to change the MBDA resistance configuration). The proposed MBDA Gain is linear within the voltage range of 0.1V to 5.3V.

MBDA is the element by which other elements will be designed. This paper reports a decenary inverting circuit as well. Finally, a correction buffer is designed and simulated to control the error caused by noise and drift.

The analog circuits used in MVL will reduce number of the transistors and thus reduces complexity of the circuit. However, use of analog circuits will not be without its drawbacks, e.g., sensitivity to noise and drift of the output circuit that are due to the tolerance of the components. This problem has been completely fixed with the design of the corrective buffer. Correction buffer should be used at output of the chip or the feedback sections.

In other words, additional circuitry will be required to fix the noise and drift effects. Simulation results confirm correctness of the operation of the proposed circuits.

In future work, intention to complete the arithmetic circuits section using analog logic. The reported circuits have the same specifications (levels voltage distance, number of levels, manufacturing technology, voltage of power supplies) as with the decenary MVL family circuitry as discussed earlier in section 1. The most important of these drawbacks are the higher sensitivity to noise and drift of the output circuit that are due to the tolerance of the components. This problem is fixed with the design of the corrective buffer. Correction buffer should be used at the output of the chip or the feedback sections. In other words, additional circuitry will be required to fix the noise and drift effects.

Simulation results confirm correctness of the operation of the proposed circuits. In future work, circuits with the same specifications will be introduced. These circuits include decenary logic circuitries and a decenary memory circuit.

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Persian Abstract

چکیده

هدف از کار ارائه شده، کمک به طراحی مدارهای ۱۰ ارزشی است. مدارهای مد ولتاژ آنالوگ که در منطق چندارزشی بکار گرفته شده‌اند در این مقاله ارائه شده است. تقویت کننده دیفرانسیلی بر پایه MOSFET (MBDA) ارائه شده، المان اساسی بکارگرفته شده در مدارهای ۱۰ ارزشی است. ویژگی‌های‌اساسی این المان بازه ولتاژی و خطی بودن گین آن است. بازه ولتاژی MBDA از ۰ تا ۵.۵ ولت است و بازه خطی بودن مدار از ۰.۱ ولت تا ۵.۳ ولت است. همچنین دو مدار معکوس کننده آنالوگ و بافر تصحیح کننده برپایه MBDA طراحی شده است.کاربرد مدار معکوس کننده آنالوگ در مدارهای محاسباتی و منطقی ۱۰ ارزشی خواهد بود. بافر تصحیح کننده نیز به عنوان ابزاری برای حذف نویز و لغزش سیگنال در خروجی گیت‌های چند ارزشی و در زمان انتقال داده بکار گرفته خواهد شد.