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Design of Area Efficient Single Bit Comparator Circuit using Quantum dot Cellular Automata and its Digital Logic Gates Realization

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ABSTRACT

Quantum dot cellular automata (QCA) is a promising transistor less nano-technology that is growing in popularity and it has the capability to replace the ubiquitous complementary metal oxide Semiconductor (CMOS) technology in the VLSI domain. The paper discussed the simple design of single bit comparator circuit using QCA. A single-bit comparator circuit compares its two inputs and indicates which one is larger or are they both equal. This paper has focused on creating an area efficient QCA comparator circuit and a comparative study of area consumption with the previously made designs. The designed comparator circuit is the most area-efficient design as it is made up of minimum possible number of cells. A comparator is used in equality testers and many other digital communications The circuit proposed in this paper is a three layered circuit which can alternatively be used to realize the basic logic gates. The circuit can also be used as an alternative to the majority and universal gates in QCA.

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1. INTRODUCTION

Though CMOS technology is currently the most preferred technology in VLSI circuit design, it has few drawbacks in terms of high leakage current. On the other hand, in QCA technology the power consumption, area required are very low. It also supports very high-speed operation (in the range of THz) because it uses the polarization as the mode of operation. These features give QCA the upper hand and research are going on in this domain. Figure 1 shows a QCA cell. The orientation of the electrons will give us the indication whether it's a Logic 0 or Logic 1.

The basic gate in this technology is a majority voter gate [1] which can be programmed to act as an AND gate or an OR gate depending on the control value given. When control value +1 is given, it acts like an OR gate and when the control input is -1, it acts like an AND gate. Many circuits have been implemented using this majority gate like adders and subtractors [2-3], multiplexers [4-5] and decoders [6] which are the basic building blocks of any digital circuit. Figure 2 shows the QCA design of a majority voter gate. In this paper, we have discussed another building block, i.e., comparators (1-bit). A novel design of a 1-bit comparator has been proposed and then compared against the previously available comparators [7-18].

The paper is organized in this way: current section i.e. section 1 discussed about the introduction of QCA and role of kink energy in QCA based circuit, section 2 describes the detail design of the comparator circuit. Section 3 discussed implementation of various logic gates using the designed comparator circuit and section 4 is for the observation and conclusion of the work.

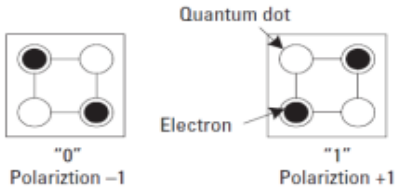

Figure 1. QCA cell with the polarizations

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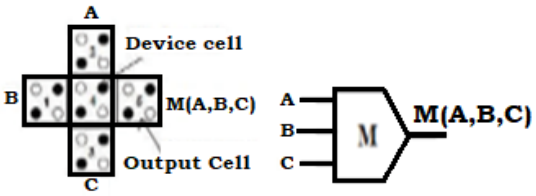


Figure 2. Majority Voter Gate

Kink energy plays an important role in QCA based designs as it should be minimum for the stable output of the circuit.

The kink energy (in Joule) between two electron charges is calculated using the formula: -

$U = (k.Q_1.Q_2)/ r$

Where $k = 1/ (4\pi\epsilon_0\epsilon_r) = 9 \times 10^9$,

$Q_1 = Q_2$ = charge of an electron = 1.6×10^{-19}C.

$U = 23.04 \times 10^{-29}/ r$

r = distance between the two charges.

$U_T = \sum_i U_i$

U_T = summation of all the individual kink energies (in Joule).

For this calculation, the below postulates are considered. (This has been shown diagrammatically in Figure 3)

1) All cells are alike and the distance from end to end of each cell is 18nm.

2) The space between two neighbouring cells (interspacing distance) is 2nm.

3) The diameter of each quantum dot is 5nm.

4) The distance between the two layers used for the design is 11.5nm.

Another important aspect in every QCA design is the clock. In QCA, clock is used to define the direction of state transition. The clocks are what that gives power to the QCA cells to operate. Clocking plays an important role in synchronizing all parts of a complex digital circuit. There are four clocking zones namely, Switch, Hold, Release, Relax as shown in Figure 4. During switch phase, inter dot barriers are raised and the cells become polarized according to the driver polarization state. In the hold phase as the name suggests, the inter dot barriers continue to be high so that the cells preserve their current states. In release phase, the inter dot barriers become low and the cells go to an unpolarized state. The relax phase keep the barriers low so that the cells can remain in that unpolarized state.

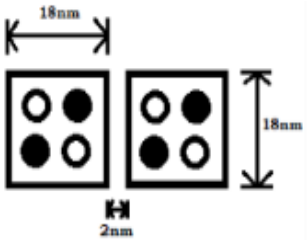


Figure 3. Dimensions of the QCA cells

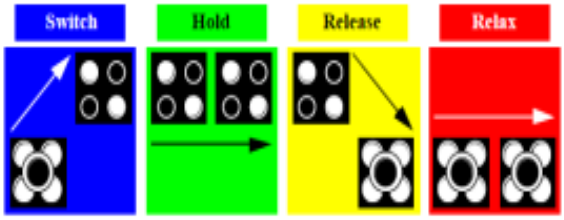


Figure 4. Four phases of a clock signal

2. SINGLE BIT COMPARATOR USING 14 CELLS

A single bit comparator is a combinational circuit that compares two bits. It has two inputs for two single bit numbers each and three outputs are for less than, equal to, and greater than comparison between two binary numbers.

Figure 5(a) shows the design of a more area efficient 1 bit comparator consisting of 14 cells. This design consists of only 14 cells which is the least number of cells used to design a QCA comparator circuit till date. Figure 6 shows the different layers of the circuit. The simulated output of the designed circuit is shown in Figure 7.

Figures 8a and 8b show the polarization and energy dissipation graph with respect to temperature respectively. Figure 8c shows the mapping of the power dissipation across the QCA cells. On mapping this result with the correspondng circuit diagram, we can see that the A>B and A<B output cells dissipates almost equal amount of power which is more than the power dissipated by the A=B output cell. Table 1 shows the different energy calculations for the comparator circuit.

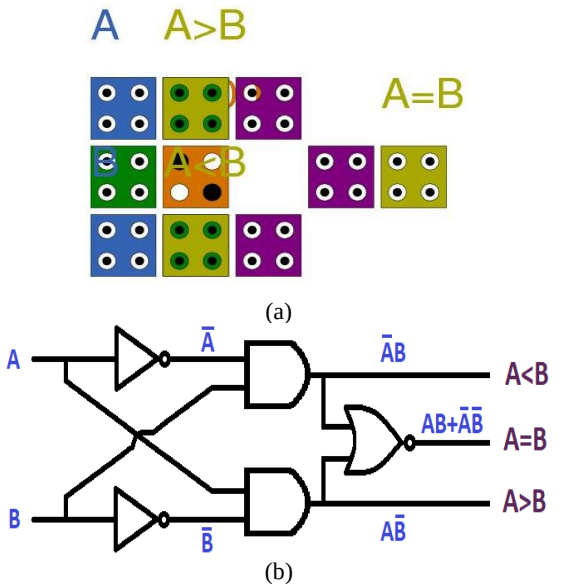


Figure 5. (a) QCA design of proposed comparator with 14 cells (b) Digital circuit diagram of a single-bit comparator

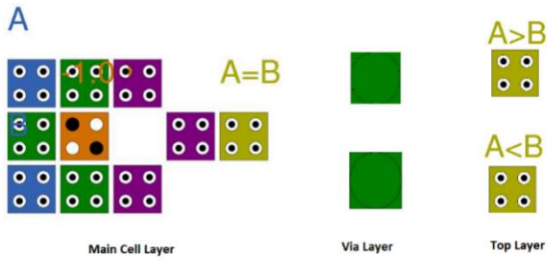


Figure 6. Breakup of the 3 layers in the circuit

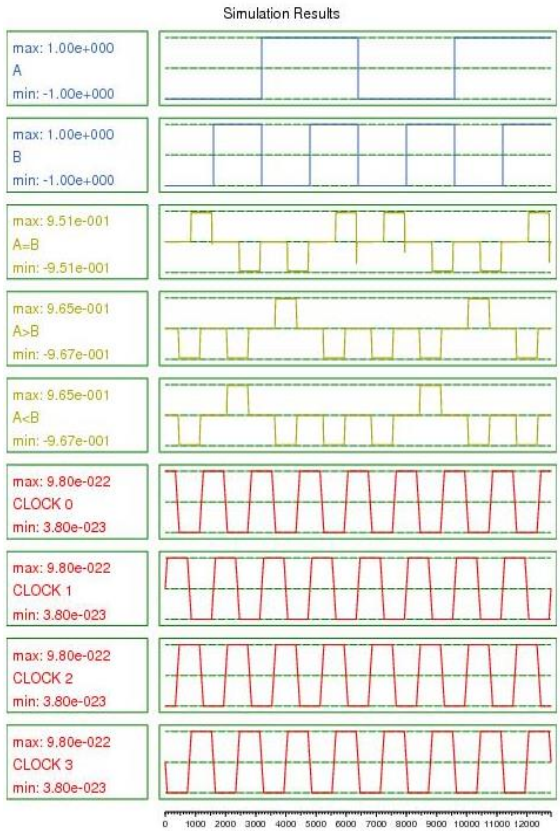
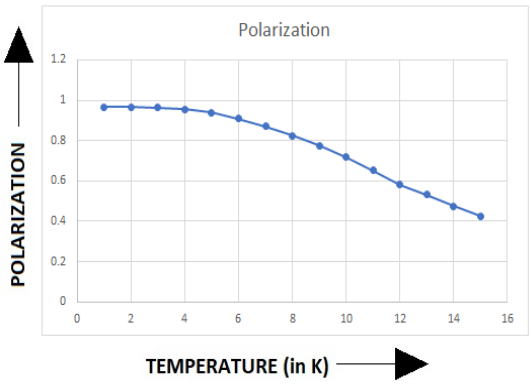
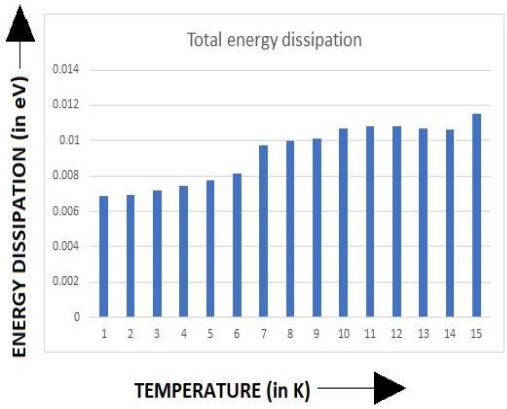


Figure 7. Output of proposed Comparator Circuit



(a)



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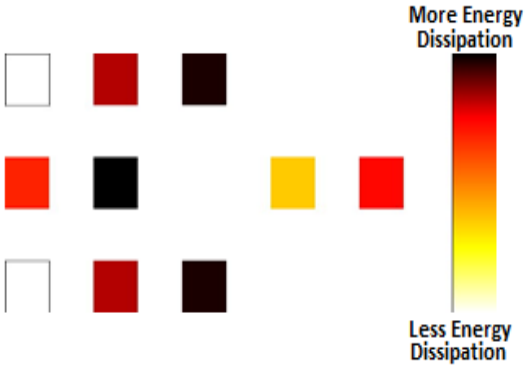


(c)

Figure 8. (a) Polarization vs Temperature (b) Energy Dissipation vs Temperature (c) Power Dissipation Mapping using QCAPro[19-20]

TABLE 1. Power Parameters of the Comparator Circuit

Power Parameters	Values
Total Energy Dissipation (in Joule)	10.96×10^{-22}
Average Energy Dissipation per Cycle (in Joule)	9.952×10^{-23}
Average Power Dissipation (in pico Watts)	181

Now, we calculate the kink energy. Kink energy is basically defined as the energy difference between two neighbouring or adjacent cells. Kink energy between two cells depends on the dimension of the QCA cell as well as the spacing between adjacent cells. It is independent on temperature. It is one of the most significant parameters for the stability of the design. The state having minimum kink Energy is most stable state.

Below, two sets of input values are taken and the kink energy of all the corresponding output cells with respect to each input are calculated. The inputs taken are

a> A=1, B=0: Naturally as A is greater than B, the A>B output cell will give output as '1' and the rest outputs will be '0';

b> A=1, B=1: Similarly, the A=B output cell will give output '1' and the others will give output '0'.

The yellow cells indicate the output cells, green cells indicate the cells are in 1st clock (Clock 0) and pink cells indicate the cells are in 2nd clock (Clock 1). All the electrons (black dots) are arranged such that minimal possible energy configuration is achieved. Then the kink energies are calculated.

In a QCA cell, there are four quantum dots but maximum two electrons are present inside a cell which occupies the opposite cornered position as it is the most stable configuration i.e. the least energy state.

In Figure 9, x_1 and x_2 represents the two opposite cornered electrons of the output cells. Similarly, e_1 and e_2 represents the two electrons of the cell nearest to the output cell. For A>B and A<B, the cells are present in two different layers, outout cell (in the top layer) lies just above the neighboring cell (in the via layer) but for A=B, the cells are on the same the same layer adjacent to each other.

Other cells present in the circuit are further away from the output cell. That is why, the distance between the electrons of the output cell and other cells are so high that the corresponding individual kink energies are too negligible to be considered for the calculation. Tables 2 and 3 shows the kink energy calculations for different inputs of A and B.

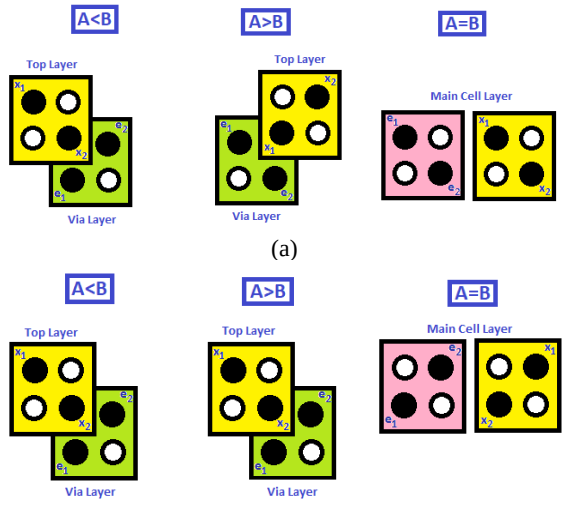


Figure 9. Reference Diagram for Kink Energy calculation for (a) A=1and B=0 (b) A=1 and B=1

TABLE 2. Kink Energies for A=1 and B=0 ($\times 10^{-21}$)

INPUT: A=1, B=0						
Kink Energy (Ue)	**A>B**		**A=B**		**A<B**	
	x1	**x2**	**x1**	**x2**	**x1**	**x2**
Ue_1	15.8	15.8	11.5	7.6	15.8	15.8
Ue_2	15.8	15.8	16.2	11.5	15.8	15.8
Total (U_T)	31.6	31.6	27.7	19.1	31.6	31.6

TABLE 3. Kink Energies for A=1 and B=1 ($\times 10^{-21}$)

INPUT: A=1, B=1						
Kink Energy (Ue)	**A>B**		**A=B**		**A<B**	
	x1	**x2**	**x1**	**x2**	**x1**	**x2**
Ue_1	15.8	15.8	11.5	16.2	15.8	15.8
Ue_2	15.8	15.8	7.6	11.5	15.8	15.8
Total (U_T)	31.6	31.6	19.1	27.7	31.6	31.6

3. REALIZATION OF BASIC LOGIC GATES USING THE PROPOSED SINGLE BIT COMPARATOR

This section deals with the designing of basic logic gates using the structure of the single bit comparator. The same design can be used as an AND, OR, NAND, NOR, XOR, XNOR, BUFFER and INVERTER GATE.

As it can be seen from Figure 10(a), when the polarization at the centre is given to be -1, then the corresponding outputs from different cells are given. Figure 10(b) gives the outputs of the same cells when a polarization of +1 is given. We are taking the outputs A'B as (A<B) output cell and AB' as (A>B) output cell. The AB + A'B' gives the (A=B) output cell. Along with these we get some other outputs as well as illustrated in Figures 10(a) and 10(b).We get the AND and OR gates as well from the comparator circuit. It is not unknown that if we invert the output of AND and OR gates we get NAND and NOR respectively. In QCA this is done by adding a cell on top of the output cell in a different layer taking the inverted output from there. In this way we can get the AND, NAND, OR and NOR gates from our proposed comparator design.

As it can be seen in Figure 11, the same comparator structure is used to implement the basic logic gates along with a buffer.

Realization of the fundamental logic gates using the proposed comparator circuit design can be seen as below.

I) AND Gate: To make an AND gate, we just need to take the cell present between the two input cells as the output cell (refer to Figure 10(a)).

II) OR Gate: To make an OR gate, we just need to take the cell present between the two input cells as the output cell (refer to Figure 10(b)).

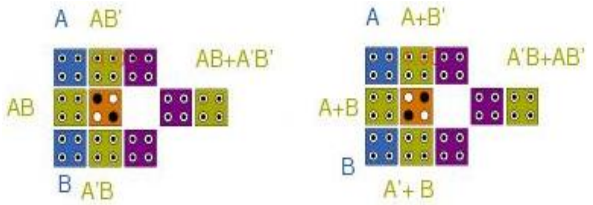


Figure 10. Outputs taken from the Comparator Circuit

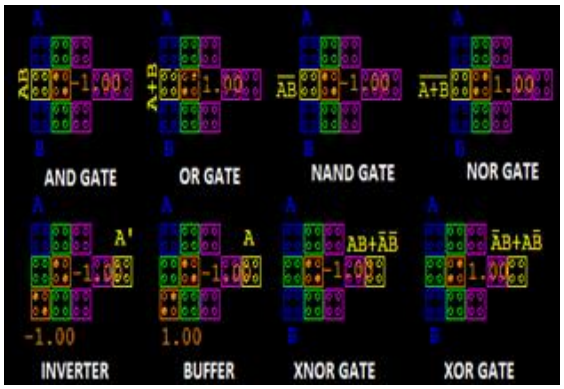


Figure 11. QCA layout of AND, OR, NAND, NOR, INVERTER, BUFFER XNOR and XOR

III) NAND Gate: NAND = AND + NOT. Hence, the cell just above the AND output cell in the new layer is taken as the NAND output cell (refer to Figure 11(top row, second from right).

IV) NOR Gate: NOR = OR + NOT. Hence, the cell above the OR output cell in a different layer is taken as the NOR output cell (refer to Figure 11(top row, rightmost)).

V) INVERTER: In the XNOR gate, if we replace the input cell B with polarization -1, we shall get an INVERTER.

XNOR => Y = AB+A'B'. If B=0, then Y = A' => an INVERTER.

VI) BUFFER: In the XNOR gate, if we replace the input cell B with polarization +1, we shall get a BUFFER.

XNOR => Y = AB+A'B'. If B=1, then Y = A => a BUFFER.

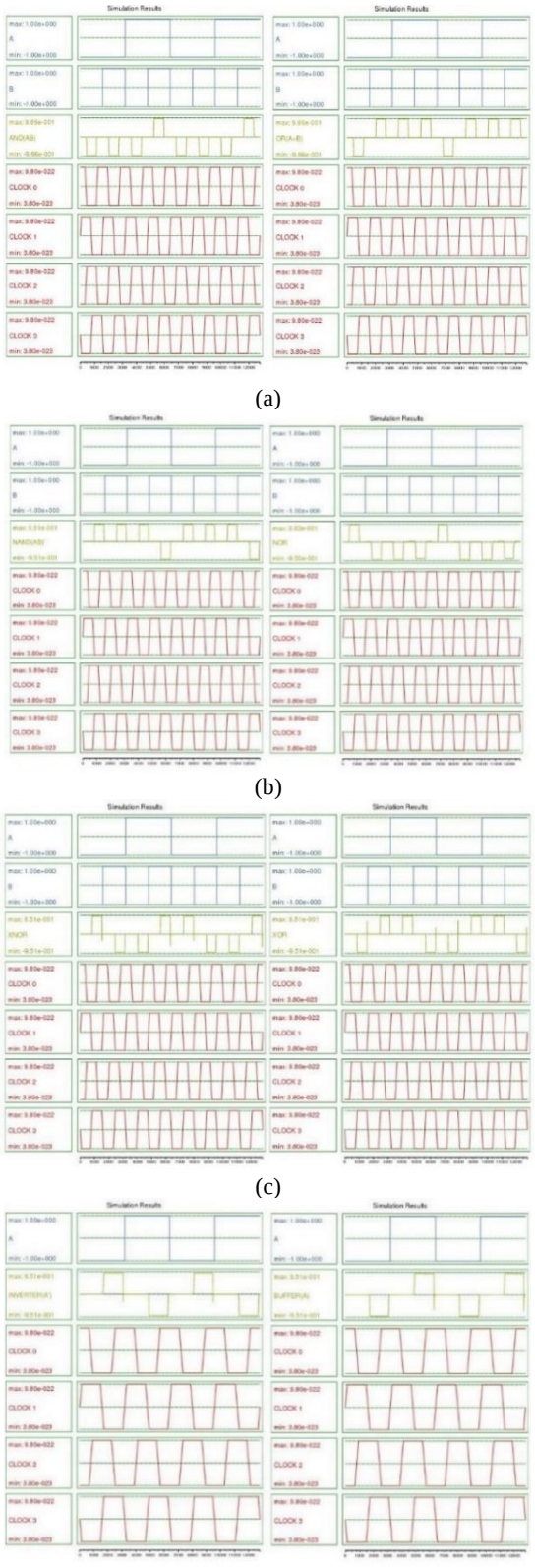
VII) XNOR Gate: In a comparator circuit, A=B is calculated using the XNOR gate. Hence, no extra design is required for the XNOR gate because it can be obtained from the comparator circuit itself.

VIII) XOR Gate: To make a XOR gate, we just need to change the polarization of the polarized cell of the comparator from -1.00 to +1.00. The position of the output cell remains same as that of the A=B comparator output (refer to Figure 11 (bottom row, rightmost)).

In Figure 12, output graphs of the fundamental logic gates using the proposed comparator circuit design are shown.

4. OBSERVATION AND RESULTS

Table 4 draws the comparisons among previously proposed single bit comparators to our proposed design with respect to cell count and area consumpsion. Proposed design consists of 14 cells and consumption of area is 0.0089 μm^2. This design can be alternatively used as the basic logic gates which has been discussed in section 3.



(a)

(b)

(c)

(d)

Figure 12. Output of the basic logic gates implemented using the proposed design. (a) AND & OR Gate, (b) NAND & NOR Gate, (c) INVERTER & BUFFER, (d) XNOR & XOR Gate

TABLE 4. Observations for 1-bit comparators

Comparator Design	No. of Cells	Area (μm^2)	Delay (clock cycle)
[7]	81	0.06	0.75
[8]	42	0.05	0.75
[9]	37	0.028	1
[10]	58	0.055	0.75
[11]	100	0.11	0.75
[12]	38	0.03	0.5
[13]	31	0.04	0.75
[14]	40	0.05	0.75
[15]	79	0.07	1
[16]	73	0.06	1
[17]	26	0.023	0.5
[١٨]	٣١	٠,٠٣	0.75
Proposed Design	14	0.0089	0.5

5. CONCLUSION

In this paper we have discussed about the design of 14 cell single bit comparator circuit and used it to design of the basic logic gates. During the comparison of the circuit with other previously proposed designs the number of cells used to formulate this is 14 which is the lowest till date. Thus we are able to propose a novel comparator design which is area efficient and also can be used in basic digital designs. The advantage of our design is that we are getting all the gates along with the comparator output. This comparator circuit can be used as a universal structure for forming the basic gates instead of the majority voter as this design is more compact and is less prone to errors.

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Persian Abstract

چکیده

آنتن کوانتوم دات سلولار (QCA) یک ترانزیستور نویدبخش با فناوری نانو کمتر است که محبوبیت روزافزون خود را افزایش می دهد و این قابلیت را دارد که در همه جا از فناوری نیمه هادی اکسید فلزی مکمل (CMOS)در حوزه VLSI استفاده کرد. این مقاله به طراحی ساده مدار مقایسه کننده تک بیتی با استفاده از QCA پرداخته است. یک مدار مقایسه ای تک بیتی دو ورودی خود را مقایسه می کند و نشان می دهد که کدام یک بزرگتر است یا هر دو برابر هستند. این مقاله بر ایجاد یک مدار مقایسه ای QCA کارآمد در منطقه و مطالعه مقایسه ای مصرف سطح با طراحی های قبلی تمرکز کرده است. مدار مقایسه شده طراحی شده از نظر مساحت کارآمدترین طرح است زیرا از حداقل تعداد ممکن سلول تشکیل شده است. یک مقایسه کننده در آزمایش کننده های برابری و بسیاری دیگر از ارتباطات دیجیتالی استفاده می شود. مدار ارائه شده در این مقاله یک مدار سه لایه است که به طور متناوب می تواند برای تحقق دروازه های منطقی اساسی مورد استفاده قرار گیرد. این مدار همچنین می تواند به عنوان جایگزینی برای دروازه های اکثریت و جهانی در QCA استفاده شود.