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Using Universal Nand-nor-inverter Gate to Design D-latch and D Flip-flop in Quantum-dot Cellular Automata Nanotechnology

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ABSTRACT

The process of reducing dimensions in CMOS technology and also making digital devices more portable, faces serious challenges such as increasing frequency and reducing power consumption. For this reason, scientists are looking for a solution such as replacing CMOS technology with other technologies including Quantum-dot Cellular Automata (QCA) technology and many researches have designed digital circuits by using QCA technology. Flip-flops are one of the main blocks in most digital circuits. In this paper, a D-type flip-flop (D-FF) is presented in QCA technology that a majority gate has been used in its feedback path to reset. The D-FF is designed by the proposed D Latch which is based on Nand-Nor-Inverter (NNI) and a new inverter gate that the proposed D latch has 24 cells and 0.5 clock cycle latency and 0.02 μm^2 area. The new inverter gate of the D-FF has output signal with high polarization level and lower area than previous inverters and the NNI gate of the D-FF is a universal gate. One of the applications of D-FFs with reset pin is the use in Phase-frequency detector (PFD). In the proposed scheme, a reset feature has been added to D-FF since the PFD structure can be designed. All of the proposed schemes are evaluated by the QCADesigner software and energy consumption simulations are estimated using QCAPro software for all proposed circuits.

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1. INTRODUCTION

CMOS technology is faced with serious challenges such as short-channel effects, cut-off leakage, and high power consumption. Hence, the researchers have proposed alternatives to replace CMOS technology. One of these technologies is QCA technology [1]. The circuits designed in QCA technology use a square cell with size of a molecule or an atom. These QCA circuits can operate at around the terahertz frequencies because of not containing any output capacitors. Since there is no current in QCA circuits, their power consumption is less than CMOS circuits [2, 3].

Today, many digital systems include storage elements, sequential logic circuits and combinational logic circuits. The storage elements have capable of storing binary information. Fip-flop as a storage element has ability of storing one bit. The flip-flops are based on latches which operate with signal levels [4]. Flip-flops are used in phase/frequency detector (PFD) of a Phase-Locked Loop (PLL) and a Delay-Locked Loop (DLL). For an example, the convensional PFD is designed by using D flip-flops [5-8].

Different D latches and D-FFs have been designed in QCA technology [9-16]. In QCA technology, digital circuits such as latches are compared in terms of area, latency and number of cells. Some of these circuits are suitable and capable of using in large circuits, but some other are not. By latency we mean number of clocks needed for generating the valid output signal.

Dehkordi, and Sadeghi [9], have designed D latch with 43 cells and a 1.25 clock cycle latency. This D latch design has a NOT gate with larger number of cells and area than the convetional NOT gate. Also, this D latch has high latency compared to current work. Hashemi and Navi [10] have proposed the D latch which has large number of cells, occupying massive area and high latency compared to current works. Also, a NOT gate uses as in

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the previous work [9]. Abutaleb [11], has proposed a design for D latch with 28 cells and 0.02 μm^2 area and 0.5 clock cycle latency, but it does not follow the basic design rules of QCA well. Sasamal et al. [12] have designed D latch with rotated majority gate, however, this design is less stable than other designs existing in literature. A D latch is designed with a 2-input multiplexer gate in literature [13] that reduces cell number and stability compared to the previous design but increases the latency. Zoka and Gholami [14] have designed D-FF with reset pin that has a large number of cells and high latency, and also in order to become resetting, the input associated with resetting must be constantly active leading to high energy dissipation. D-FF with reset terminal in literature [15], has reduced latency while number of cells and area are large, however, the D-FF uses coplanar crossovers. Binaei and Gholami [16] have designed D-FF with reset pin has only reduced number of cells when comparing to our work.

In this work, first, a universal gate, called NNI gate, is used in D-latch and D flip-flop. Second, a method for creating D flip-flop with reset pin is introduced in which the D flip-flop resets by interrupting the feedback path. Third, a new PFD is designed in QCA Technology. The NNI gates used in the D latch hass low latency. The D flip-flop designed based on the D-latch is sensitive with rising edges of the clock.

The next section describes the QCA structure. In section 3, the proposed structures for D latch, D-FFs and PFD will be explained. Section 4 is about simulation and the results.

2. THE BASIC PRINCIPLES OF QCA

In QCA technology, logic circuits are designed based on a square cell. This cell has 4 quantum holes or dots in its four corners where two of the dots are charged with two electrons. The electrons have moving ability among these dots by tunneling between them. The logical state is determined by the arrangement of electrons of within this cell. Due to repulsive force of the same charges, these electrons have two stable situations that the two stable situations are considered as ZERO and ONE logical in digital circuits. There are two forms of arrangement for these cells, 45° and 90° [17, 18].

According to coulomb repulsion force law, the electrons within dots of adjacent cells act on each other. So, in this way the data is transferred from one cell to its adjacent cell. Thus a wire can be implemented by putting a row of cells together. Because of the arrangement of cells in the two forms of 90° and 45°, there are two models of wire alignment [13]. To generate different signals in wire crossings, there are two crossover options in QCA technology: coplanar crossings [19] and multilayer crossover [20].

Two basic gates known in QCA technology are majority gate and inverter. By using the colony force and mutual interaction between cells, these basic gates can be made in QCA technology.

To have a synchronous circuits in QCA technology, in addition to control data flow in the wire to the same as that in a pipeline, a clock zone method is used. To operate correctly, Functional QCA circuits need clock [13, 21]. The cells also operate on clock. Clocking has two roles in QCA. It controls data flow and serves as power supply [3]. Although mapping conventional logic functions to majority logic can be done easily, the clock scheme in QCA makes directly conversion of a CMOS architecture into QCA counterpart difficult. The main unit of such designs is majority gate while this gate isn't a universal gate and cannot realize the logical NOT operation. The designers must consider a separate costly QCA cell arrangements for realization of the logical NOT. By combining these functions with inverters, these logical components are used to implement other logical functions. Therefore, a universal gate structure called the Nand-Nor-Inverter (NNI) has been introduced by Sen and Sikdar [22] which can be used as a logical element for QCA-based designs. This gate implements the function of $F = NNI(A, B, C) = maj(A', B, C') = A'B + BC' + C'A'$.

3. THE PROPOSED STRUCTURE

In this section, a D latch and a D-FF are proposed by using the NNI gate [22]. Then, a PFD is designed using the proposed D-FF along with adding a reset pin to demonstrate applicability and usability in larger circuits.

The block diagram of proposed D latch and the design of its structure in QCA technology are shown in Figures 1 and 2, respectively. The proposed D latch has 24 cells and 0.5 clock cycle latency and 0.02 μm^2 area. As shown in Figure 1, a 2:1 multiplexer is designed by using basic gates of QCA technology, and it is converted to D latch by applying feedback path which is shown with dashed line in Figure 1. This proposed D latch is designed with NNI gate [22] and the new inverter gate introduced by Zahmatkesh et al. [23].

Then, the proposed D latch is converted to a D-FF by adding a level-to-edge converter on the clock input. The D-FF is shown in Figure 3. The level-to-edge converter is a logic circuit that converts level to falling, rising or dual edge. The level-to-rising edge converter used in the proposed D-FF is shown by dashed rectangle in Figure 3. The NNI gate is used in this converter to reduce number of cell, area, and also the complexity of the circuit. Function of rising edge converter is $CLK_{new}(t) = CLK(t).\overline{CLK(t-1)}$ [13]. The proposed D-FF of Figure 3 has 43 cells and 1 clock cycle latency and 0.04 μm^2 area.

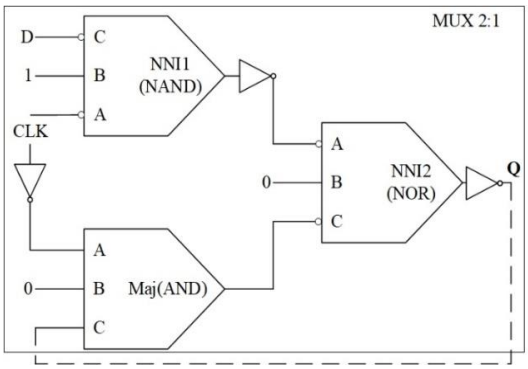

Figure 1. block diagram of proposed D latch

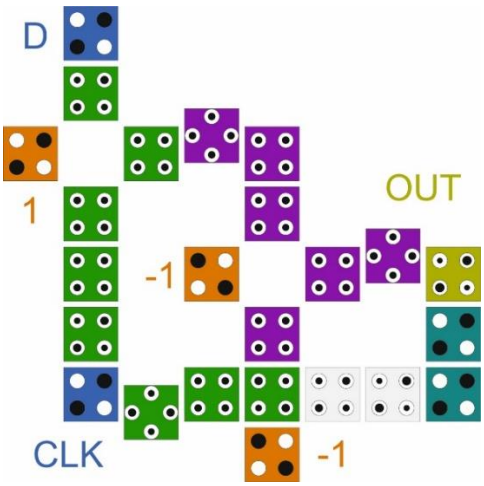

Figure 2. proposed D latch in QCA technology

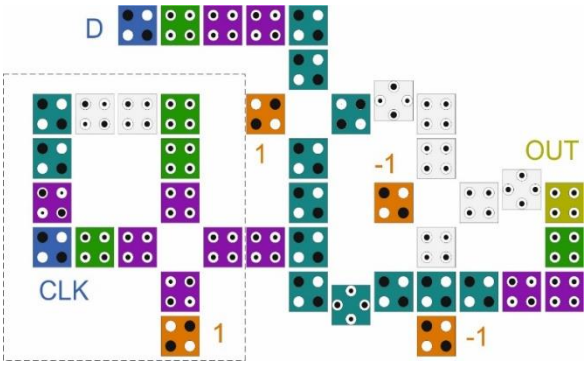

Figure 3. Proposed D-FF in QCA technology

As shown in Figure 4, the proposed D-FF (Figure 3) can be easily converted to a D-FF with reset pin by inserting a 3-input majority gate (Maj2) and changing this majority gate to 2-input AND gate. To reset the D-FF, a logical ONE is applied to one of the inputs of this AND gate (Maj2) while reset pin is set to logic ZERO (because an inverter is used on reset path). Due to this work, applying any value to another inputs of Maj2, same value is resulted in output of Maj2. If reset pin is set to logical ONE, logical ZERO is applied to one of the Maj2 and output of Maj2 becomes logical ZERO and this shows how resetting of the proposed D-FF is reset with the reset pin. The block diagram for the proposed D-FF with reset pin and its circuit in QCA technology are shown in Figures 4 and 5, respectively.

The proposed D-FF with reset pin consists of 54 cells, 1.25 clock cycle latency and 0.047 μm^2 area. Finally, the proposed PFD structure can be designed by using two the proposed D-FFs with reset pin and an AND gate. If the PFD circuit is designed based on conventional block diagram [5], the outputs of PFD will have no correct values due to the pipeline feature of QCA circuits. Therefore, the PFD circuit in QCA technology is designed based on block diagram shown in Figure 6 in which a subtraction operation is performed at the end of the proposed PFD circuit illustrated in this figure by dashed rectangle. The proposed PFD in QCA technology is depicted in Figure 7. As it can be seen in this figure, in the proposed PFD, the outputs of two D-FFs with reset pin are connected to the AND gate. Theoutput of the AND gate is connected to the reset pins of the D-FFs. As both D-FFs become high output simultaneously, the reset operation is completed by the AND gate, this implies that the PFD has calculated phase and frequency difference. According to Figure 6, the subtraction operation is as follows. Output of D-FF1 with reverse of output of D-FF2 are connected to the inputs of AND gate (1). The

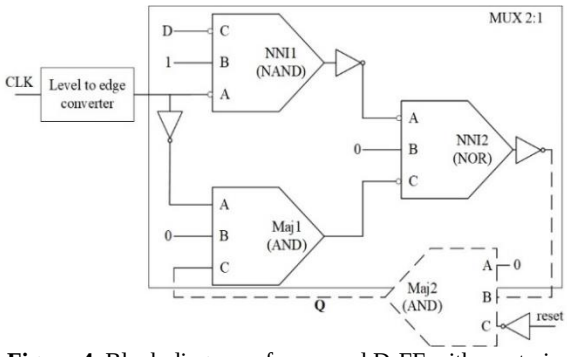

Figure 4. Block diagram of proposed D-FF with reset pin

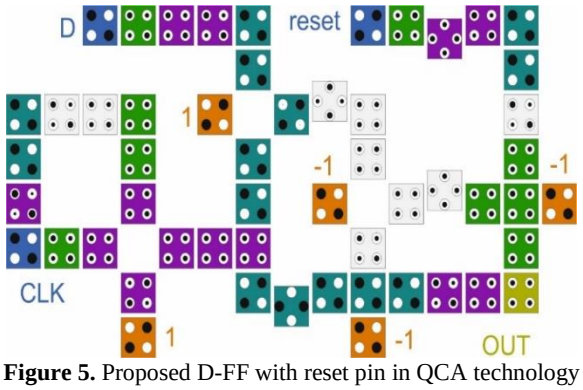

Figure 5. Proposed D-FF with reset pin in QCA technology

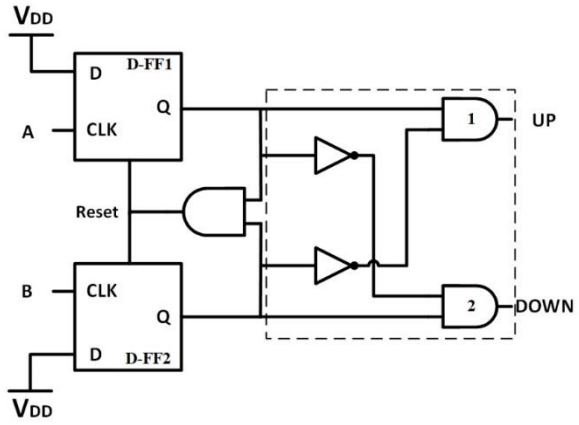

Figure 6. Block diagram of proposed PFD

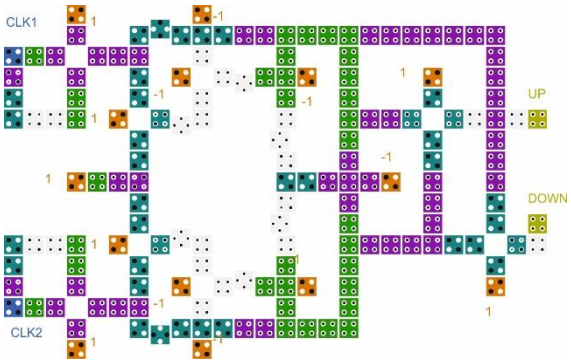

Figure 7. Proposed PFD circuit in QCA technology

output of AND gate (1) is correct UP output of the PFD. Then, the output of D-FF2 with reverse of output of D-FF1 are connected to the inputs of another AND gate (2), and the output of this AND gate (2) is DOWN output of the PFD. By doing this, latency does not affect outputs of the PFD. In this design the AND gates are designed based on NNI gate. This helps omitting inverter gate on the paths that where inputs are required to be reversed. So, this acting reduces the complexity and area of the circuit. The proposed PFD consists of 161 cells, 2 clock cycle latency and 0.175 μm^2 area.

4. SIMULATIONS AND RESULTS

In this section, the results of simulations and the energy dissipation for the proposed circuits are expressed. The simulations of the circuits' schemes has been done by QCADesigner software version 2.0.3 [24]. For better performance of QCA circuit analysis, all proposed QCA schemes were investigated using both coherence vector and bistable approximation simulation engines with default parameters.

First, the simulation results for the proposed D latch of Figure 2 can be seen in Figure 8 that the output depends on logical ONE level of the clock input. When the input of the clock becomes logical ONE level, the D input is sampled. This means that it responds to logical ONE level of the clock pulse. On the other hand, when the level becomes logical ZERO, the proposed D latch is stored the last value of its output. All of these actions are marked with arrows. The state of a latch or flip-flop is switched when a change in the control input occurs. This momentary change is called a *trigger*, and the transition caused by it is called flip-flop triggering. This means that clock input of the latch is sensitive to level, but clock input of the flip-flop is sensitive to edge and latch is converted to flip-flop by placing a level-to-edge converter at the clock input of latch. This flip-flop can be sensitive to falling, rising or dual edge. The simulation results for proposed D-FF with reset pin is illustrated in Figure 9. As shown in Figure 9 is marked with arrows, this D flip-flop is sensitive to rising edge. At any

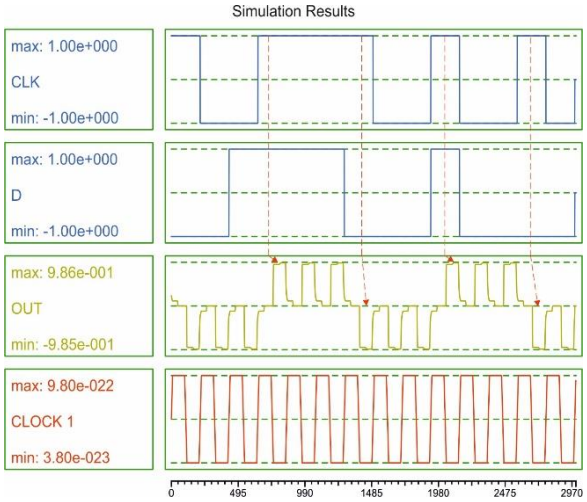

Figure 8. Simulation results of proposed D-latch

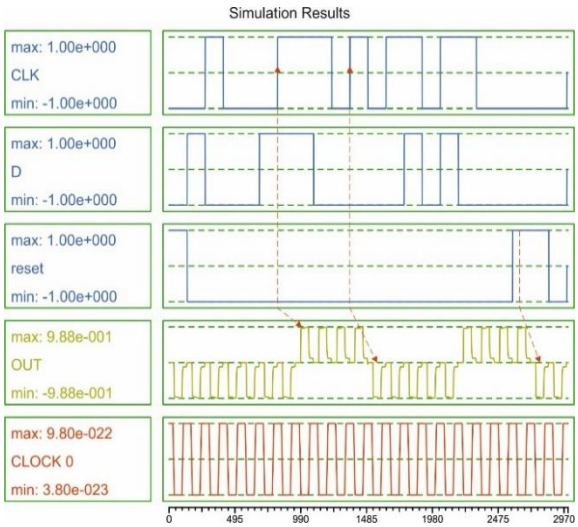

Figure 9. Simulation results of proposed D-FF with reset pin

moments that the clock input sense rising edges, value of D input is transferred to the output. When the reset input is set to logical ONE, output of D-FF with reset pin reaches logical ZERO. Tables 1 and 2 show the comparison of proposed D latch and D-FF with related designs. As it can be seen in these the proposed D-FF has the best delay performance while it contains few number of cells, and also energy dissipation of the proposed D-FF has improved.

Finally, the simulation results of the proposed PFD are shown in Figures 10, 11 and 12. The PFD can detect phase and frequency differences of its input signals. For this purpose, simulations of Figures 10 and 11 is performed, two signals are shown with the same frequency and different phases in Figure 10 and the proposed PFD detects phase difference of these two signals. Two signals with different frequencies are applied to inputs of the proposed PFD and the results are shown in Figure 11. In Figure 12, two different inputs are applied to inputs of proposed PFD, in order to test its detecting ability of phase differences for both inputs. Table 3 is listed comparison of the proposed PFD with other related works. As shown in Table 3, structure of the proposed PFD has improved in terms of cells, area, latency and energy dissipations.

TABLE 1. Comparison of the proposed D latch with other related works

Structure	Cells count	Area (μm^2)	Latency	Average switching energy dissipation (meV) $0.5E_k$	Average leakage energy dissipation (meV) $0.5E_k$
D latch in [9]	43	0.04	1.25	-	-
D latch in [10]	48	0.05	1	-	-
D latch in [11]	28	0.02	0.5	31.50	8.49
D latch in [12]	23	0.02	0.5	-	-
D latch in [13]	19	0.02	0.75	0.00467	0.03033
Proposed D latch in figure 2	24	0.02	0.5	0.01689	0.01041

TABLE 2. Comparison of the proposed D-FF with reset pin with other related works

Structure	Cells count	Area (μm^2)	Latency	Average switching energy dissipation (meV), $0.5E_k$	Average leakage energy dissipation (meV), $0.5E_k$
D-FF in [14]	82	0.11	2	-	-
D-FF in [15]	95	0.11	1	-	-
asynchronous D-FF in [16]	73	0.11	3	0.05643	0.02574
synchronous D-FF in [16]	73	0.1	2.5	0.04319	0.02656
Proposed D-FF in fig. 5	54	0.047	1.25	0.04414	0.02205

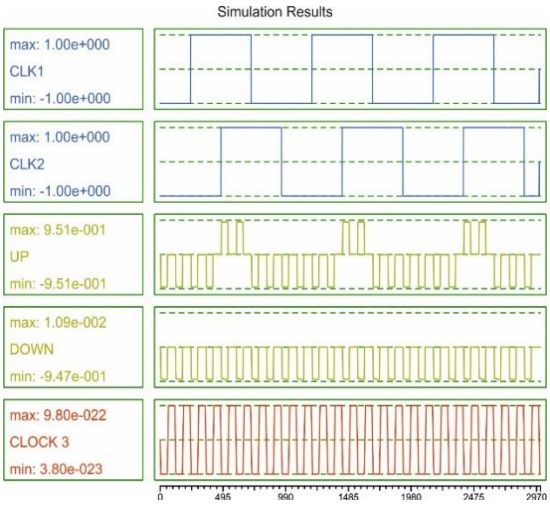

Figure 10. Detect different phases

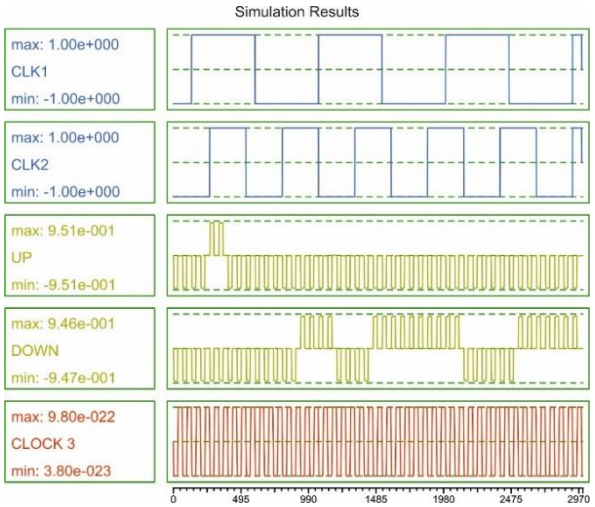

Figure 11. Detect different frequencies

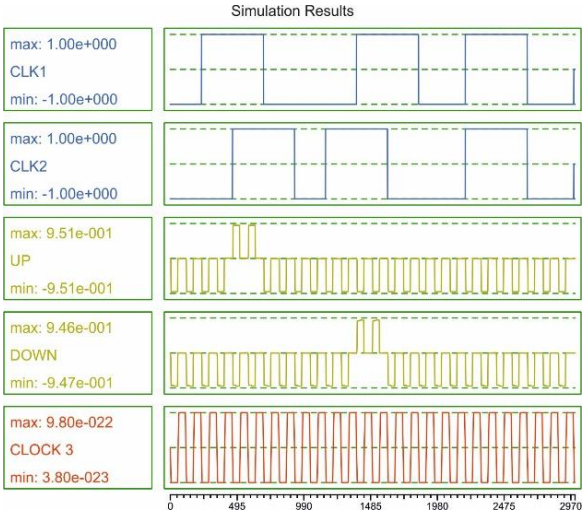

Figure 12. Correct examination two input of proposed PFD

Power consumption analysis of proposed designs is done by QCAPro software that the software uses a fast approximation method to estimate the most erroneous cells in the QCA circuit design [25]. Power dissipation maps for the proposed circuits of Figures 2, 5, and 7 with $0.5E_k$ are illustrated in Figures 13 to 15, respectively. QCA logic gates are thought to be ideal, so there is no charge transfer between cells and current does not flow. Also, the electric charges do not leave any cell, no current is released. These gates cause energy dissipation and we compare the energy consumption of conventional QCA logic gates in electrostatic and thermodynamic approaches. The results show that by increasing the number of inputs, the geometry concentration and the unbalanced numbers of "0" and "1" output modes in the gate truth table will add to the energy dissipation of a QCA gate. We believe that electron transfer between points is a wasteful phenomenon, though the net current is zero. Figures 13, 14 and 15 show that there are dissipations [29]. Darker points define points with more energy dissipation in these figures. The vectors of Figures 8 to 10 are employed for power dissipation maps in Figures 13 to 15, respectively. In Table 4, average for switching energy dissipation and leakage energy dissipation have been listed for the proposed structures and for the power dissipation maps in Figures 13 to 15.

TABLE 3. Comparison of the proposed PFD with other related works

Structure	Cells count	Area (μm^2)	Latency	Average switching energy dissipation (meV), $0.5E_k$	Average leakage energy dissipation (meV), $0.5E_k$
PFD in [26]	199	0.22	2	0.09642	0.06169
PFD in [27]	170	0.26	2.75	0.08667	0.06530
PFD in [28]	159	0.2	2.25	0.03771	0.05370
PFD in [29]	141	0.17	2	0.08679	0.05061
Proposed PFD in figure 7	161	0.175	2	0.05555	0.06202

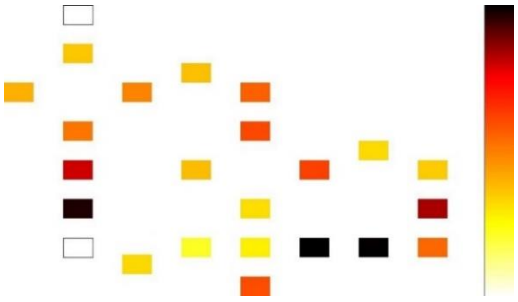

Figure 13. Power dissipation maps for proposed D latch with $0.5E_k$

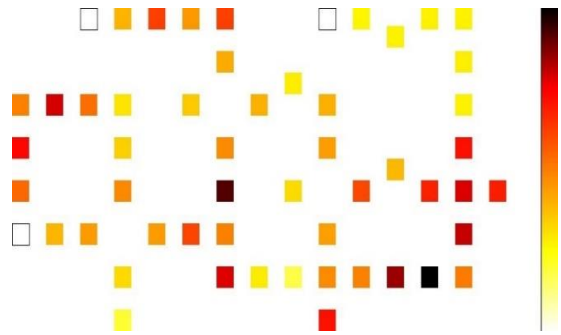

Figure 14. Power dissipation maps for proposed D-FF with reset pin with $0.5E_k$

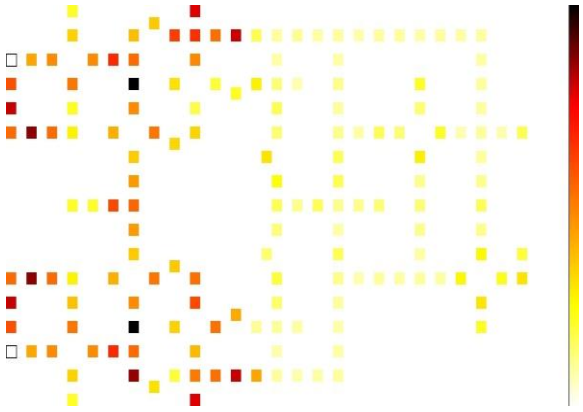

Figure 15. Power dissipation maps for proposed PFD with $0.5E_k$

TABLE 4. Power analysis results

	Average switching energy dissipation (meV)			Average leakage energy dissipation (meV)		
	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$
Proposed D latch in figure 2	0.01689	0.01358	0.01101	0.01041	0.02637	0.04328
Proposed D-FF with reset pin in figure 5	0.04414	0.03510	0.02819	0.02205	0.05909	0.09869
Proposed PFD in figure 7	0.05555	0.04347	0.03464	0.06202	0.17174	0.29340

5. CONCLUSION

In this paper a novel D-latch has been designed based on QCA nanotechnology. The proposed D-latch uses NNI gate. The proposed D-latch has only 24 QCA cells, 0.02μm^2 and delay of 0.5 cycle of QCA clock. These parameters indicate that the proposed D-latch has improved compared to previous work, and this D-latch improves the design of larger circuits. Then, the proposed D-latch is used to have a new D-FF in QCA nanotechnology. Reset ability is added to proposed D-FF since this pin is needed in many applications of D-FFs such as counter, shift register and PFD. To show the correct performance of the proposed D-FF with reset ability, it is used in PFD structure. Also, PFD can be used in PLL and DLL. power simulations for all of the proposed designs have been reported.

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Persian Abstract

چکیده

روند کاهش ابعاد در فناوری CMOS و همچنین قابل حمل تر شدن دستگاه های دیجیتال، با چالش‌های جدی از جمله افزایش فرکانس و کاهش توان مصرفی روبرو است. به همین دلیل دانشمندان به دنبال راه‌حلی مانند جایگزینی فناوری CMOS با فناوری دیگری از جمله فناوری آتاماتای سلولی دات–کوانتومی (QCA) است و بساری از محققان مدارهای دیجیتالی با استفاده از فناوری QCA طراحی کرده‌اند. فلیپ‌فلاپ‌ها یکی از بلوک‌های اصلی در اکثر مدارهای دیجیتالی هستند. دراین مقاله، یک فلیپ‌فلاپ نوع D در تکنولوژی QCA ارائه می‌شود که از یک گیت اکثریت در مسیر فیدبک آن جهت بازنشانی استفاده شده است. فلیپ‌فلاپ D توسط لچ D پیشنهادی مبتنی‌بر گیت Nand-Nor-Inverter (NNI) و گیت وارونگر جدید طراحی شده که لچ D پیشنهادی ۲۴ سلول و ۰/۵ دوره چرخش کلاک تاخیر و مساحت $0.02\ \mu m^2$ دارد. گیت وارونگر فلیپ‌فلاپ D سیگنال خروجی با سطح قطبیت زیاد و مساحت کمتر نسبت به وارونگرهای گذشته دارد و گیت NNI فلیپ‌فلاپ D گیتی یونیورسال می‌باشد. یکی از کاربردهای فلیپ‌فلاپ D استفاده در آشکارساز فاز–فرکانس (PFD) است. در طرح پیشنهادی ویژگی بازنشانی به فلیپ‌فلاپ D اضافه شده تا ساختار PFD را بتوان طراحی کرد. تمام طرح‌های پیشنهادی توسط نرم‌افزار QCADesigner و شبیه‌سازی انرژی مصرفی برای همه مدارات پیشنهادی با استفاده از نرم‌افزار QCAPro سنجیده شده‌اند.