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Designing Bi-directional Counters using Quantum-dot Cellular Automata Nanotechnology

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ABSTRACT

One of the major problems in designing highly compact integrated circuits is the power consumption of the circuits. Therefore, several technologies have been introduced to overcome the problems facing MOSFET technology. One of these technologies is the Quantum-Dot Cellular Atomata (QCA), which has several advantages. In this paper, we focus on computational logic gates based on the T-Latch circuit. T-latch is the basis of many circuit in arithmetic logic unit (ALU). The proposed structure for T-latch has a lower number of cells, occupied area and lower power consumption than existing methods. In the proposed T-Latch, compared to previous best designs, 6.45% cross section area and 44.49% power consumption were reduced. Also in this paper, for the first time a T-latch with reset terminal and a T-Latch with both set and reset terminals were designed. In addition, using the proposed T-latch, a 3-bit bidirectional up-down counter which consists of 204 quantum cells, 0.26 μm^2 cross-sectional area, delay of 5.25 clock cycles, a three-bit up-down counter with a reset pin and a three-bit up-down counter with set and reset terminals were made. The proposed up-down circuits are designed for the first time in QCA technology. All the design and simulation results are done in QCADesigner software.

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1. INTRODUCTION

In recent years, manufacturing of integrated circuits has improved with CMOS technology [1]. Reducing the size of transistors has reduced power consumption and increased the speed of integrated circuits [2], but due to the physical limitations of CMOS technology, ample research has begun to produce a new generation of integrated circuits. Among the emerging technologies, the technology of quantum cellular automata is more prominent than other technologies [3]. This technology has simple cells that are used as key elements in the creation of gates, wires and memories [4]. Also, while having a simpler structure, it has other capabilities, such as high speed and low power consumption, due to the small number of elements used in the circuit structure than complementary metal oxide semiconductor (MOS) technology [5]. It also looks like this technology will be a new way to implement digital circuits in the future [6].

Counters are the most common circuits in the processing unit, and these circuits are generally sequential logic circuits that are activated by an external signal called a clock signal [7]. In the previous works, counters have been introduced in QCA technology, each of which has its advantages and disadvantages. Amirzadeh and Gholami [8] proposed a 3-bit D-type flip-flop based counter that has relatively large cell counts and cross-sections area, and high latencies despite proper performance. It has also been suggested Majeed et al. [9] T-type flip-flop based counters that, despite improvements in area level and delay rate, they have a large number of cells. In addition, none of the counters proposed in the past were able to count specific numbers (for example for counting between 2 and 5) due to lack of set and reset terminals. A reset-based counter using D-type flip-flop was proposed by Zoka and Gholami [10], which had a relatively large number of cells, cross-sectional area, delay, and power consumption. Therefore, in this paper, using the proposed T-latch and T-type flip-

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flop structure, bidirectional counters, bidirectional counters with reset capability and bidirectional counters with set and reset capabilities will be presented.

This article will provide the following sections. In the second part, the basic concepts and how to make quantum cells in QCA technology will be discussed. In the third section, the proposed conventional up-down counter circuit and the proposed counter with set and reset terminals in QCA technology are reported. Also, simulation results which shows the performance of the proposed circuits are presented in this section. Finally, power analysis are discussed in section four.

2. BASICS OF QCA

Quantum-dot cellular automata (QCA) is an emerging technology for the design of nanoscale electronic devices that meet the requirements of modern digital systems [11]. In this technology, states are not defined by voltage levels, but by the position of the electrons [12]. In QCA, a cell has four quantum dots located at the corners of a square [13]. Within each cell, there are two free electrons. Because of the electron repulsion between them, these electrons are separated at the farthest distance [14]. Using these cells, different types of QCA based circuits can be made. One of the basic logic gates in the QCA is the majority gate. By using the majority gate and fixing one of the inputs, the AND and OR logic function can be created [15]. Another basic logic gate in a quantum cellular atom is the NOT gate that is obtained by placing the cells obliquely above or below the target cell [16]. Another important block in the QCA is the wire, which is created by putting cells together in a linear fashion. The QCA also uses a clock system to control information from the QCA, which includes four phases Switch, Hold, Release, and Relax.

In the switch phase, the electron wants to get to the new state from the previous state. In the hold phase, the electrons are not affected by the electrons of the adjacent cells and the cell retains its polarity. In the release phase, the energy of the inner points of the cell decreases to a point that the cell loses its polarity. In the relax phase, there are no internal points and the cell does not have any effect on its adjacent cells.

Also, the interdot potential barriers of a QCA cell are induced by electric or magnetic field. So, a common approach to realizing clock circuits is to bury the wires below the QCA level [17].

3. PROPOSED UP-DOWN COUNTERS IN QCA NANOTECHNOLOGY AND SIMULATION RESULTS

Bidirectional counters have the ability to count up and down directions for any given sequence. It is also possible to reverse the count at any point in the counting sequence, using an additional control input [18]. In the following, the proposed bidirectional counters will be discussed and their principles and work will be examined.

The main blocks of the proposed bidirectional counter circuits are T flip-flops and 2×1 multiplexer. In this paper, for the design of the proposed bidirectional counters, proposed T flip-flop and proposed T flip-flop with set and reset terminals are used which are appropriate in terms of cell number of cells, occupied area, and design capability. The proposed bidirectional counter circuits will be designed with minimum cell number and delay while also have reset or set ability. In the proposed designs 2×1 multiplexer is used based on the circuit in literature [19].

One of the most noteworthy topics in circuit design is the memory elements and flip flops that have been considered in QCA technology. T flip-flop is one of these flip flops that is used for toggling an input. T flip-flop is works as follows: if T='1' and in the edge of the clock, the output will reverse the previous state and in all other cases, the output will be the same as its previous state. This is true for flip-flops sensitive to edge of the clock (rising or falling).

A proposed bi-directional counter which counts ascending or descending numbers in QCA nanotechnology is shown in Figure 1. This counter is asynchronous thee-bit up-down counter and is designed using proposed T-flip flops. This counter will counts between 0 (000) and 7 (111). When the down counter's selector is activated, the counter start counting reversely (for example from 7 to 0). So the counting string in this counter, in the up counting mode is 0, 1, 2, 3, 4, 5, 6, 7 and in the down counting mode, it is 7, 6, 5, 4, 3, 2, 1, 0. It should be mentioned that in this block diagram, when both of the selectors are zero, the counter will be UP-counter and when both of the selectors are logical one, the counter will be down-counter. In addition, it should be noted that when the selector's values are being changed, the counting process will start from the same point in reverse manner.

In this design, to have the correct counting numbers for proposed bidirectional counter and also, in order to be able to reverse the count at any point, the circuit diagram block was designed in a way that: Since the circuit is asynchronous and the flip-flops are sensitive

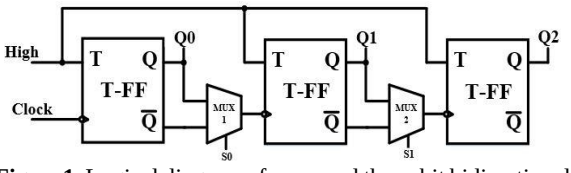

Figure1. Logical diagram of proposed three-bit bidirectional counter

to the downward edges, for counting incremental numbers, the Q output of each flip flop must go to the clock input of next flip-flop, and when the circuit wants to count down, the $\bar{Q}$ output of the each flip flop should be connected to the clock input next flip-flop. Therefore, a multiplexer is used at the output of each flip-flops as shown in Figure 1. As can be seen, the inputs of multiplexer come from outputs of Q and $\bar{Q}$ of flip-flops in previous stages. When the selector input of multiplexer is zero, the Q will be sent to the clock of next stage and the circuit will be up-counter and when the selector is zero, the circuit acts as down-counter since the $\bar{Q}$ will be sent to the clock of next stage. With this logical block diagram, this circuit starts counting from zero to 7 and then starts again to 7 counting and counts to 0 at any point in time that the selectors change from zero to logical one. This is obviously illustrated in Figure 1.

Figure 2 shows the proposed three-bit bidirectional counter structure in QCA technology, which consists of 204 quantum cells, 0.26 μm^2 cross-sectional area, delay of 5.25 clock cycles. The proposed structure consists of three proposed T-latches, three level to edge converters and two 2 × 1 multiplexers which is designed according to structure of Figure 1.

Figure 3 shows the simulation results of the proposed bidirectional counter in QCA technology and works as follows: When the first and second selectors are zero, the up-counting is activated and counter counts from 0 to 7 and every time the first and second selectors

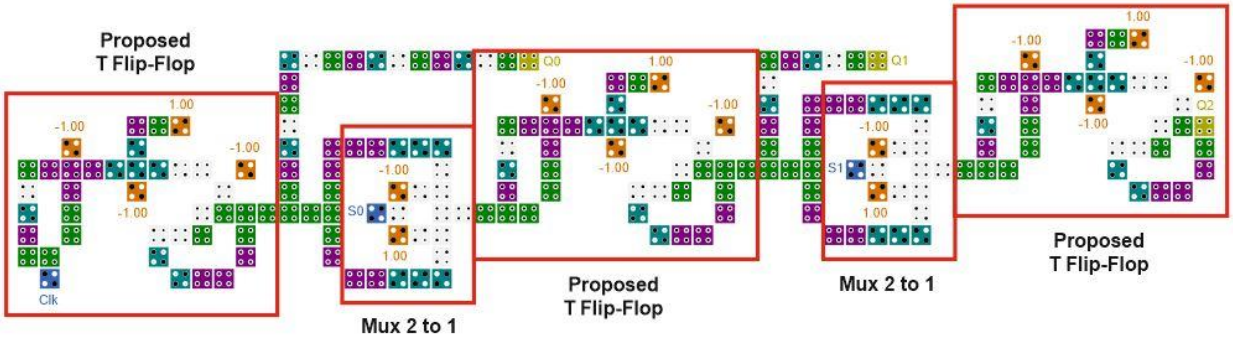

Figure 2. Layout of proposed bidirectional counter

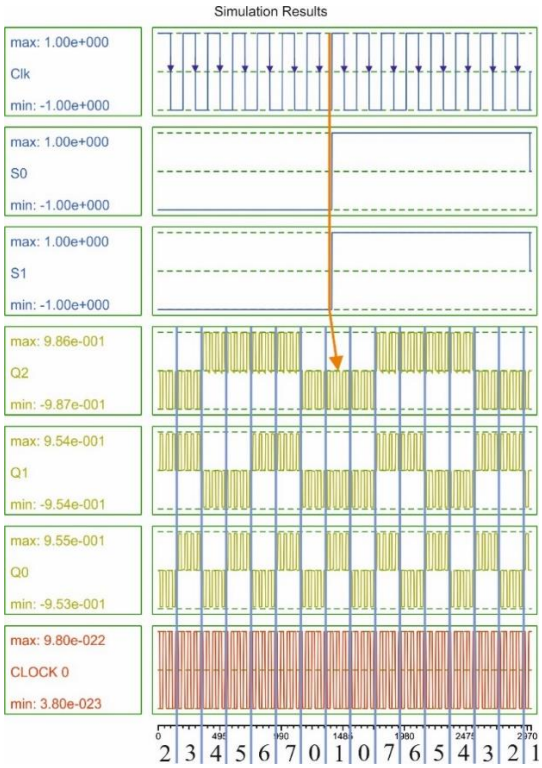

Figure 3. Output waveforms of proposed bidirectional counter

are logical one, the down-counting mode will be activated and the proposed counter starts counting from 7 to 0. As a result, when the first and second selectors are zero and according to the initial conditions given to the circuit, the circuit begins to count upwards and when the selectors become logical one, the counter starts counting backwards at any point in the count. Figure 3 shows the correct operation of the circuit.

Figure 4 shows the block diagram of the proposed bidirectional counter with a reset pin. In this design, to make the circuit correctly counts, and after counting it is possible to reverse the count at any point in the counting sequence and perform the reset operation correctly in the circuit, the circuit block diagram is thus designed according to Figure 4. Based on to this figure the proposed circuit work as follows. When the circuit is

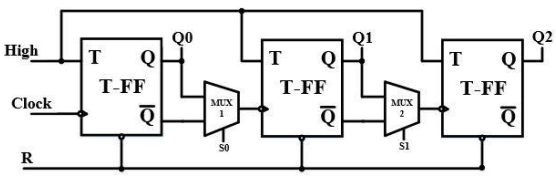

Figure 4. Logical block diagram of proposed bidirectional counter with reset ability

asynchronous and the clock is sensitive to the downward edges, the Q (output of each stages) must go to the clock of the next stage in order to count the upward numbers, and when the circuit wants to count downward, the $\bar{Q}$ must be sent to the clock of the next stage. Therefore, again multiplexer is inserted between each flip-flops to do these acts. As a result, when the first and second selectors are zero and according to the initial conditions given to the circuit, the circuit begins to count upwards and when the selectors become logical one, the counter starts counting backwards at any point in the count. In addition, since this circuit has a reset input, when the reset is activated the output will be zero in any time of counting.

Figure 5 shows the proposed three-bit bidirectional counter with reset ability in QCA technology, comprising 288 cells, 0.36 μm^2 cross-sectional area and 5.75 clock cycles delay. The proposed structure consists of three proposed T-latches with reset input, three level to falling edge converter and two 2 × 1 multiplexers according to topology of Figure 4.

Figure 6 shows the simulation results of the proposed bidirectional reset-based counter in QCA technology and works as follows: When the first and

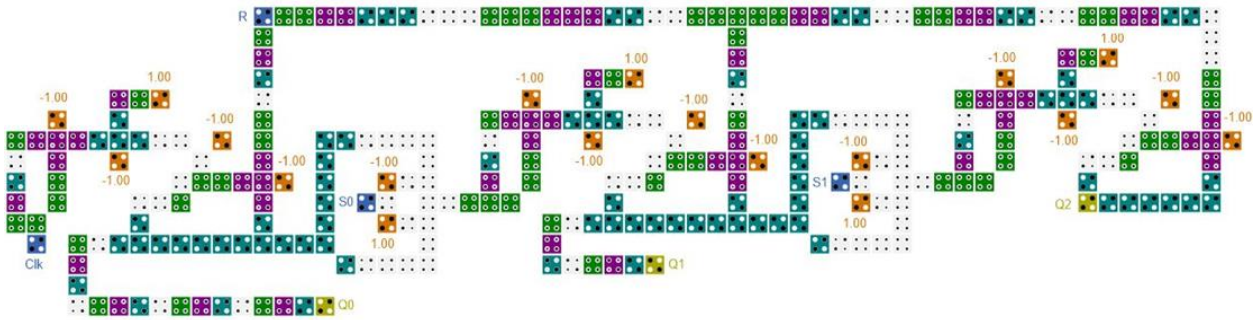

Figure 5. Layout of proposed bidirectional counter with reset ability

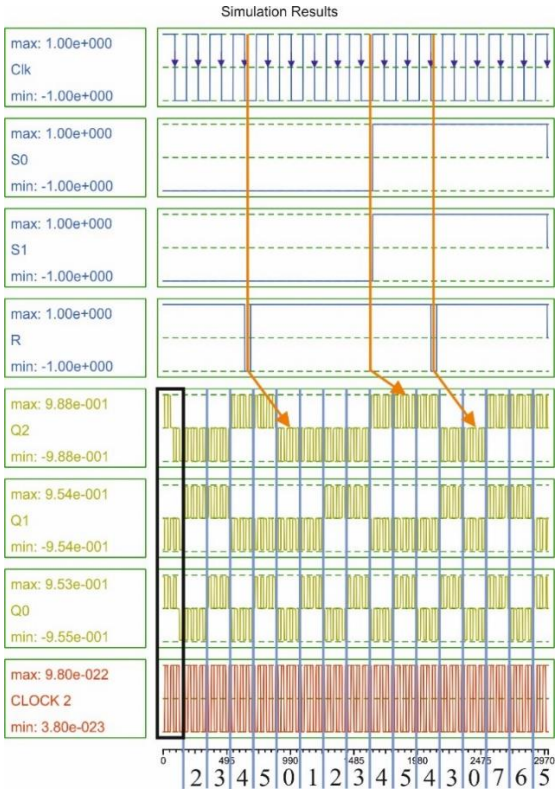

Figure 6. Output waveforms of proposed bidirectional counter with reset ability

second selectors are logical zero, the up-counting is activated and started and when the first and second selectors are logical one, the down-counting will be activated. In addition, since this circuit has a reset input, when the reset is activated the output will be zero in any time of counting. All of these can be seen in Figure 6. Figure 7 shows the block diagram of the proposed bidirectional counter with set and reset inputs. The performance of this circuit is similar to the previous designs and only set and reset capabilities have been added to the proposed counter. With this structure we can have an up-down counter with the ability to count arbitrarily. The counting can be continued in these counters while counting using set and reset inputs from the number that we want.

Figure 8 illustrates the proposed three-bit bi-directional counter-set structure with set and reset inputs in QCA technology, comprising 363 cells, 0.40 μm^2 cross section area, and 5.75 clock cycles delay. The proposed structure consists of three proposed T-latches with a set and reset pins, three level to edge converters and two 2×1 multiplexers designed according to Figure 7. In addition, Figure 9 illustrates the simulation results of the three-bit bi-directional set-counter and the proposed reset in QCA technology. In this figure the process of counting is separated for two cases down and up counting.

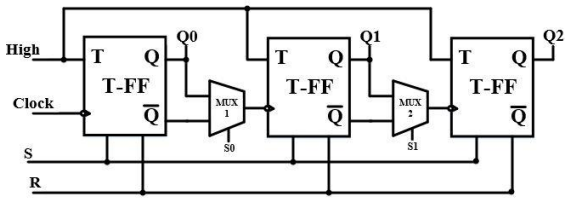

Figure 7. Logical diagram of proposed bidirectional counter with set and reset abilities

Table 1 shows the comparison of proposed designs. Since, bidirectional counter is designed for first time in this paper, we cannot find any related works in this domain for comparing the results.

4. POWER SIMULATIONS

Recent studies show that although there is no electricity in QCA gates, these devices are not without energy loss [20]. The results show that the number of circuit inputs and the geometric compression in QCA are two very effective factors in energy loss [21]. All the proposed designs have been investigated at three tunneling levels $0.5E_K$, $1E_K$ and $1.5E_K$ at T=2ºK. The results are abbreviated in Table 2. Also, all the relationships related to how to calculate energies are discussed by Toress et al. [22]. Figures 10 and 11 show the power consumption of the proposed bidirectional counter structure, the proposed bidirectional counter with reset ability and the

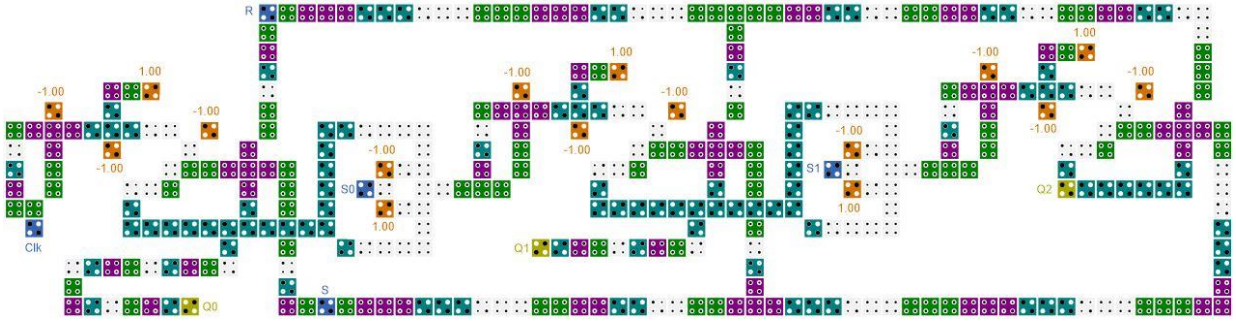

Figure 8. Layout of proposed bidirectional counter with set and reset abilities

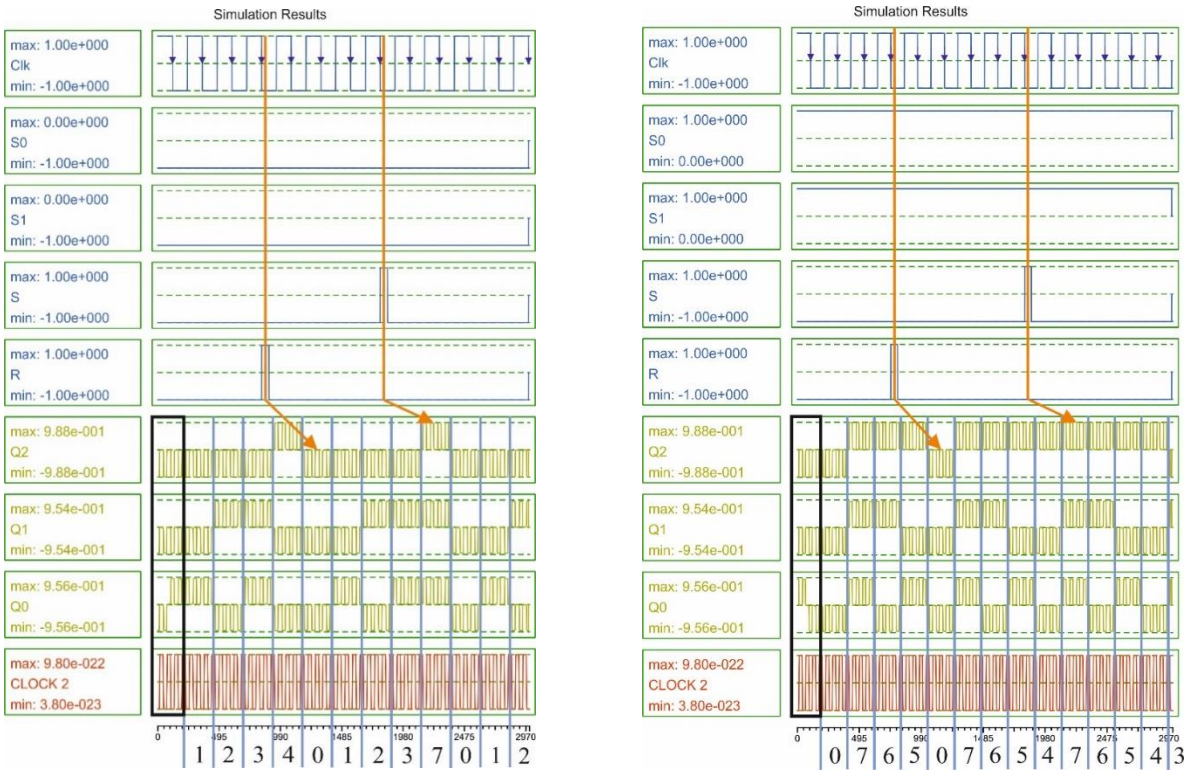

Figure 9. Output waveforms of proposed bidirectional counter with set and reset abilities (a) up direction; (b) down direction

TABLE 1. Results of proposed designs

Circuit	Cell count (# Cells)	Area (μm^2)	Latency ($10^{-12}s$)	Total Energy dissipation 0.5 E_k (meV)	Set input	Reset input
Proposed T-Latch	21	0.0174	0.75	16.22	NO	NO
Proposed T-Latch with Reset	31	0.03	1.25	18.86	NO	YES
Proposed T-Latch with Set and Reset	36	0.04	1.25	22.53	YES	YES
Proposed up-down counter(Fig.2)	204	0.26	5.25	117.77	NO	NO
Proposed up-down with reset (Fig.5)	288	0.36	5.75	213.16	NO	YES
Proposed up down with set and reset (Fig.8)	363	0.40	5.75	167.21	YES	YES

TABLE 2. Results of average leakage energy dissipation and average switching energy dissipation

Circuit	Average Leakage energy dissipation (meV)			Average Switching energy dissipation (meV)		
	0.5 E_K	1.0 E_K	1.5 E_K	0.5 E_K	1.0 E_K	1.5 E_K
Proposed T-Latch	8.36	22.16	36.89	7.86	6.60	5.42
Proposed T-Latch with Reset	11.79	31.69	53.27	7.07	5.93	4.91
Proposed T-Latch with Set and Reset	13.41	36.02	60.64	9.12	7.55	6.22
Proposed up-down counter(Fig.2)	84.68	224.54	377.53	33.09	27.32	22.61
Proposed up-down with reset (Fig.5)	102.62	293.05	508.96	110.54	90.55	73.96
Proposed up down with set and reset (Fig.8)	127.13	366.68	639.28	40.08	33.28	27.54

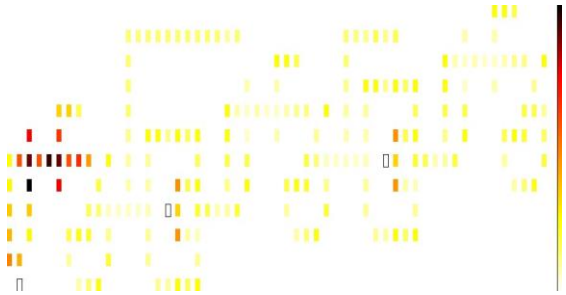

Figure 10. The power dissipation maps of proposed up-down counter

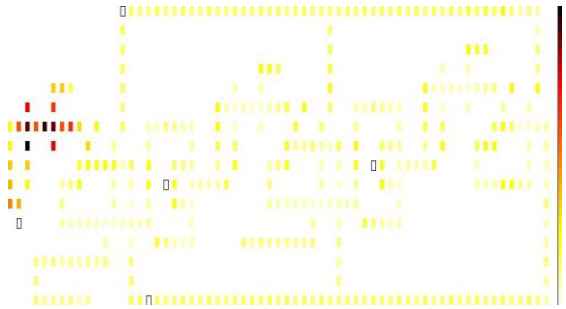

Figure 11. The power dissipation maps of proposed up down with set and reset

proposed up-down counter with set and reset abilites at the 0.5E_K level, respectively. In addition, the results of average leakage energy dissipation and average switching energy dissipation of proposed designs are abbreviated in Table 2.

5. CONCLUSION

In this paper, we discuss the basic concepts of quantum cells and schemes of proposed T flip-flop, T flip-flop with reset and T flip-flop with set and reset. In addition three Up-Down counters are proposed: conventional bidirectional counter, bidirectional counter with reset ability and bidirectional counter with set and reset inputs. Also, the proposed design are simulated using QCADesigner and QCAPro.

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Persian Abstract

چکیده

یکی از مشکلات مهم در طراحی مدارهای مجتمع بسیار فشرده، کاهش توان مصرفی مدارها است. بنابراین تکنولوژی های متعددی برای خروج از مشکلات پیش روی تکنولوژی MOSFET معرفی شده است. یکی از این تکنولوژی‌ها آتوماتای سلولی کوانتومی نقطه ایی (QCA) است، که دارای مزایای متعددی میباشد. در این مقاله بروی گیت های محاسباتی مدار منطقی، لچ T تمرکز گردید که به عنوان مدار پایه در بسیاری از مدارات دیگر و همچنین واحدهای محاسباتی و مقایسه ای استفاده می گردد. ساختار پیشنهاد شده از سلول، مساحت اشغال شده و توان مصرفی کمتری نسبت به روشهای پیاده‌سازی موجود برخوردار است. بطوریکه در لچ T پیشنهادی در مقایسه با بهترین طرحهای گذشته، ٪6.45 سطح مقطع و ٪44.49 توان مصرفی کاهش داده شد. همچنین در این مقاله، برای اولین بار لچ T با پایه ریست و لچ T با پایه ست و ریست نیز طراحی شد. علاوه بر این‌ها در ادامه با استفاده از لچ T پیشنهادی، شمارنده سه بیتی دوجهته (بالا و پایین شمار) که شامل 204 سلول، 0.26 μm^2 سطح مقطع، 5.25 سایکل کلاک تاخیر، شمارنده سه بیتی دوجهته با پایه‌ی ریست و شمارنده سه بیتی دوجهته با پایه‌ی ست و ریست برای اولین بار ساخته شد که با بررسی هایی که صورت گرفته مقالات مشابهی که اعداد را به صورت دوجهته بشمارند وجود نداشته است. تمامی طراحی‌ها و نتایج شبیه سازی‌ها در نرم افزار QCADesigner انجام شده است.